

Structure Silicon Monolithic Integrated Circuit  
 Product Name Power management LSI for mobile phone

Type **BH6056GU**

Features Charge pump DC/DC converter  
 White LED driver 6ch for MAIN, 2ch for SUB  
 General Purpose Output 3ch

○Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Condition
Maximum applied voltage	Vmax	5.5	V	
Power dissipation	Pd	1290 ( * )	mW	
Logic input voltage1	V <sub>LIN1</sub>	GND -0.3 to VBAT +0.3	V	RST
Logic input voltage2	V <sub>LIN2</sub>	GND -0.3 to VDD +0.3	V	SCL, SDA
Logic output voltage1	V <sub>LOUT1</sub>	GND -0.3 to VDD +0.3	V	SDA
Logic output voltage2	V <sub>LOUT2</sub>	DGND -0.3 to 5.5	V	GPO0~GPO2
Storage temperature range	Tstr	-55 to 125	°C	

\* This value is the measurement value that was mounted on the PCB by ROHM.  
 (50mm×58mm×1.8mm glass epoxy Board)  
 Temperature delecting: 12.9mW/°C from Ta>25°C

○Recommended operating conditions (Ta=-30 to 85°C)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
VBAT Battery voltage	VBAT	3.1	3.6	4.8	V	
DVDD Battery voltage	DVDD	2.5	2.9	4.8	V	Use in DVDD ≤ VBAT
Operating temperature range	Topr	-30	25	85	°C	

This product isn't designed to protect itself against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification.  
 A customer may use this translation version only for a reference to help reading the formal version.  
 If there are any differences in translation version of this document, formal version takes priority.

Application example

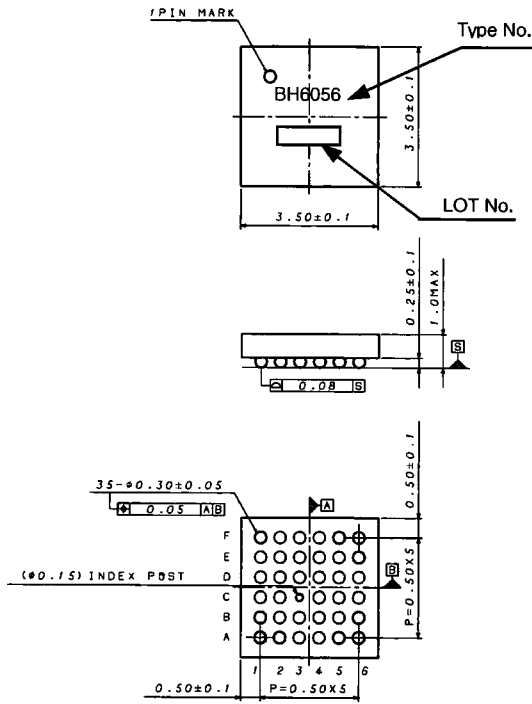
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## ○Electrical Characteristics

Unless otherwise noted, Ta=25°C, VBAT=3.6V, DVDD= 2.9V

Parameter	Symbol	Spec			Unit	Condition
		Min.	Typ.	Max.		
<b>1-1-1-1 Current consumption</b>						
VBAT Current consumption 1	IBAT1	-	-	1.0	μA	RST=L LED Driver all off
VBAT Current consumption 2	IBAT2	-	1.5	3.0	mA	DC/DC converter × 1mode LED Driver MAIN 6ch 10mA
VBAT Current consumption 3	IBAT3	-	8.4	16.0	mA	DC/DC converter × 1.5mode LED Driver MAIN 6ch 10mA
DVDD Current consumption	IDVDD	-	-	1.0	μA	SCL, SDA=fixed All registers are initial state.
<b>1-1-1-2 DC/DC converter</b>						
Output voltage	V <sub>O</sub>	4.0	-	-	V	I <sub>o</sub> =160mA, VBAT≥3.35V DC/DC converter × 1.5mode
Output current	I <sub>omax</sub>	160	-	-	mA	
Output resistance	R <sub>ON</sub>	-	0.6	3.0	Ω	DC/DC converter × 1mode
<b>1-1-1-3 LED Driver</b>						
Output current 1mA	I <sub>led1</sub>	0.8	1	1.2	mA	LED Terminal voltage=1V IREF resistor = 100kΩ
Output current 2mA	I <sub>led2</sub>	1.6	2	2.4	mA	
Output current 6.5mA	I <sub>led6.5</sub>	5.525	6.5	7.475	mA	
Output current 7.5mA	I <sub>led7.5</sub>	6.375	7.5	8.625	mA	
Output current 9mA	I <sub>led9</sub>	7.65	9	10.35	mA	
Output current 10mA	I <sub>led10</sub>	8.5	10	11.5	mA	
Output current 13mA	I <sub>led13</sub>	11.7	13	14.3	mA	
Output current 15mA	I <sub>led15</sub>	13.5	15	16.5	mA	
Output current 18mA	I <sub>led18</sub>	16.2	18	19.8	mA	
Output current 20mA	I <sub>led20</sub>	18	20	22	mA	
<b>1-1-1-4 General Purpose Output</b>						
Output L level	I <sub>gpo</sub>	-	-	0.3	V	I <sub>o</sub> =10mA

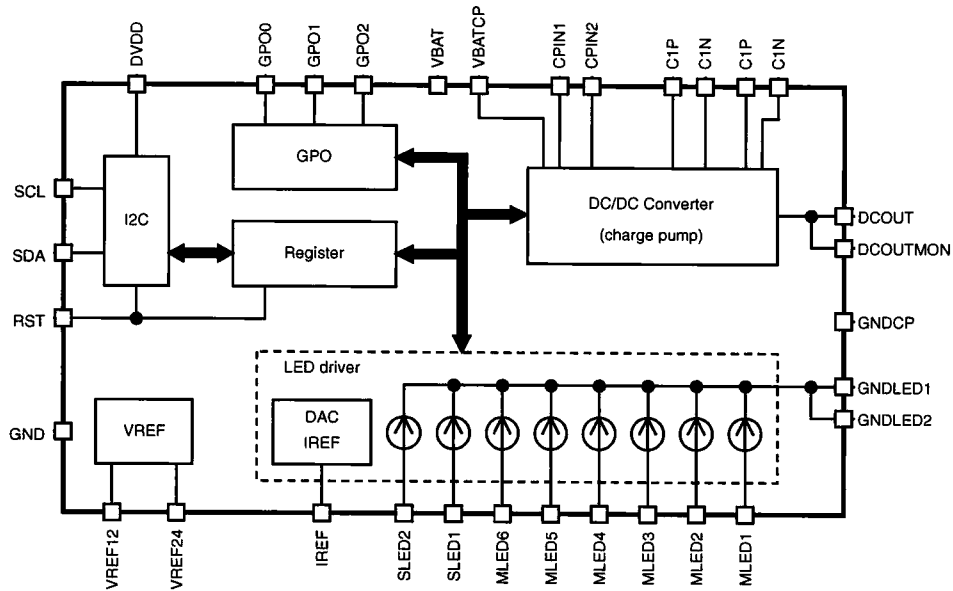
External dimensions



Terminals

PIN	PIN Name	PIN	PIN Name
D1	VBAT	C2	IREF
C1	DVDD	B2	MLED1
E4	RST	A2	MLED2
C5	SCL	B3	MLED3
D5	SDA	A3	MLED4
C6	VREF12	A4	MLED5
D6	VREF24	B4	MLED6
D3	GND	A5	SLED1
E6	VBATCP	B5	SLED2
E5	CPIN1	B1	GNDLED1
F2	CPIN2	B6	GNDLED2
F3	C1P	D2	GPO0
E2	C1N	D4	GPO1
F5	C2P	C4	GPO2
E3	C2N	A1	TEST1
F4	DCOUT	A6	TEST2
F6	DCOUTMON	F1	TEST3
E1	GNDCP	—	—

Block diagram



## ○Cautions on use

## (1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

## (2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

## (3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

## (4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

## (5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

## (6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

## (7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

## (8) Thermal shutdown circuit (TSD)

This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

## (9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

## (10) Other cautions on use

Please consult supplementary documents such as technical notebook, function manual and application design guide of this LSI.

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