

## NTE3094 Optoisolator Dual, High Speed, Open Collector NAND Gate

**Description:**

The NTE3094 consists of a pair of inverting optically coupled gates each with a GaAsP emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. Each circuit is temperature, current and voltage compensated.

This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0° to +70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt V<sub>CC</sub> applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 57ns.

**Features:**

- LSTTL/TTL Compatible: 5V Supply
- Ultra High Speed
- Low Input Current Required
- High Common Mode Rejection
- 3000V DC Withstand Test Voltage
- Typical Data Rate 10M/Bit(s)

**Absolute Maximum Ratings:** (T<sub>A</sub> = +25°C unless otherwise specified)

**Input Diode (Each Channel)**

Reverse Voltage, V <sub>R</sub> .....	5V
Forward Current, I <sub>F</sub>	
Average .....	15mA
Peak (≤ 1ms Duration) .....	30mA

**Output Transistor (Each Channel)**

Supply Voltage (1 Minute Maximum), V <sub>CC</sub> .....	7V
Output Voltage, V <sub>O</sub> .....	7V
Output Current, I <sub>O</sub> .....	16mA
Collector Power Dissipation, P <sub>D</sub> .....	60mW

**Total Device**

Operating Temperature Range, T <sub>opr</sub> .....	0° to +70°C
Storage Temperature Range, T <sub>stg</sub> .....	-55° to +125°C
Lead Temperature (During Soldering, 1.6mm below seating plane, 10sec Max), T <sub>L</sub> .....	+260°C

**Recommended Operating Conditions:**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Current, Low Level (Each Channel)	$I_{FL}$		0	–	250	$\mu\text{A}$
Input Current, High Level (Each Channel)	$I_{FH}$	Note 1	6.3	–	15	mA
Supply Voltage, Output	$V_{CC}$		4.5	–	5.5	V
Fan Out (TTL Load)	N		–	–	8	
Operating Temperature	$T_A$		0	–	70	$^{\circ}\text{C}$

Note 1. 6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

**Electrical Characteristics:** ( $T_A = 0^{\circ}$  to  $+70^{\circ}\text{C}$ , Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Output Current	$I_{OH}$	$V_{CC} = 5\text{V}$ , $V_O = 5.5\text{V}$ , $I_F = 250\mu\text{A}$ , Note 3	–	40	250	$\mu\text{A}$
Low Level Output Voltage	$V_{OL}$	$V_{CC} = 5.5\text{V}$ , $I_F = 5\text{mA}$ , $I_{OL(\text{sinking})} = 13\text{mA}$ , Note 3	–	0.4	0.6	V
High Level Supply Current	$I_{CCH}$	$V_{CC} = 5\text{V}$ , $I_F = 0$ , (Both Channels)	–	15	30	mA
Low Level Supply Current	$I_{CCL}$	$V_{CC} = 5\text{V}$ , $I_F = 10\text{mA}$ , (Both Channels)	–	27	36	mA
Input–Output Insulation Leakage Current	$I_{IO}$	Relative Humidity = 45%, $T_A = +25^{\circ}\text{C}$ , $t = 5\text{s}$ , $V_{IO} = 3000\text{V DC}$ , Note 4	–	–	1.0	$\mu\text{A}$
Resistance	$R_{IO}$	$V_{IO} = 500\text{V}$ , $T_A = +25^{\circ}\text{C}$ , Note 4	–	$10^{12}$	–	$\Omega$
Capacitance	$C_{IO}$	$f = 1\text{MHz}$ , $T_A = +25^{\circ}\text{C}$ , Note 4	–	0.6	–	pF
Input Forward Voltage	$V_F$	$I_F = 10\text{mA}$ , $T_A = +25^{\circ}\text{C}$ , Note 3, Note 5	–	1.5	1.75	V
Input Reverse Breakdown Voltage	$V_{(BR)R}$	$I_R = 10\mu\text{A}$ , $T_A = +25^{\circ}\text{C}$	5	–	–	V
Input Capacitance	$C_{IN}$	$V_F = 0$ , $f = 1\text{MHz}$ , Note 3	–	60	–	pF
Current Transfer Ratio	CTR	$I_F = 5\text{mA}$ , $R_L = 100\Omega$ , Note 6	–	700	–	%
Resistance (Input–Input)	$R_{II}$	$V_{II} = 500\text{V}$ , Note 7	–	$10^{11}$	–	$\Omega$
Capacitance (Input–Input)	$C_{II}$	$f = 1\text{MHz}$ , Note 7	–	0.27	–	pF

Note 2. All typicals at  $T_A = +25^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified.

Note 3. Each channel.

Note 4. Measured between Pin1, Pin2, Pin3 and Pin4 shorted together and Pin5, Pin6, Pin7 and Pin8 shorted together.

Note 5. At 10mA,  $V_F$  decreases with increasing temperature at the rate of  $1.6\text{mV}/^{\circ}\text{C}$ .

Note 6. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.

Note 7. Measured between Pin1 and Pin2 shorted together and Pin3 and Pin4 shorted together.

**Switching Characteristics:** ( $T_A = +25^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Propagation Delay Time	$t_{PLH}$	$I_F = 7.5\text{mA}$ , $R_L = 350\Omega$ , $C_L = 15\text{pF}$	Note 8	–	57	75	ns
	$t_{PHL}$		Note 9	–	45	75	ns
Output Rise Time (10% to 90%)	$t_r$	$I_F = 7.5\text{mA}$ , $R_L = 350\Omega$ , $C_L = 15\text{pF}$ , Note 3	–	25	–	ns	
Output Fall Time (90% to 10%)	$t_f$		–	35	–	ns	
Common Mode Transient Immunity	$CM_H$	$I_F = 0\text{mA}$ , $V_{O(\min)} = 2\text{V}$	$V_{CM} = 10\text{V}_{P-P}$ $R_L = 350\Omega$	–	500	–	$\text{V}/\mu\text{s}$
	$CM_L$	$I_F = 7.5\text{mA}$ , $V_{O(\max)} = 0.8\text{V}$		–	–500	–	$\text{V}/\mu\text{s}$

Note 3. Each channel.

Note 8. The  $t_{PLH}$  propagation delay is measured from the 3.75mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.

Note 9. The  $t_{PHL}$  propagation delay is measured from the 3.75mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.

Note 10. Common mode transient immunity in Logic High level is the maximum tolerable (positive)  $dv_{cm}/dt$  on the leading edge of the common mode pulse ( $V_{CM}$ ) to assure that the output will remain in a Logic High state (i.e.  $V_O 2.0\text{V}$ ). Common mode transient immunity in Logic Low level is the maximum tolerable (negative)  $dc_{cm}/dt$  on the trailing edge of the common mode pulse signal ( $V_{CM}$ ) to assure that the output will remain in a Logic Low state (i.e.  $V_O 0.8\text{V}$ ).

