

Features

- EE Programmable 262,144 x 1-, 524,288 x 1-, 1,048,576 x 1-, 2,097,152 x 1-, and 4,194,304 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)
- Available as a 3.3V ($\pm 10\%$) Commercial and Industrial Version
- Simple Interface to SRAM FPGAs
- Pin Compatible with Xilinx[®] XC17SXXXA and XC17SXXXXL PROMs
- Compatible with Xilinx Spartan[®]-II, Spartan-IIE and Spartan XL FPGAs in Master Serial Mode
- Very Low-power CMOS EEPROM Process
- Available in 8-lead PDIP, 8-lead SOIC, 20-lead SOIC and 44-lead TQFP Packages for a Specific Density
- Low-power Standby Mode
- High-reliability
 - Endurance: Minimum 10 Write Cycles
 - Data Retention: 20 Years at 85°C

Description

The AT17N series FPGA Configuration EEPROM (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17N series device is packaged in the 8-lead PDIP, 8-lead SOIC, 20-lead SOIC and 44-lead TQFP, see Table 1. The AT17N series Configurators uses a simple serial-access procedure to configure one or more FPGA devices.

The AT17N series configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable and factory programming.

Table 1. AT17N Series Packages

| Package | AT17N256 | AT17N512/ AT17N010 | AT17N002 | AT17N040 |
|--------------|----------|-----------------------|----------|----------|
| 8-lead PDIP | Yes | Yes | – | – |
| 8-lead SOIC | Yes | – | – | – |
| 20-lead SOIC | Yes | Yes | Yes | – |
| 44-lead TQFP | – | – | Yes | Yes |



FPGA Configuration Memory

AT17N256
AT17N512
AT17N010
AT17N002
AT17N040

3.3V System Support

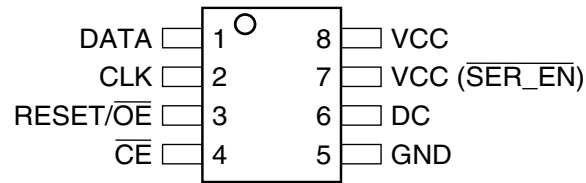
Not Recommended For New Design

AT17N256 replaced by AT17LV256
AT17N512 replaced by AT17LV512
AT17N010 replaced by AT17LV010
AT17N002 replaced by AT17LV002
AT17N040 replaced by AT17LV040

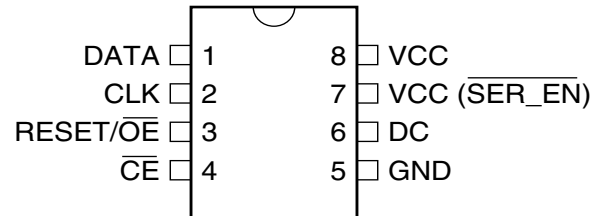


Pin Configuration

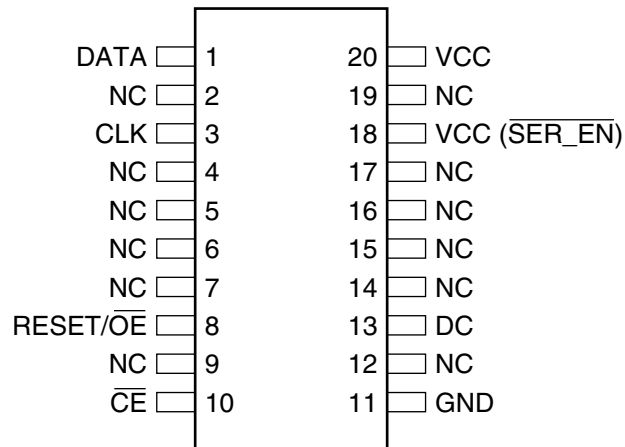
8-lead SOIC



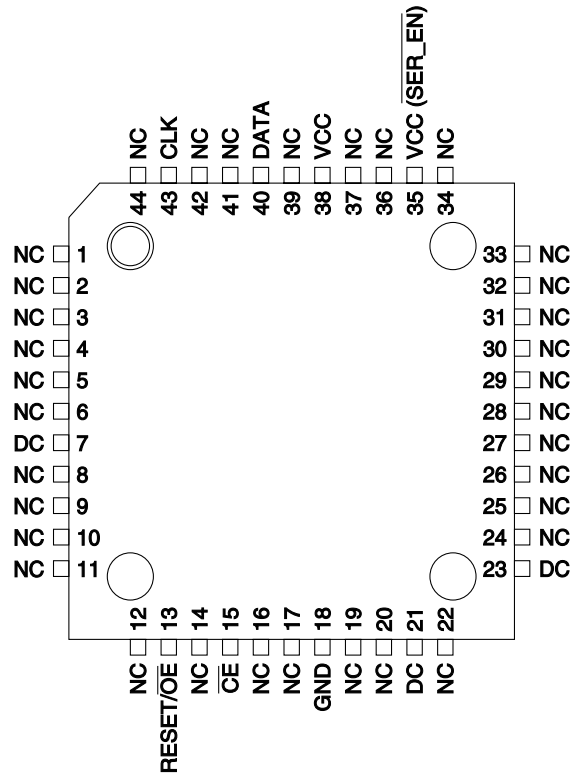
8-lead PDIP



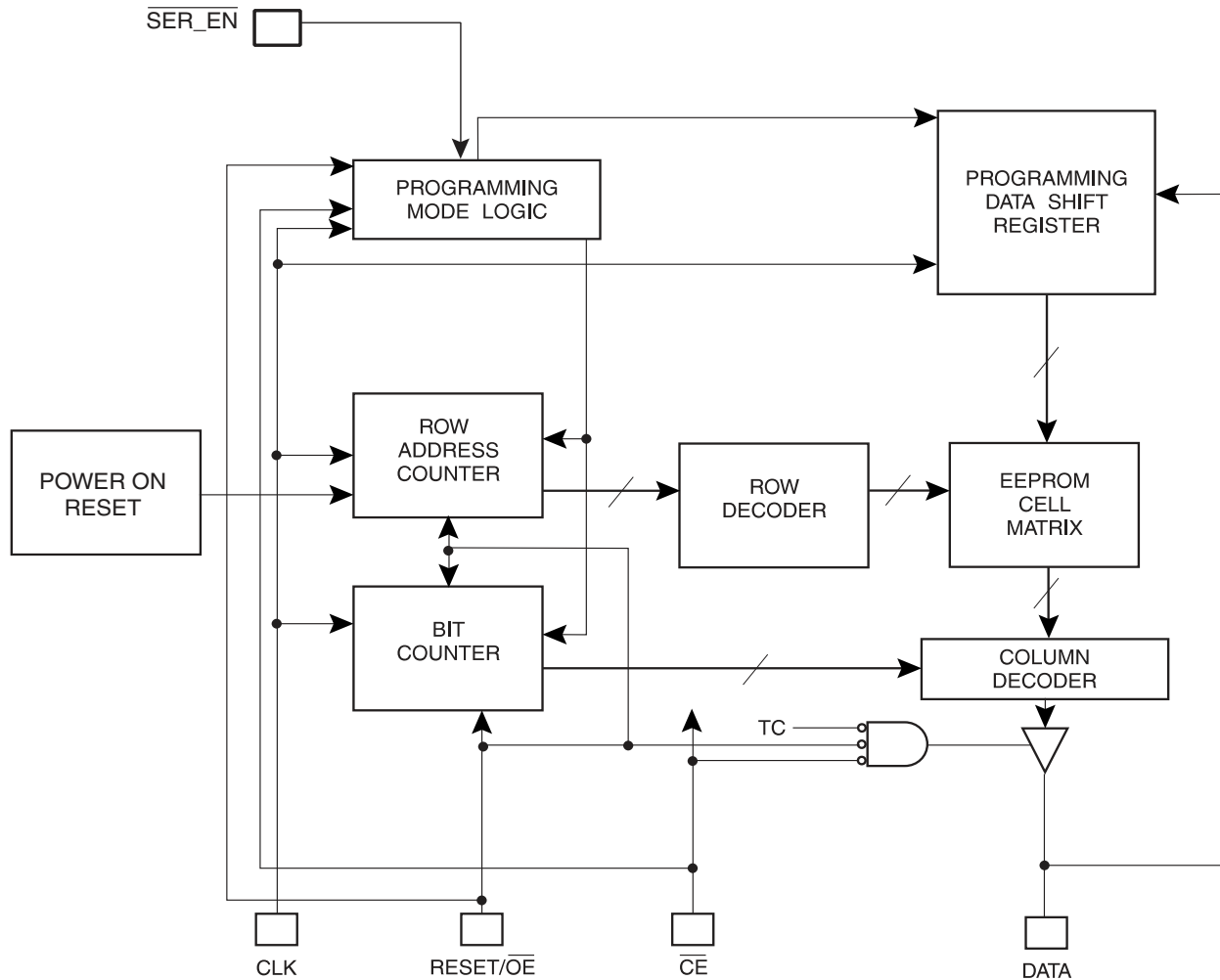
20-lead SOIC



44 TQFP



Block Diagram



Device Description

The control signals for the configuration EEPROM (\overline{CE} , $\overline{RESET/OE}$ and $CCLK$) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM $\overline{RESET/OE}$ and \overline{CE} pins control the tri-state buffer on the DATA output pin and enable the address counter. When $\overline{RESET/OE}$ is driven High, the configuration EEPROM resets its address counter and tri-states its DATA pin. The \overline{CE} pin also controls the output of the AT17N series configurator. If \overline{CE} is held High after the $\overline{RESET/OE}$ reset pulse, the counter is disabled and the DATA output pin is tri-stated. When \overline{OE} is subsequently driven Low, the counter and the DATA output pin are enabled. When $\overline{RESET/OE}$ is driven High again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of \overline{CE} . Upon power-up, the address counter is automatically reset.

Pin Description

| Name | I/O | AT17N256 | | AT17N512/ AT17N010 | | AT17N002 | | AT17N040 |
|------------------------------------|-----|-------------------|------------|-----------------------|------------|------------|------------|------------|
| | | 8 DIP/ SOIC | 20 SOIC | 8 DIP | 20 SOIC | 20 SOIC | 44 TQFP | 44 TQFP |
| DATA | I/O | 1 | 1 | 1 | 1 | 1 | 40 | 40 |
| CLK | I | 2 | 3 | 2 | 3 | 3 | 43 | 43 |
| RESET/ $\overline{\text{OE}}$ | I | 3 | 8 | 3 | 8 | 8 | 13 | 13 |
| $\overline{\text{CE}}$ | I | 4 | 10 | 4 | 10 | 10 | 15 | 15 |
| GND | | 5 | 11 | 5 | 11 | 11 | 18 | 18 |
| DC | O | 6 | 13 | 6 | 13 | 13 | 21 | 21 |
| DC | O | – | – | – | – | – | 23 | 23 |
| VCC($\overline{\text{SER_EN}}$) | I | 7 | 18 | 7 | 18 | 18 | 35 | 35 |
| V _{CC} | | 8 | 20 | 8 | 20 | 20 | 38 | 38 |

DATA

Three-state DATA output for configuration. Open-collector bi-directional pin for programming.

CLK

Clock input. Used to increment the internal address and bit counter for reading and programming.

RESET/ $\overline{\text{OE}}$

Output Enable (active High) and RESET (active Low) when $\overline{\text{SER_EN}}$ is High. A Low level on RESET/OE resets both the address and bit counters. A High level (with $\overline{\text{CE}}$ Low) enables the data output driver. The logic polarity of this input is programmable as either RESET/ $\overline{\text{OE}}$ or $\overline{\text{RESET/OE}}$. For most applications, RESET should be programmed active Low. This document describes the pin as $\overline{\text{RESET/OE}}$.

$\overline{\text{CE}}$

Chip Enable input (active Low). A Low level (with OE High) allows CLK to increment the address counter and enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will *not* enable/disable the device in the Two-Wire Serial Programming mode ($\overline{\text{SER_EN}}$ Low).

GND

Ground pin. A 0.2 μF decoupling capacitor between V_{CC} and GND is recommended.

VCC($\overline{\text{SER_EN}}$)

Serial enable must be held High during FPGA loading operations. Bringing $\overline{\text{SER_EN}}$ Low enables the Two-Wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER_EN}}$ should be tied to V_{CC}.

V_{CC}

3.3V ($\pm 10\%$) Commercial and Industrial power supply pin.

NC

NC pins are No Connect pins, which are not internally bonded out to the die.

DC

DC pins are No Connect pins internally connected to the die. It is not recommended to connect these pins to any external signal.



FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17N Serial Configuration EEPROM has been designed for compatibility with the Master Serial mode.

This document discusses the master serial mode configuration of Atmel AT17N series configuration memories, pin compatible with Spartan-II, Spartan-IIe and Spartan XL OTP PROMs.

Control of Configuration

Most connections between the FPGA device and the AT17N Serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17N series configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17N series configurator.
- $\overline{\text{SER_EN}}$ must be connected to V_{CC} (except during ISP).
- The $\overline{\text{CE}}$ and $\text{OE}/\overline{\text{Reset}}$ are driven by the FPGA to enable output data buffer of the EEPROM.

Programming Mode

The programming mode is entered by bringing $\overline{\text{SER_EN}}$ Low. In this mode the chip can be programmed by the Two-Wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip.

Standby Mode

The AT17N series configurators enter a low-power standby mode whenever $\overline{\text{CE}}$ is asserted High. In this mode, the AT17N256 configurator consumes less than 50 μA of current at 3.3V (100 μA for the AT17N512/010 and 200 μA for the AT17N002/040).

Absolute Maximum Ratings*

| | |
|---|--------------------------|
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -0.1V to $V_{CC} + 0.5V$ |
| Supply Voltage (V_{CC}) | 3.0V to +3.6V |
| Maximum Soldering Temp. (10 sec. @ 1/16 in.)..... | 260°C |
| ESD ($R_{ZAP} = 1.5K, C_{ZAP} = 100 \text{ pF}$)..... | 2000V |

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Conditions

| Symbol | Description | | 3.3V | | Units |
|----------|-------------|--|------|-----|-------|
| | | | Min | Max | |
| V_{CC} | Commercial | Supply voltage relative to GND -0°C to +70°C | 3.0 | 3.6 | V |
| | Industrial | Supply voltage relative to GND -40°C to +85°C | 3.0 | 3.6 | V |





DC Characteristics

$$V_{CC} = 3.3V \pm 10\%$$

| Symbol | Description | AT17N256 | | AT17N512/ AT17N010 | | AT17N002/ AT17N040 | | Units | | |
|------------------|---|------------|-----------------|-----------------------|-----------------|-----------------------|-----------------|-------|-----|-----|
| | | Min | Max | Min | Max | Min | Max | | | |
| V _{IH} | High-level Input Voltage | 2.0 | V _{CC} | 2.0 | V _{CC} | 2.0 | V _{CC} | V | | |
| V _{IL} | Low-level Input Voltage | 0 | 0.8 | 0 | 0.8 | 0 | 0.8 | V | | |
| V _{OH} | High-level Output Voltage (I _{OH} = -2.5 mA) | Commercial | 2.4 | 2.4 | 2.4 | 2.4 | 2.4 | V | | |
| V _{OL} | Low-level Output Voltage (I _{OL} = +3 mA) | | 0.4 | | | | | | 0.4 | 0.4 |
| V _{OH} | High-level Output Voltage (I _{OH} = -2 mA) | Industrial | 2.4 | 2.4 | 2.4 | 2.4 | 2.4 | V | | |
| V _{OL} | Low-level Output Voltage (I _{OL} = +3 mA) | | 0.4 | | | | | | 0.4 | 0.4 |
| I _{CCA} | Supply Current, Active Mode | | 5 | | 5 | | 5 | mA | | |
| I _L | Input or Output Leakage Current (V _{IN} = V _{CC} or GND) | | -10 | | 10 | | -10 | | 10 | μA |
| I _{CCS} | Supply Current, Standby Mode | Commercial | | | 50 | | 100 | | 150 | μA |
| | | Industrial | | | 100 | | 100 | | 150 | μA |

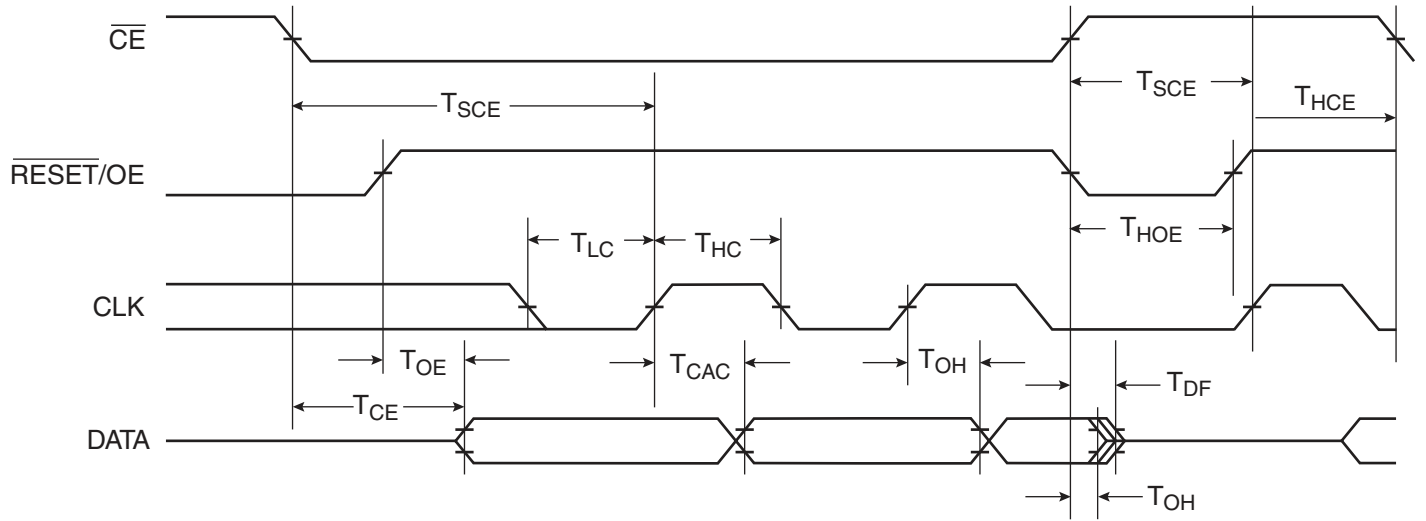
AC Characteristics

$$V_{CC} = 3.3V \pm 10\%$$

| Symbol | Description | AT17N256 | | | | AT17N512/010/002/040 | | | | Units |
|---------------------------------|--|------------|-----|------------|-----|----------------------|-----|------------|-----|-------|
| | | Commercial | | Industrial | | Commercial | | Industrial | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| T _{OE} ⁽¹⁾ | OE to Data Delay | | 50 | | 55 | | 50 | | 55 | ns |
| T _{CE} ⁽¹⁾ | \overline{CE} to Data Delay | | 60 | | 60 | | 55 | | 60 | ns |
| T _{CAC} ⁽¹⁾ | CLK to Data Delay | | 75 | | 80 | | 55 | | 60 | ns |
| T _{OH} | Data Hold from \overline{CE} , OE, or CLK | 0 | | 0 | | 0 | | 0 | | ns |
| T _{DF} ⁽²⁾ | \overline{CE} or OE to Data Float Delay | | 55 | | 55 | | 50 | | 50 | ns |
| T _{LC} | CLK Low Time | 25 | | 25 | | 25 | | 25 | | ns |
| T _{HC} | CLK High Time | 25 | | 25 | | 25 | | 25 | | ns |
| T _{SCE} | \overline{CE} Setup Time to CLK (to guarantee proper counting) | 35 | | 60 | | 30 | | 35 | | ns |
| T _{HCE} | \overline{CE} Hold Time from CLK (to guarantee proper counting) | 0 | | 0 | | 0 | | 0 | | ns |
| T _{HOE} | OE High Time (guarantees counter is reset) | 25 | | 25 | | 25 | | 25 | | ns |
| F _{MAX} | Maximum Clock Frequency | | 10 | | 10 | | 15 | | 10 | MHz |

- Notes: 1. AC test lead = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

AC Characteristics

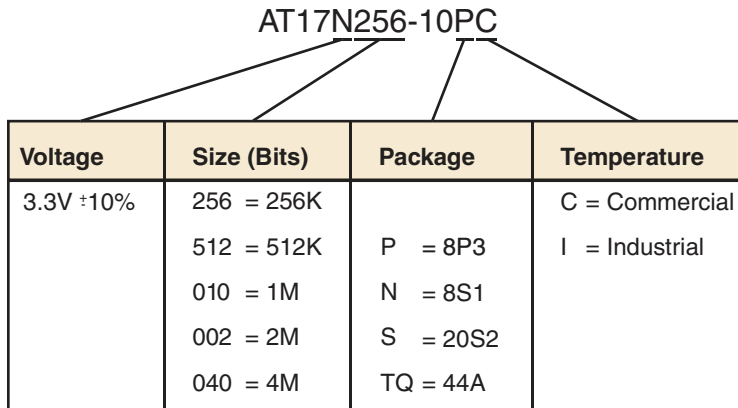


Thermal Resistance Coefficients⁽¹⁾

| Package Type | | | AT17N256 | AT17N512/ AT17N010 | AT17N002 | AT17N040 |
|--------------|--|--|----------|-----------------------|----------|----------|
| 8P3 | Plastic Dual Inline Package (PDIP) | θ_{JC} [$^{\circ}\text{C}/\text{W}$] | 37 | 37 | – | – |
| | | θ_{JA} [$^{\circ}\text{C}/\text{W}$] ⁽²⁾ | 107 | 107 | – | – |
| 8S1 | Plastic Gull Wing Small Outline (SOIC) | θ_{JC} [$^{\circ}\text{C}/\text{W}$] | 45 | – | – | – |
| | | θ_{JA} [$^{\circ}\text{C}/\text{W}$] ⁽²⁾ | 150 | – | – | – |
| 20S2 | Plastic Gull Wing Small Outline (SOIC) | θ_{JC} [$^{\circ}\text{C}/\text{W}$] | | | | – |
| | | θ_{JA} [$^{\circ}\text{C}/\text{W}$] ⁽²⁾ | | | | – |
| 44A | Thin Plastic Quad Flat Package (TQFP) | θ_{JC} [$^{\circ}\text{C}/\text{W}$] | – | – | 17 | 17 |
| | | θ_{JA} [$^{\circ}\text{C}/\text{W}$] ⁽²⁾ | – | – | 62 | 62 |

- Notes: 1. For more information refer to the “Thermal Characteristics of Atmel’s Packages”, available on the Atmel web site.
 2. Airflow = 0 ft/min.

Figure 1. Ordering Code



| Package Type | |
|--------------|--|
| 8P3 | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 8S1 | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 20S2 | 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 44A | 44-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP) |



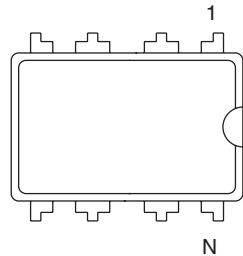
Ordering Information

| Memory Size | Ordering Code | Package | Operation Range |
|-------------|----------------|---------|-------------------------------|
| 256-Kbit | AT17N256-10PC | 8P3 | Commercial (0°C to 70°C) |
| | AT17N256-10NC | 8S1 | |
| | AT17N256-10SC | 20S2 | |
| | AT17N256-10PI | 8P3 | Industrial (-40°C to 85°C) |
| | AT17N256-10NI | 8S1 | |
| | AT17N256-10SI | 20S2 | |
| 512-Kbit | AT17N512-10SC | 20S2 | Commercial (0°C to 70°C) |
| | AT17N512-10SI | 20S2 | Industrial (-40°C to 85°C) |
| 1-Mbit | AT17N010-10SC | 20S2 | Commercial (0°C to 70°C) |
| | AT17N010-10SI | 20S2 | Industrial (-40°C to 85°C) |
| 2-Mbit | AT17N002-10SC | 20S2 | Commercial (0°C to 70°C) |
| | AT17N002-10TQC | 44A | |
| | AT17N002-10SI | 20S2 | Industrial (-40°C to 85°C) |
| | AT17N002-10TQI | 44A | |
| 4-Mbit | AT17N040-10TQC | 44A | Commercial (0°C to 70°C) |
| | AT17N040-10TQI | 44A | Industrial (-40°C to 85°C) |

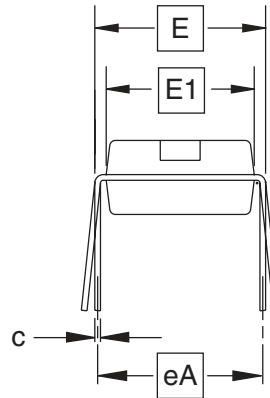
Notes: 1. For the -10CC and -10CI packages, customers may migrate to AT17LVXXX-10CU.

Packaging Information

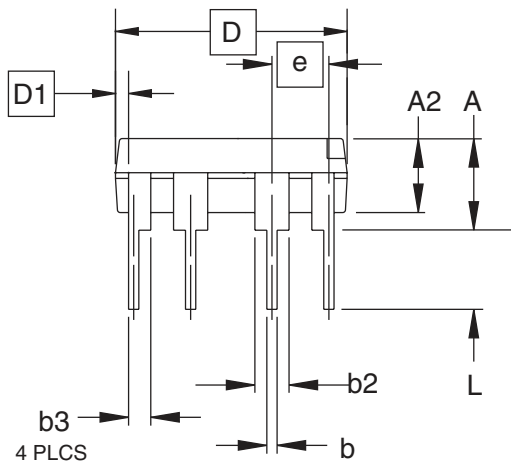
8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-------|-------|------|
| A | | | 0.210 | 2 |
| A2 | 0.115 | 0.130 | 0.195 | |
| b | 0.014 | 0.018 | 0.022 | 5 |
| b2 | 0.045 | 0.060 | 0.070 | 6 |
| b3 | 0.030 | 0.039 | 0.045 | 6 |
| c | 0.008 | 0.010 | 0.014 | |
| D | 0.355 | 0.365 | 0.400 | 3 |
| D1 | 0.005 | | | 3 |
| E | 0.300 | 0.310 | 0.325 | 4 |
| E1 | 0.240 | 0.250 | 0.280 | 3 |
| e | 0.100 BSC | | | |
| eA | 0.300 BSC | | | 4 |
| L | 0.115 | 0.130 | 0.150 | 2 |

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
 2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
 3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
 4. E and eA measured with the leads constrained to be perpendicular to datum.
 5. Pointed or rounded lead tips are preferred to ease insertion.
 6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02



2325 Orchard Parkway
San Jose, CA 95131

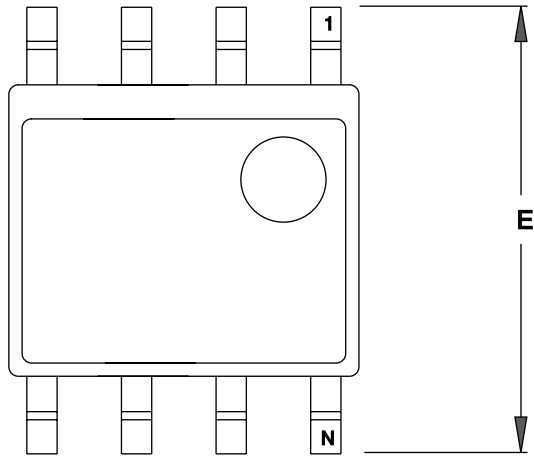
TITLE
8P3, 8-lead, 0.300" Wide Body, Plastic Dual
In-line Package (PDIP)

DRAWING NO.
8P3

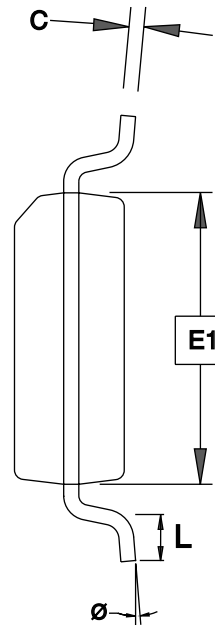
REV.
B



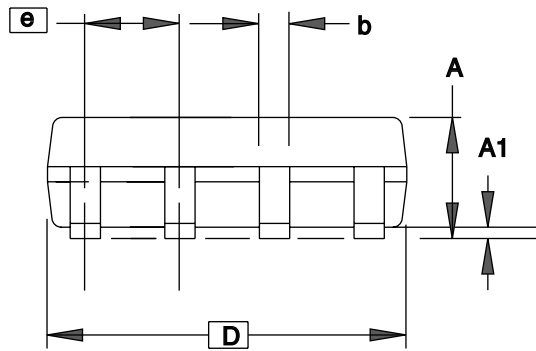
8S1 – SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-----|------|------|
| A | 1.35 | – | 1.75 | |
| A1 | 0.10 | – | 0.25 | |
| b | 0.31 | – | 0.51 | |
| C | 0.17 | – | 0.25 | |
| D | 4.80 | – | 5.05 | |
| E1 | 3.81 | – | 3.99 | |
| E | 5.79 | – | 6.20 | |
| e | 1.27 BSC | | | |
| L | 0.40 | – | 1.27 | |
| θ | 0° | – | 8° | |

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

3/17/05



1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906

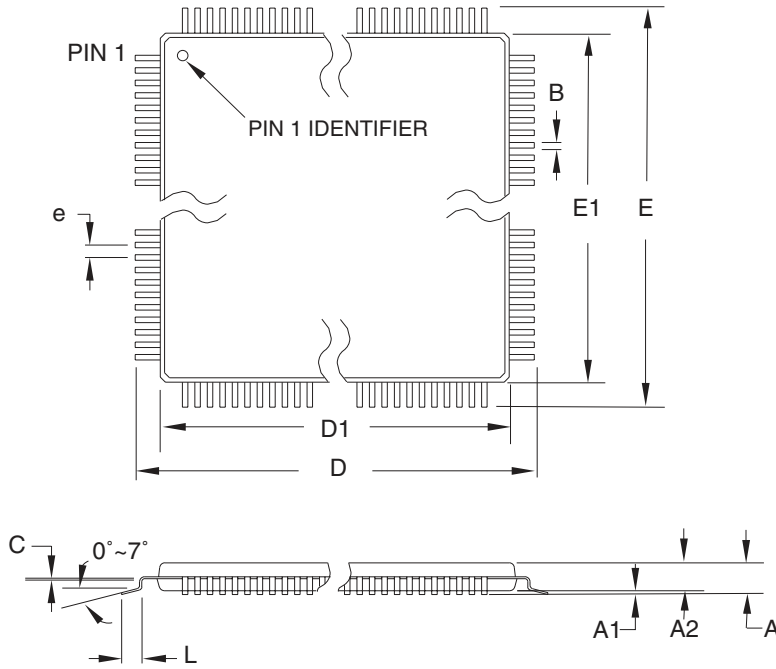
TITLE
8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing
Small Outline (JEDEC SOIC)

DRAWING NO.
8S1

REV.
C

20S2 – SOIC

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-------|-------|--------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 11.75 | 12.00 | 12.25 | |
| D1 | 9.90 | 10.00 | 10.10 | Note 2 |
| E | 11.75 | 12.00 | 12.25 | |
| E1 | 9.90 | 10.00 | 10.10 | Note 2 |
| B | 0.30 | – | 0.45 | |
| C | 0.09 | – | 0.20 | |
| L | 0.45 | – | 0.75 | |
| e | 0.80 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

| | | | |
|--|--|--------------------|-------------|
| 2325 Orchard Parkway San Jose, CA 95131 | TITLE 44A , 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | DRAWING NO. | REV. |
| | | 44A | B |

Revision History

| Revision Level – Release Date | History |
|-------------------------------|--|
| B – March 2006 | Added last-time buy for AT17NXXX-10CC and AT17NXXX-10CI. |
| C – August 2007 | Removed 8CN4 8-lead LAP package. |



Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
configurator@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© Atmel Corporation 2007. All rights reserved. Atmel®, logo and combinations thereof, Everywhere You Are® and others are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. FLEX™ is the trademark of Altera Corporation; ORCA™ is the trademark of Lattice Semiconductors; SPARTAN® and Virtex® are the registered trademarks of Xilinx, Inc.; XC3000™, XC4000™ and XC5200™ are the trademarks of Xilinx, Inc.; APEX™ is the trademark of MIPS Technologies; Other terms and product names may be the trademarks of others.