To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS

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DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD3739

5000 PIXELS CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD3739 is a CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The μPD3739 is a 2-output type CCD sensor with 2 rows of high-speed charge transfer register, which transfers the photo signal electrons of 5000 pixels separately in odd and even pixels. It is suitable for 400 dpi/A3 high-speed digital copiers, OCRs and high-end business facsimiles.

FEATURES

- Valid photocell : 5000 pixels
- Photocell's pitch : 7 μm
- High sensitivity : 9.0 V/lx•s TYP. (Light source: Daylight color fluorescent lamp)
- Low image lag : 1 % MAX.
- Peak response wavelength : 550 nm (green)
- Resolution : 16 dot/mm (400 dpi) A3 (297 × 420 mm) size (shorter side)
- Data rate : 40 MHz MAX. (20 MHz/1 output)
- Output type : 2 outputs out of phase (2 outputs in phase also supported)
- Power supply : +12 V
- Drive clock level : CMOS output under 5 V operation
- On-chip circuit : Automatic φR level adjuster

ORDERING INFORMATION

	Part Number	Package
<R>	μPD3739D-A	CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

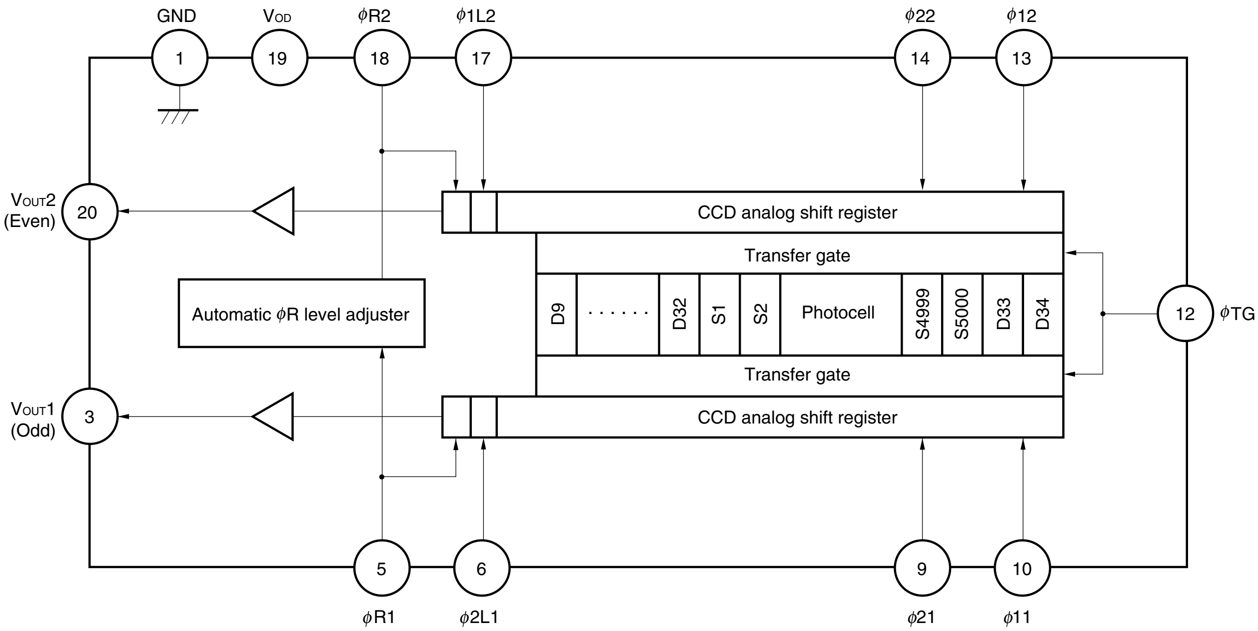
Remark The μPD3739D-A is a lead-free product.

Document No. S12744EJ4V0DS00 (4th edition)
Date Published October 2006 NS CP (K)
Printed in Japan

The mark " <R>" shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

BLOCK DIAGRAM



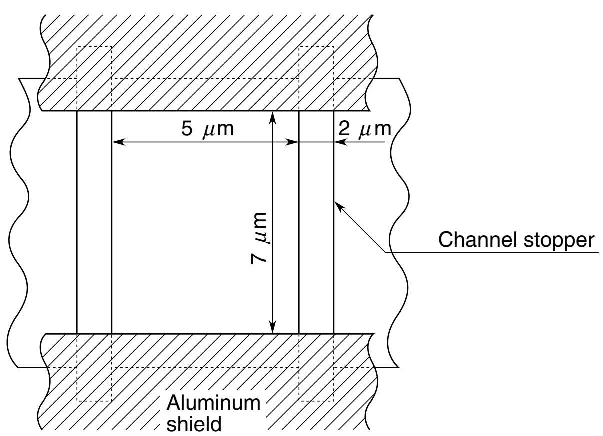
PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400 mil))
μPD3739D-A

Ground	1	GND	NC	22	No connection
No connection	2	NC	NC	21	No connection
Output signal 1 (Odd)	3	$V_{OUT}1$	$V_{OUT}2$	20	Output signal 2 (Even)
No connection	4	NC	V_{OD}	19	Output drain voltage
Reset gate clock 1	5	ϕR1	ϕR2	18	Reset gate clock 2
Last stage shift register clock 2	6	ϕ2L1	ϕ1L2	17	Last stage shift register clock 1
No connection	7	NC	NC	16	No connection
No connection	8	NC	NC	15	No connection
Shift register clock 2	9	ϕ21	ϕ22	14	Shift register clock 2
Shift register clock 1	10	ϕ11	ϕ12	13	Shift register clock 1
No connection	11	NC	ϕTG	12	Transfer gate clock

Caution　Connect the No connection pins (NC) to GND.

PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$	–0.3 to +15	V
Reset gate clock voltage	$V_{\phi R1}$, $V_{\phi R2}$	–0.3 to +15	V
Transfer gate clock voltage	$V_{\phi TG}$	–0.3 to +15	V
Operating ambient temperature Note	T_A	–25 to +55	°C
Storage temperature	T_{stg}	–40 to +100	°C

Note Use at the condition without dew condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = –25 to +55°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD}		11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi 1H}$, $V_{\phi 2H}$		4.5	5.0	5.5	V
Shift register clock low level	$V_{\phi 1L}$, $V_{\phi 2L}$		–0.3	0	+0.5	V
Reset gate clock high level	$V_{\phi R1H}$, $V_{\phi R2H}$	**Note**	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi R1L}$, $V_{\phi R2L}$	**Note**	–0.3	0	+0.5	V
Capacitance of reset gate clock pin external capacitor	$C_{EXT\phi R}$	Non-polar type	800	1000	1200	pF
Transfer gate clock high level	$V_{\phi TGH}$		4.5	5.0	5.5	V
Transfer gate clock low level	$V_{\phi TGL}$		–0.3	0	+0.5	V
Data rate	$2f_{\phi R1}$, $2f_{\phi R2}$		0.5	2	40	MHz

Note Input the reset gate clocks 1 and 2 (φR1, φR2) to pins 5 and 18, respectively, via an input resistor and a capacitor. Use of a capacitor is indispensable. Refer to **APPLICATION CIRCUIT EXAMPLE** for the connection method. The reset gate clock high level and low level at the IC pins (after passing through the external capacitor) varies according to the IC, due to the on-chip automatic φR level adjuster. The recommended operating conditions of reset gate clocks 1, 2 (φR1, φR2) in the table above are for signals applied to the external capacitor.

Remark φ1 in the above tables represents φ11, φ12 and φ1L2. φ2 represents φ21, φ22 and φ2L1.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = 12 V, $f_{\phi 1}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms
light source: 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm), input signal clock = 5 V_{p-p})

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{sat}		1.0	1.5	—	V
Saturation exposure	SE	Daylight color fluorescent lamp	—	0.17	—	lx•s
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV	—	4	10	%
Average dark signal	ADS	Light shielding	—	0.3	3.0	mV
Dark signal non-uniformity	DSNU	Light shielding	0	4.0	6.0	mV
Power consumption	P_W		—	200	400	mW
Output impedance	Z_O		—	0.2	0.5	kΩ
Response	R_F	Daylight color fluorescent lamp	7.2	9.0	10.8	V/lx•s
Response peak			—	550	—	nm
Image lag	IL	V_{OUT} = 1 V	—	0.3	1.0	%
Offset level Note 1	V_{OS}		2.0	3.5	5.0	V
Output fall delay time Note 2	t_d	V_{OUT} = 1 V	—	20	—	ns
Register imbalance	RI	V_{OUT} = 500 mV	0	—	4.0	%
Total transfer efficiency	TTE	V_{OUT} = 500 mV, data rate = 40 MHz	92	98	—	%
Dynamic range	DR1	V_{sat}/DSNU	—	375	—	times
	DR2	V_{sat}/σ	—	2143	—	times
Reset feed-through noise Note 1	RFTN	Light shielding	0	400	600	mV
Random noise	σ	Light shielding	—	0.7	—	mV

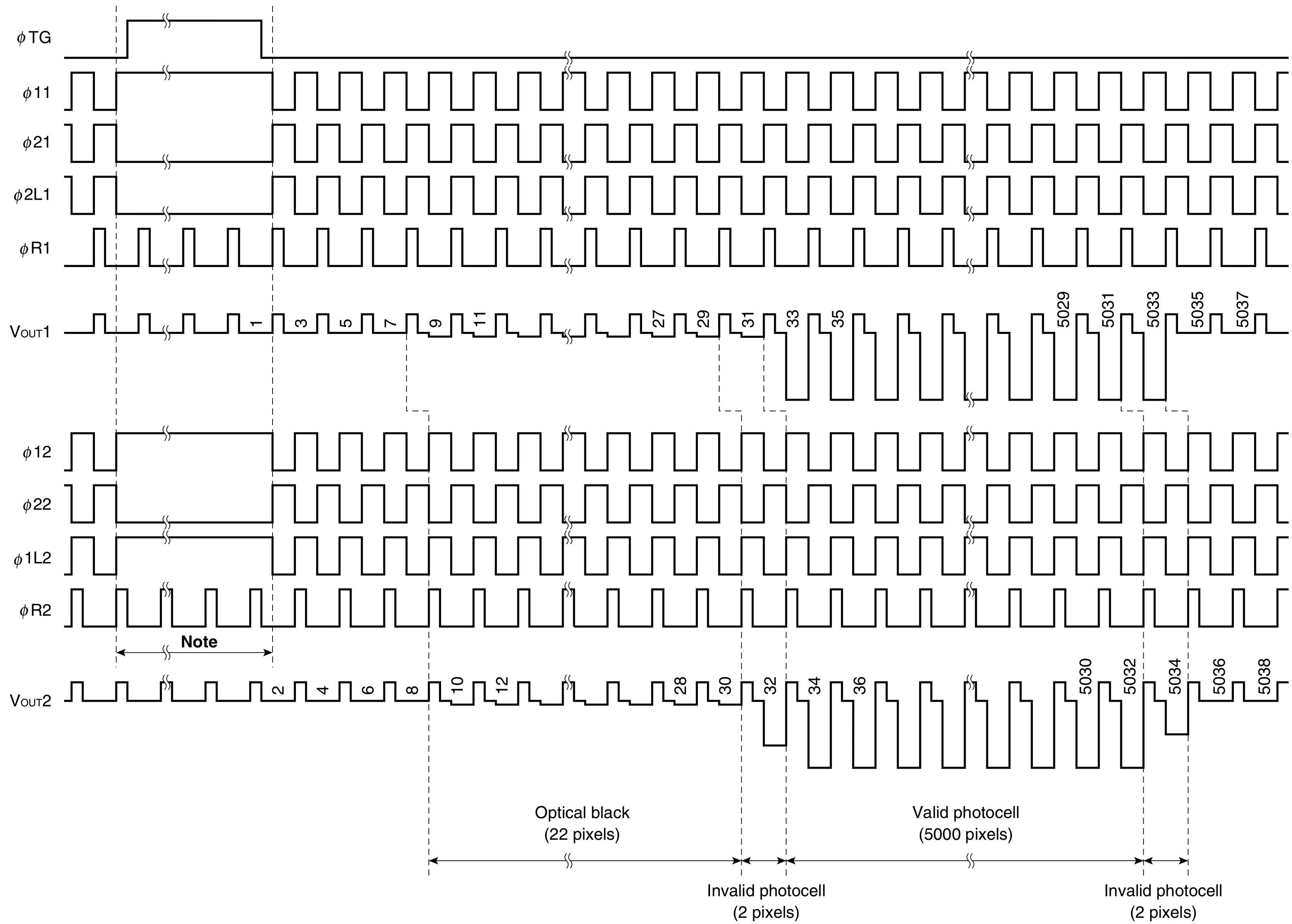
Notes 1. Refer to **TIMING CHART 2, 5**.

2. Typical value when the respective fall times of ϕ1L2 and ϕ2L1 are t11’, t41’ and t2’, t32’ (refer to **TIMING CHART 2, 5**). Note that $V_{OUT}1$ and $V_{OUT}2$ are the outputs of the two steps of emitter-follower shown in **APPLICATION CIRCUIT EXAMPLE**.

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

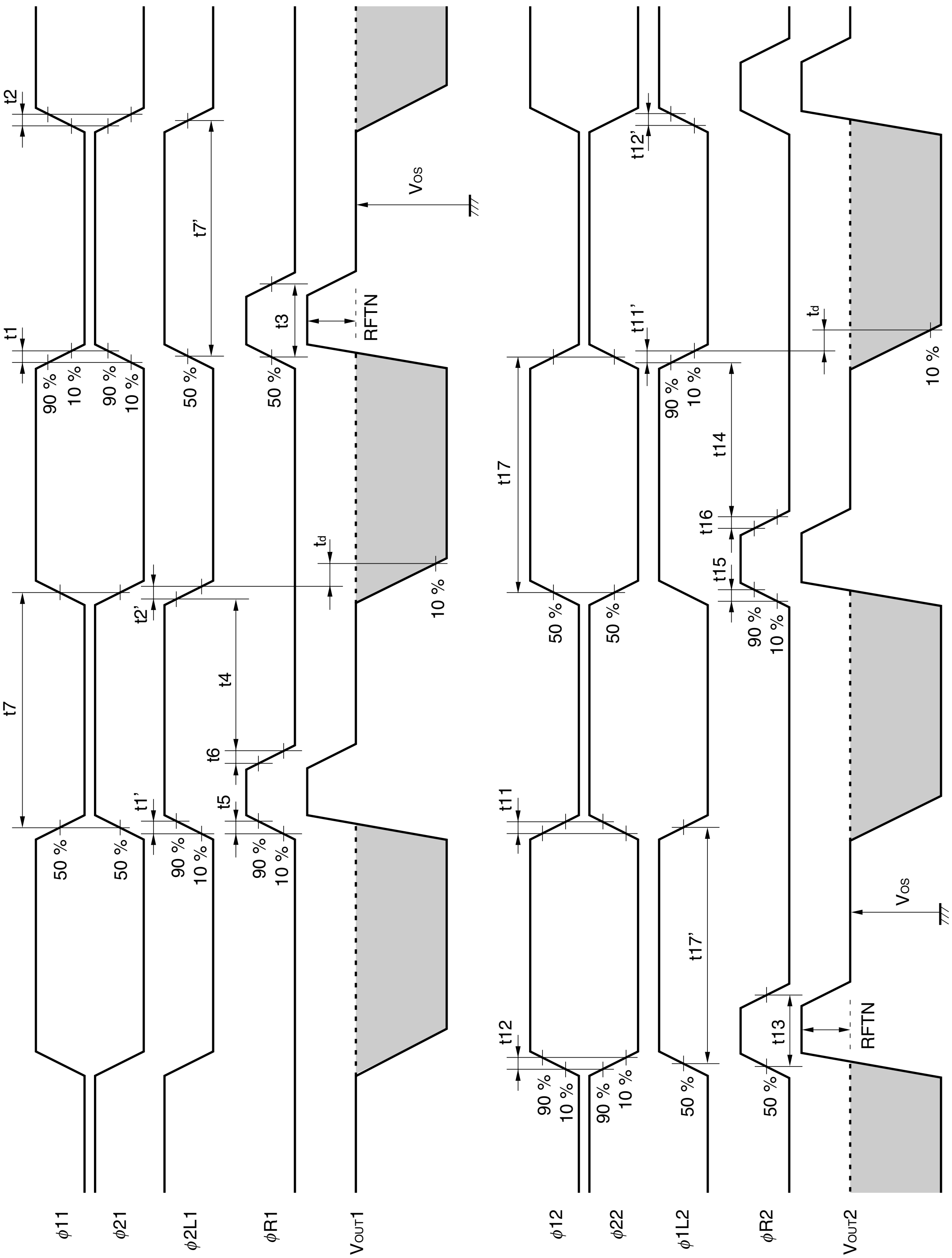
Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ11	10	250	350	500	pF
		ϕ12	13	250	350	500	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ21	9	250	350	500	pF
		ϕ22	14	250	350	500	pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	ϕ1L2	17	40	50	100	pF
		ϕ2L1	6	40	50	100	pF
Reset gate clock pin capacitance	$C_{\phi R}$	ϕR1	5	8	10	15	pF
		ϕR2	18	8	10	15	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG	12	100	150	200	pF

TIMING CHART 1 (Out of phase operation)

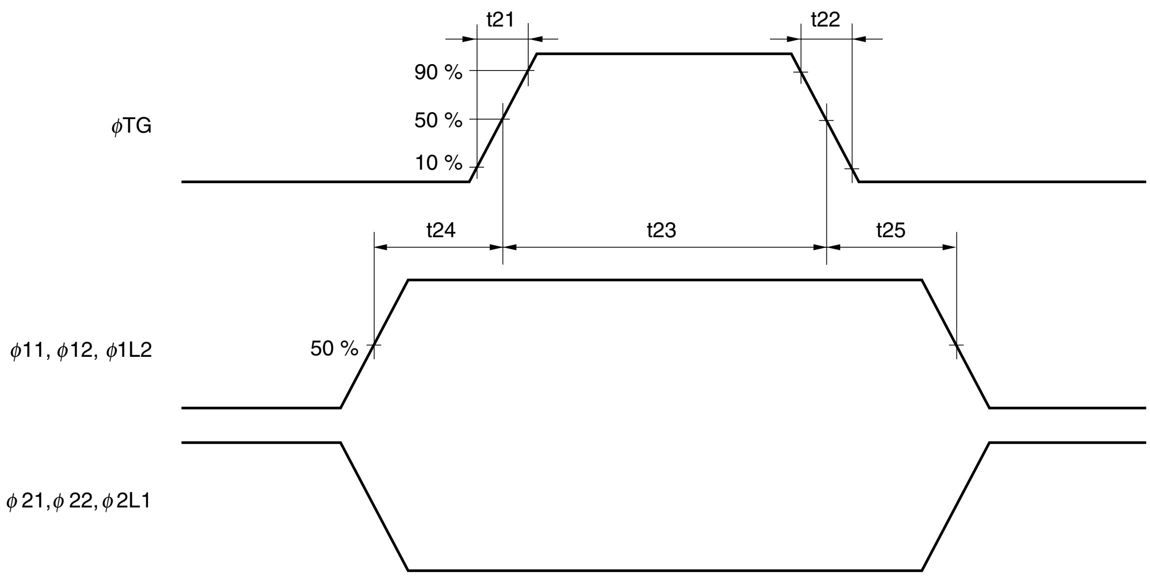


Note Input the ϕR1 and ϕR2 pulses continuously during this period, too.

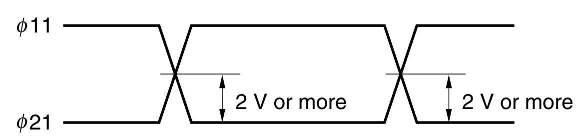
TIMING CHART 2 (Out of phase operation)



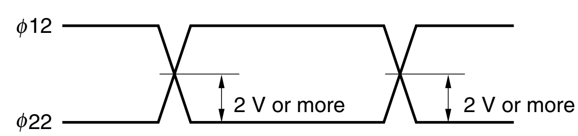
TIMING CHART 3 (Out of phase operation)



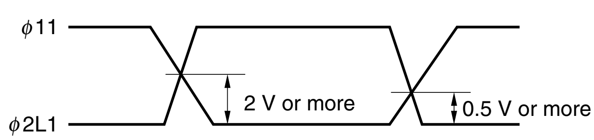
φ11, φ21 cross points



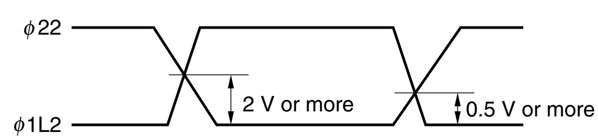
φ12, φ22 cross points



φ11, φ2L1 cross points



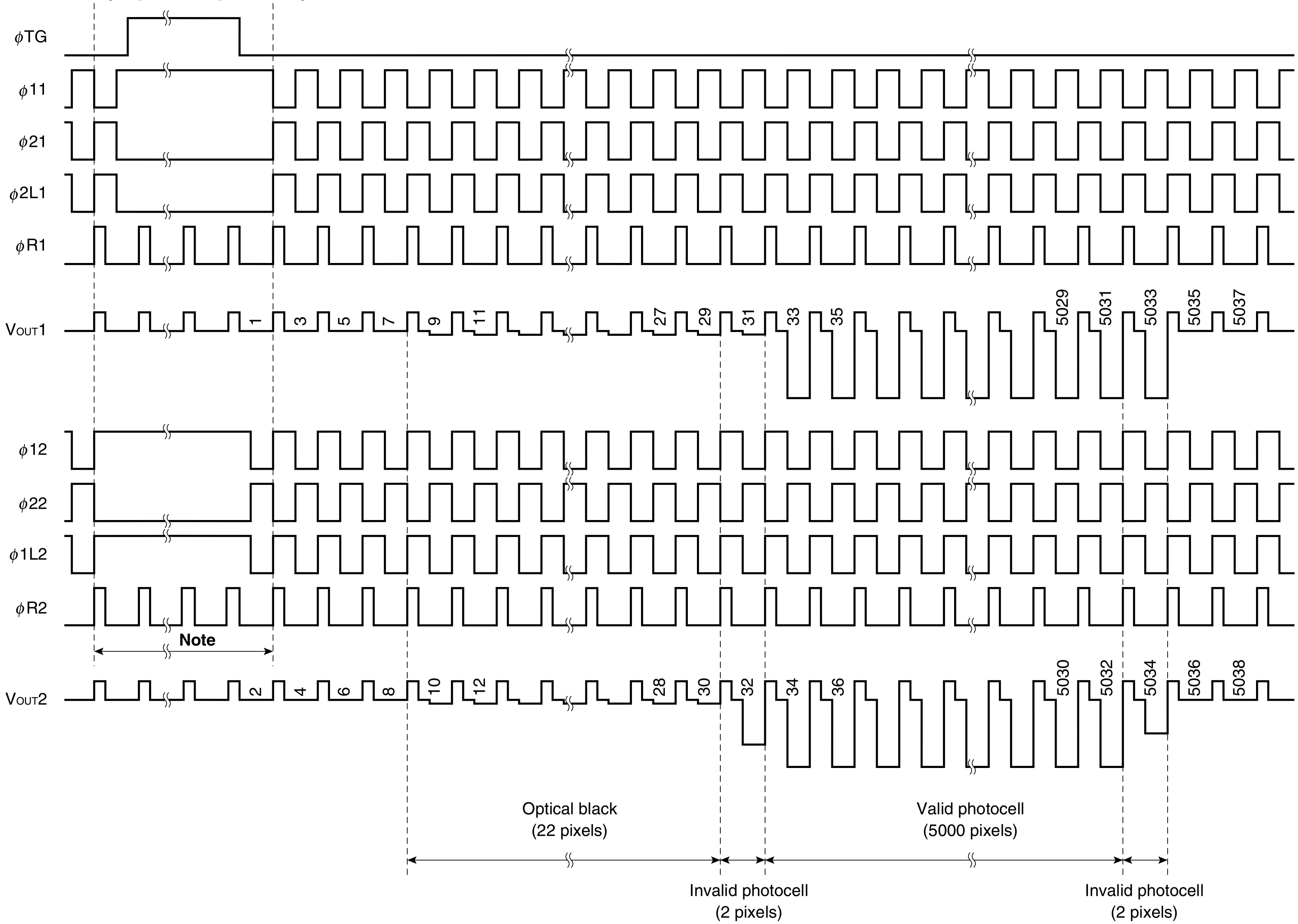
φ1L2, φ22 cross points



Remark Adjust cross points of (φ11, φ21), (φ12, φ22), (φ11, φ2L1) and (φ1L2, φ22) with input resistance of each pin.

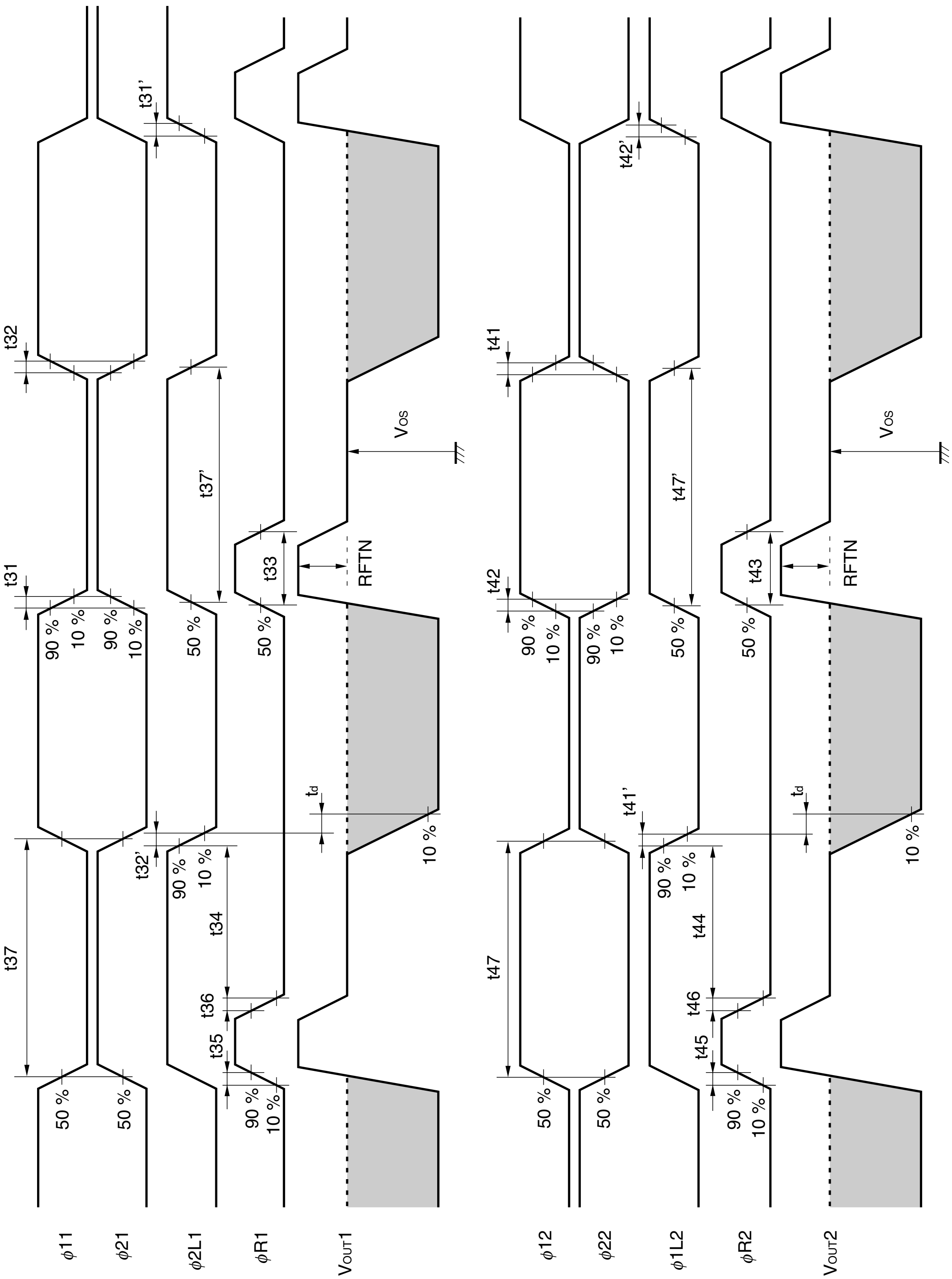
Symbol	MIN.	TYP.	MAX.	Unit
t1, t2, t11, t12	0	50	—	ns
t1', t2', t11', t12'	0	5	—	ns
t3, t13	15	50	—	ns
t4, t14	5	20	—	ns
t5, t6, t15, t16	0	20	—	ns
t7, t7', t17, t17'	25	—	—	ns
t21, t22	0	50	—	ns
t23	1000	2000	5000	ns
t24, t25	10	100	—	ns

TIMING CHART 4 (In phase operation)

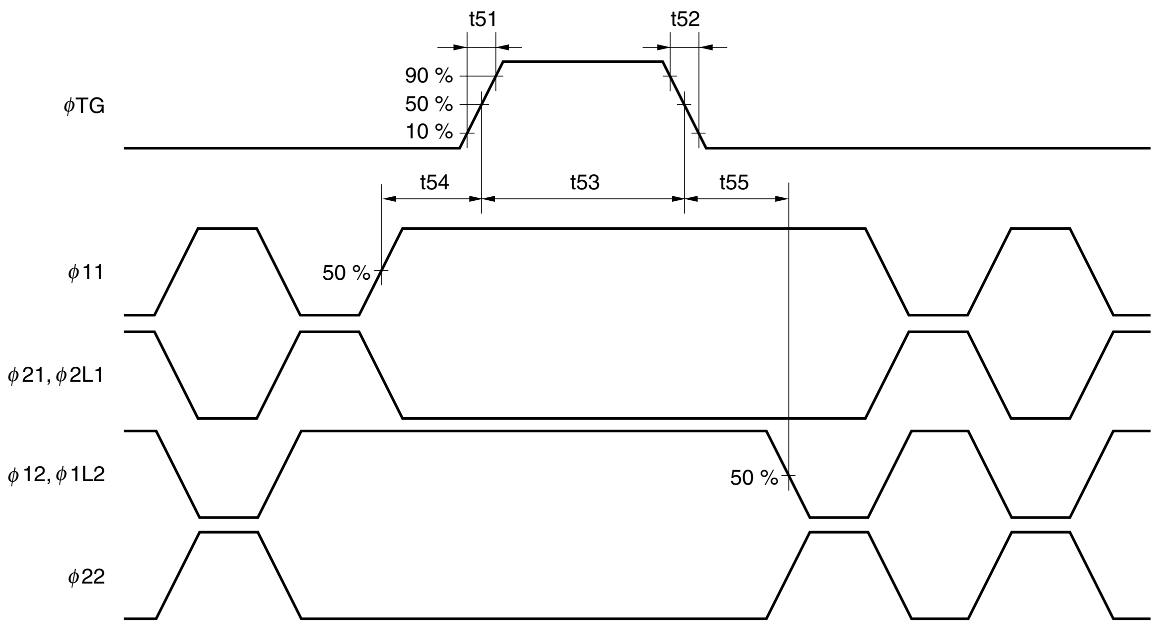


Note Input the ϕR1 and ϕR2 pulses continuously during this period, too.

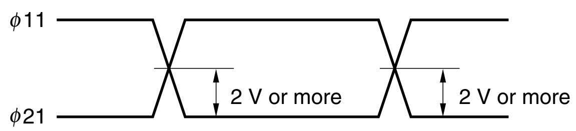
TIMING CHART 5 (In phase operation)



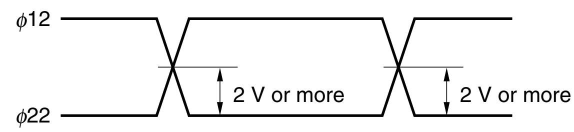
TIMING CHART 6 (In phase operation)



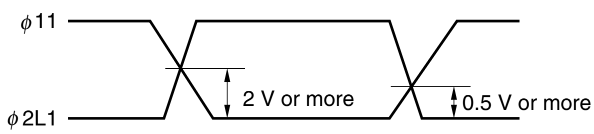
φ11, φ21 cross points



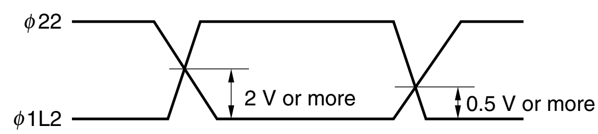
φ12, φ22 cross points



φ11, φ2L1 cross points



φ1L2, φ22 cross points



Remark Adjust cross points of (φ11, φ21), (φ12, φ22), (φ11, φ2L1) and (φ1L2, φ22) with input resistance of each pin.

Symbol	MIN.	TYP.	MAX.	Unit
t31, t32, t41, t42	0	50	—	ns
t31', t32', t41', t42'	0	5	—	ns
t33, t43	15	50	—	ns
t34, t44	5	20	—	ns
t35, t36, t45, t46	0	20	—	ns
t37, t37', t47, t47'	25	—	—	ns
t51, t52	0	50	—	ns
t53	1000	2000	5000	ns
t54, t55	10	100	—	ns

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: V_{sat}

Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE

Product of intensity of illumination (Ix) and storage time(s) when saturation of output voltage occurs.

3. Photo response non-uniformity: PRNU

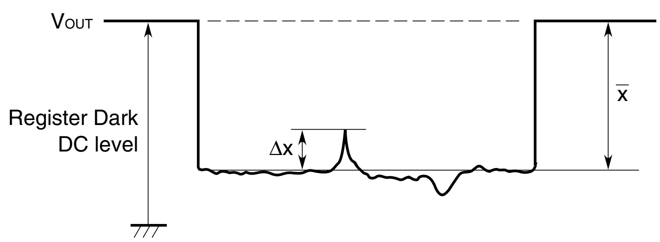
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$\text{PRNU}\ (\%) = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|\, x_j - \overline{x} \,|$

$$\overline{x} = \frac{\sum_{j=1}^{5000} x_j}{5000}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal: ADS

Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{ADS (mV)} = \frac{\sum_{j=1}^{5000} d_j}{5000}$$

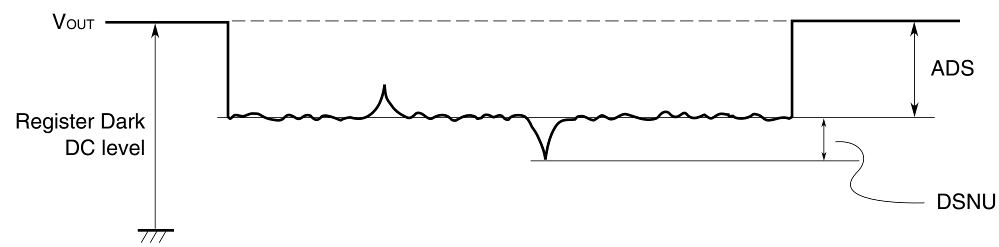
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity: DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV): maximum of $| d_j - ADS |_{\ j = 1 \text{ to } 5000}$

d_j : Dark signal of valid pixel number j



6. Output impedance: ZO

Impedance of the output pins viewed from outside.

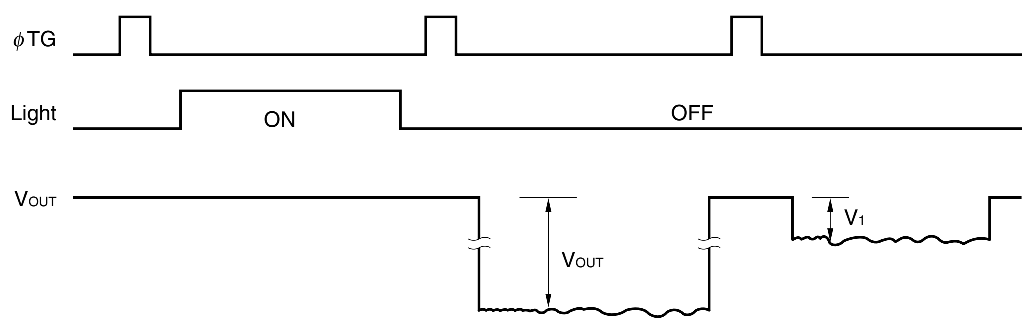
7. Response: R

Output voltage divided by exposure (lx•s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag: IL

The rate between the last output voltage and the next one after read out the data of a line.



$$IL (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Register imbalance: RI

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI\ (\%) = \frac{\dfrac{2}{n}\left|\displaystyle\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\dfrac{1}{n}\displaystyle\sum_{j=1}^{n} V_j} \times 100$$

n : Number of valid pixels

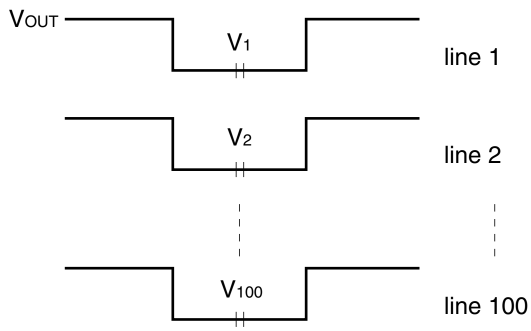
V_j : Output voltage of each pixel

10. Random noise: σ

Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding).

$$\sigma\ (mV) = \sqrt{\frac{\displaystyle\sum_{i=1}^{100} (V_i - \overline{V})^2}{100}} \quad , \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} V_i$$

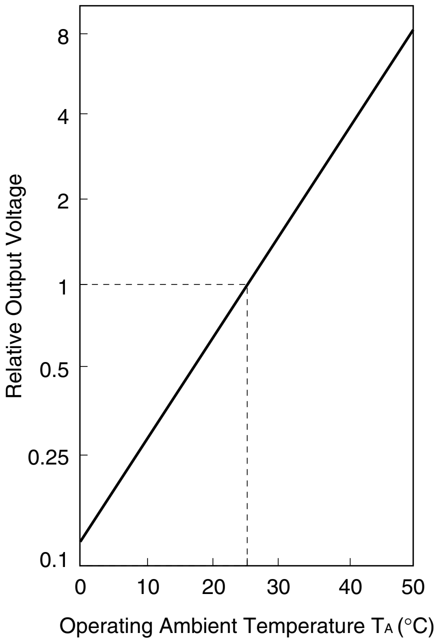
V_i : A valid pixel output signal among all of the valid pixels



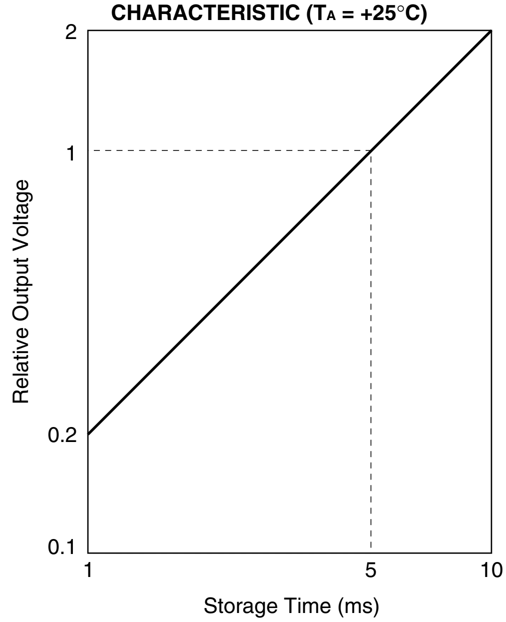
This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

STANDARD CHARACTERISTIC CURVES (Reference Value)

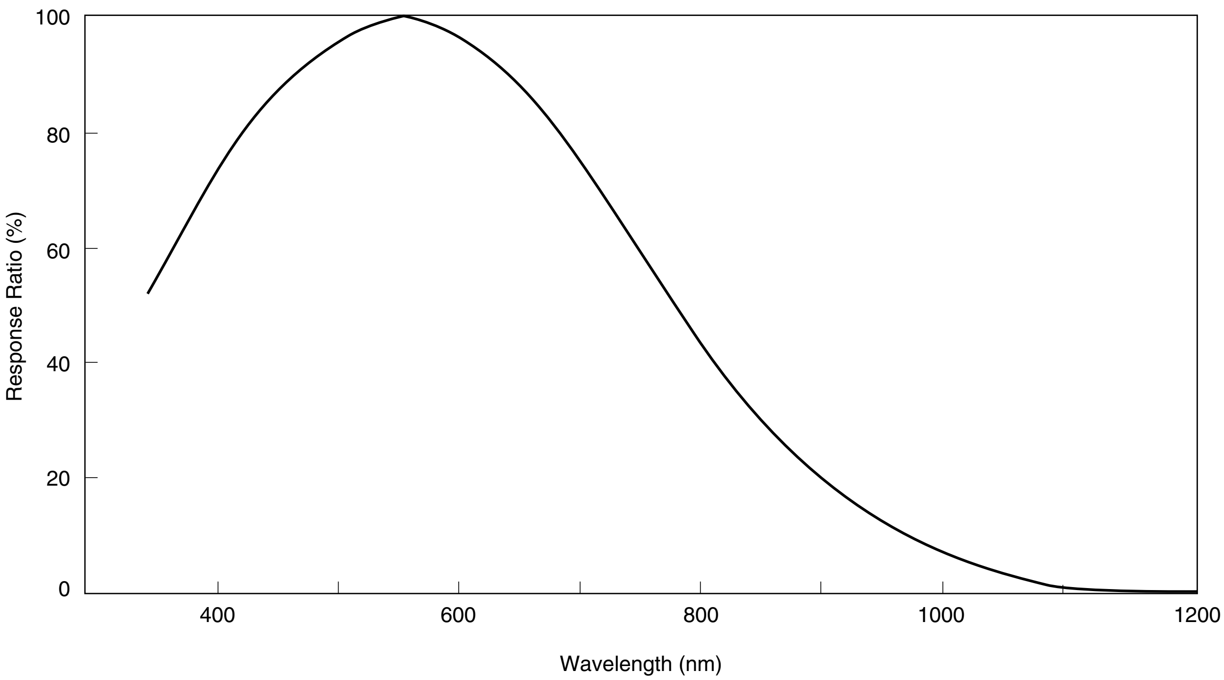
DARK OUTPUT TEMPERATURE CHARACTERISTIC



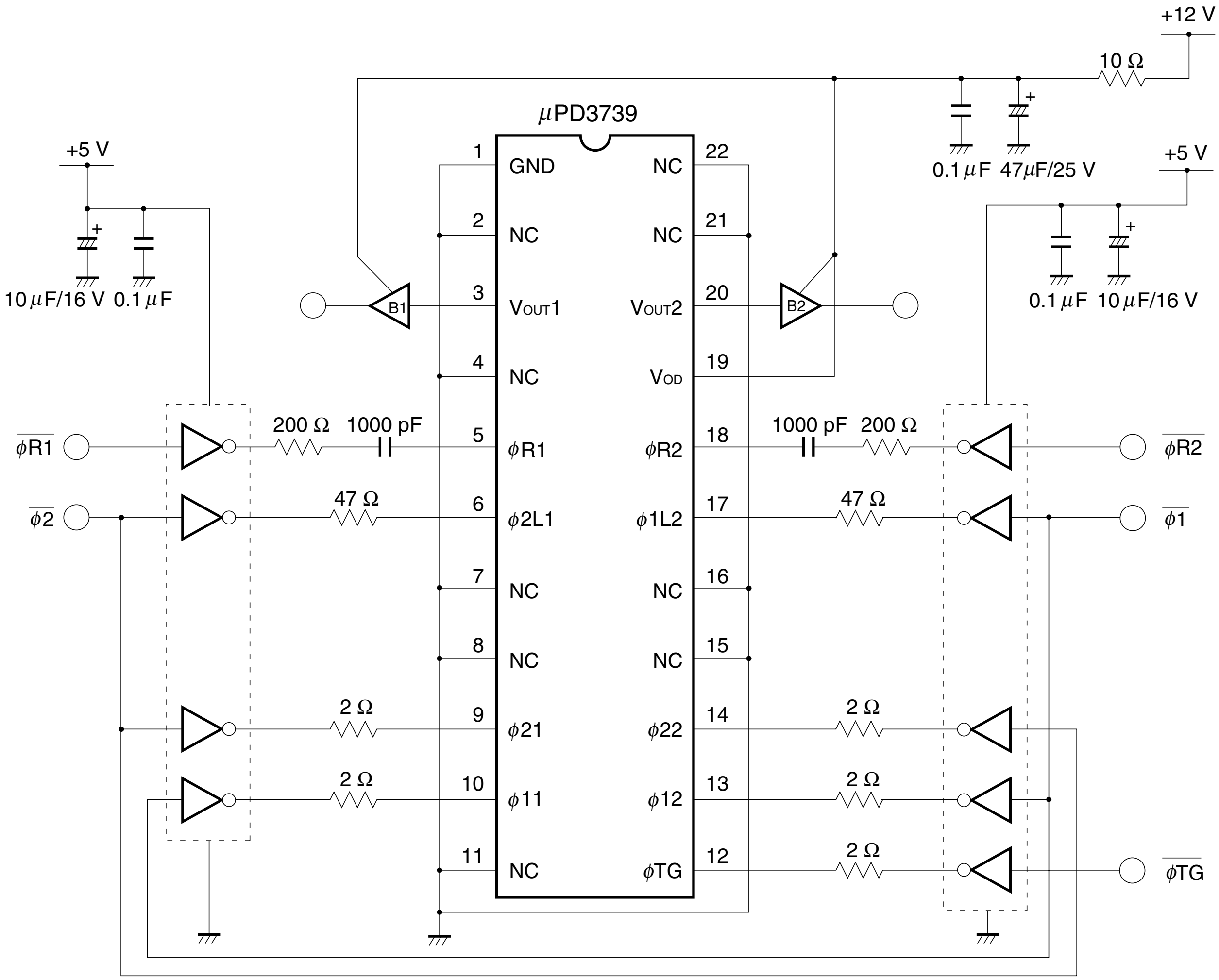
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (T_A = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTIC (without infrared cut filter) (T_A = +25°C)



APPLICATION CIRCUIT EXAMPLE (Out of phase operation)



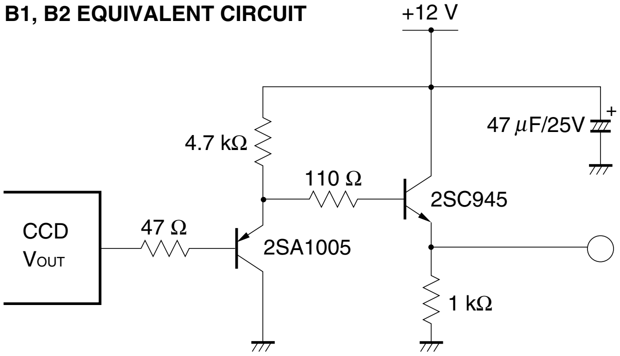
Caution Connect the No connection pins (NC) to GND.

Remarks **1.** The μPD3739 can be operated leaving pin 2 (NC) unconnected, and connecting pin 4 (NC) and pin 11 (NC) to a +12 V power supply.

2. It is recommended that pins 6 (φ2L1) and 17 (φ1L2) each is separately driven a driver other than that of pins 10, 13 (φ11, φ12) and pins 9, 14 (φ21, φ22).

3. The inverters shown in the above application circuit example are the 74AC04.

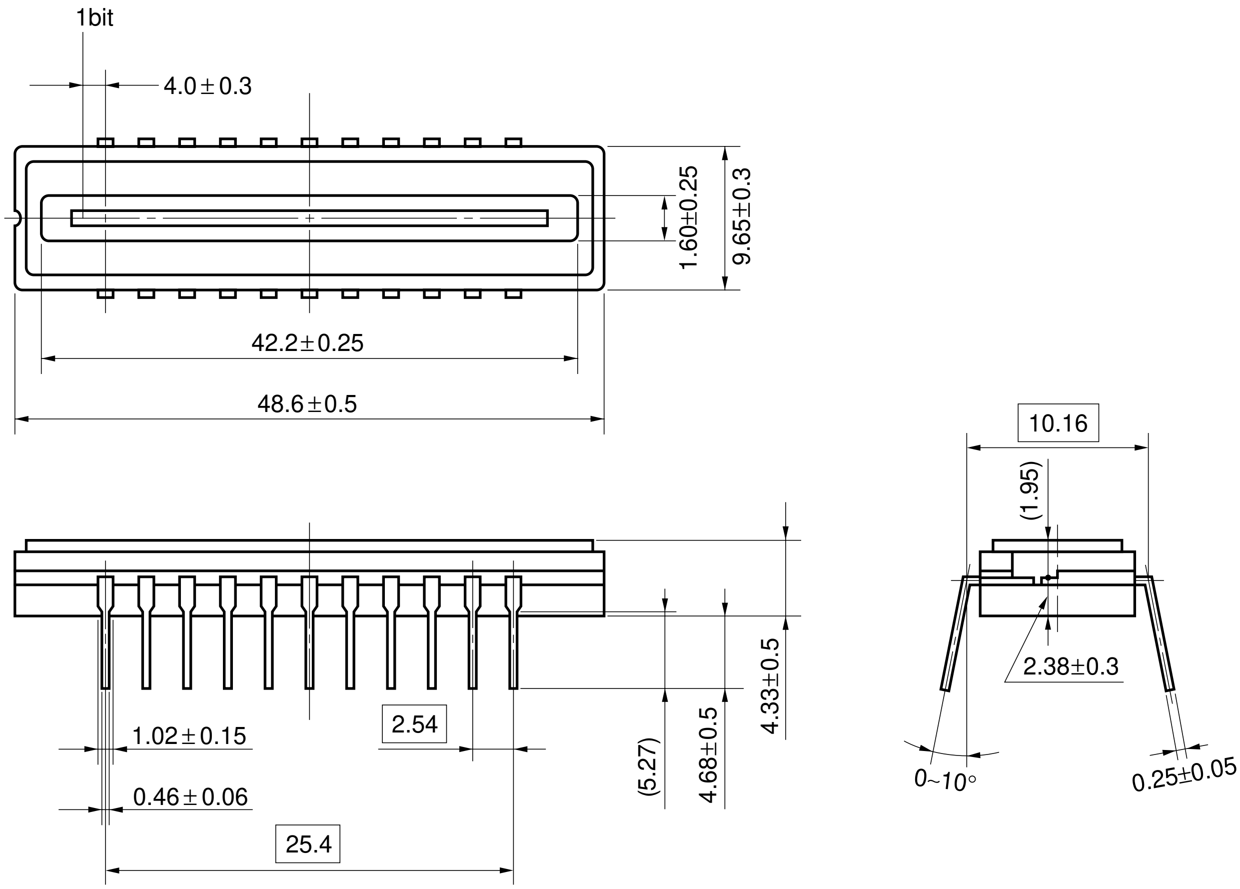
B1, B2 EQUIVALENT CIRCUIT



PACKAGE DRAWING

μPD3739D
CCD LINEAR IMAGE SENSOR 22-PIN CERAMIC DIP (CERDIP) (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Glass cap	47.5×9.25×0.7	1.5

22D-1CCD-PKG8-1

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD3739D-A: CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature: 380°C or below, Heat time: 3 seconds or less (per pin).

<R>

Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the glass cap. The optical characteristics could be degraded by such contact.

2. Soldering by the solder flow method may have deleterious effects on prevention of glass cap soiling and heat resistance. So the method cannot be guaranteed.

NOTES ON HANDLING THE PACKAGES

① MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with glass cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

② GLASS CAP

Don’t either touch glass cap surface by hand or have any object come in contact with glass cap surface. Care should be taken to avoid mechanical or thermal shock because the glass cap is easily to damage. For dirt stuck through electricity ionized air is recommended.

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[MEMO]

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.