

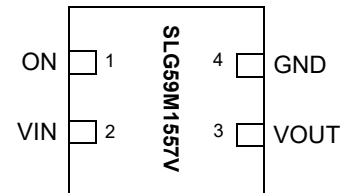
General Description

The SLG59M1557V is designed for load switching applications with ultra low quiescent current. The part comes with one 28.5 mΩ 1.0 A rated P-channel MOSFET controlled by a single ON control pin. The product is packaged in an ultra-small 1.0 x 1.0 mm package.

Features

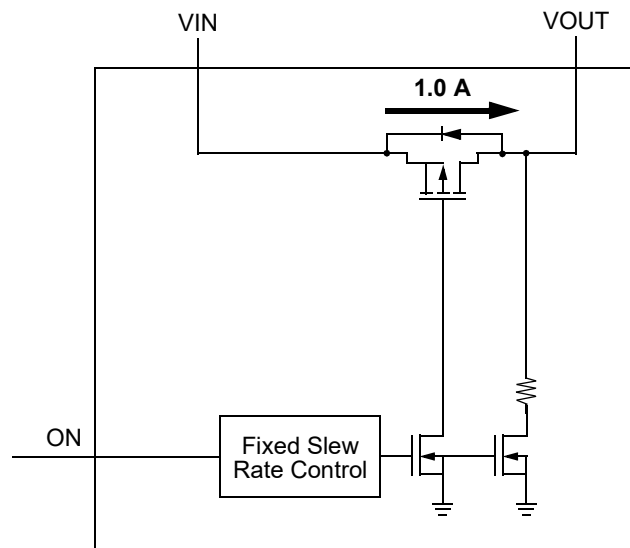
- One 1.0 A MOSFET
- Ultra Low Quiescent Current
- Low RDSON
 - 28.5 mΩ @ 5.0 V
 - 36.4 mΩ @ 3.3 V
 - 44.3 mΩ @ 2.5 V
 - 60.8 mΩ @ 1.8 V
 - 77.6 mΩ @ 1.5 V
- $V_{IN} = 1.5\text{ V to }5.5\text{ V}$
- Integrated Discharge Resistor
- Pb-Free / Halogen-Free / RoHS compliant
- STDFN 4L, 1.0 x 1.0 x 0.55 mm

Pin Configuration



4-pin STDFN
(Top View)

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	Turns on MOSFET.
2	VIN	MOSFET	Power MOSFET input
3	VOUT	MOSFET	Power MOSFET output
4	GND	GND	Ground

Ordering Information

Part Number	Type	Production Flow
SLG59M1557V	STDFN 4L	Industrial, -40 °C to 85 °C
SLG59M1557VTR	STDFN 4L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Supply		--	--	6	V
T_S	Storage Temperature		-65	--	140	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
W_{DIS}	Package Power Dissipation		--	--	0.5	W
MOSFET $I_{DS_{PK}}$	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	1.5	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

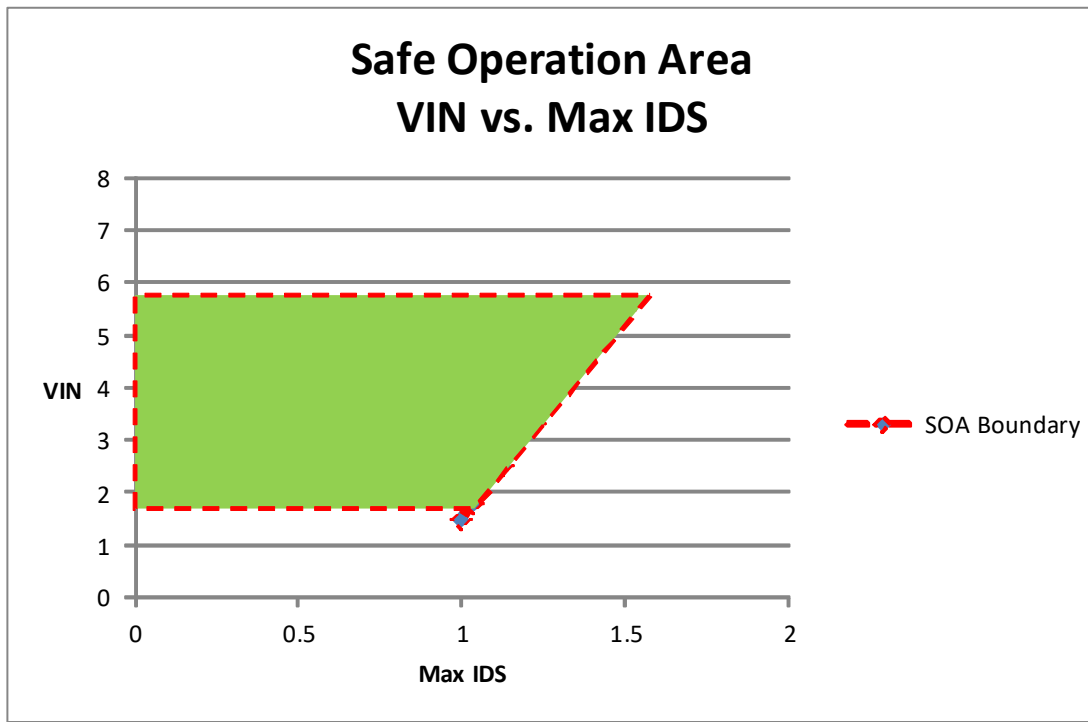
$T_A = -40\text{ °C to }85\text{ °C}$ (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Supply Voltage	-40 °C to 85 °C	1.5	--	5.5	V
I_{DD}	Power Supply Current (PIN 2)	when OFF, $V_{IN} = 5.5\text{ V}$, No load	--	0.02	1	μA
		when ON = V_{IN} , No load	--	0.05	0.5	μA
I_{ON_LKG}	ON Pin Input Leakage		--	--	0.1	μA
$R_{DS_{ON}}$	Static Drain to Source ON Resistance @ $T_A\ 25\text{ °C}$	@ 5.5 V, 100 mA	--	28.5	32.0	mΩ
		@ 3.3 V, 100 mA	--	36.4	40.0	mΩ
		@ 2.5 V, 100 mA	--	44.3	49.0	mΩ
		@ 1.8 V, 100 mA	--	60.8	65.0	mΩ
		@ 1.5 V, 100 mA	--	77.6	82.0	mΩ
$R_{DS_{ON}}$	Static Drain to Source ON Resistance @ $T_A\ 85\text{ °C}$	@ 5.5 V, 100 mA	--	34.0	36.0	mΩ
		@ 3.3 V, 100 mA	--	43.8	46.0	mΩ
		@ 2.5 V, 100 mA	--	53.3	56.0	mΩ
		@ 1.8 V, 100 mA	--	72.2	76.0	mΩ
		@ 1.5 V, 100 mA	--	90.7	94.0	mΩ
I_{DS}	Operating Current	$V_{IN} = 1.5\text{ V to }5.5\text{ V}$	--	--	1.0	A
T_{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin $V_{IN} = 5\text{ V}$, $V_{OUT_Cap} = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$	10	15	27	μs
		50% ON to Ramp Begin $V_{IN} = 3.3\text{ V}$, $V_{OUT_Cap} = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$	17	31	40	μs
		50% ON to Ramp Begin $V_{IN} = 1.5\text{ V}$, $V_{OUT_Cap} = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$	44	69	96	μs
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_{OUT} $V_{IN} = 5\text{ V}$, $V_{OUT_Cap} = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$	114	122	134	μs
		50% ON to 90% V_{OUT} $V_{IN} = 3.3\text{ V}$, $V_{OUT_Cap} = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$	146	156	176	μs
		50% ON to 90% V_{OUT} $V_{IN} = 1.5\text{ V}$, $V_{OUT_Cap} = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$	292	332	399	μs

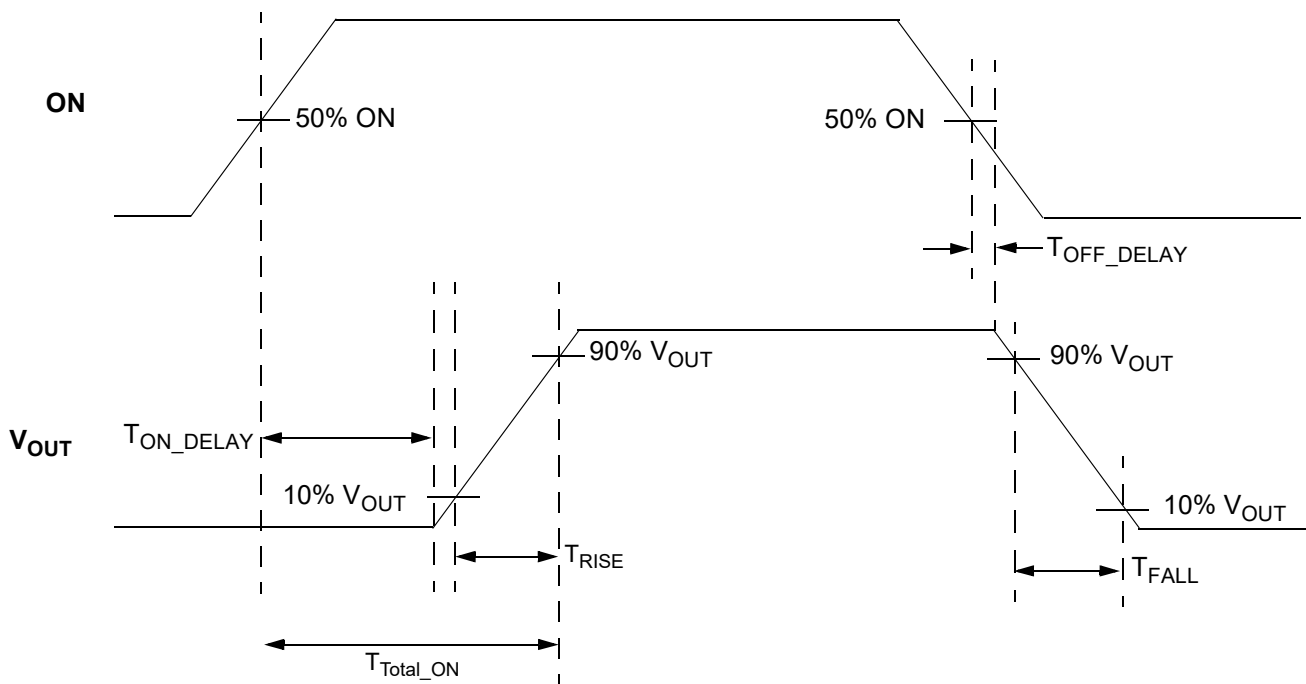
T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T _{RISE}	Rise Time	10% VOUT to 90% VOUT V _{IN} = 5.0 V, VOUT_Cap = 0.1 μF, R _L = 10 Ω	92	97	107	μs
		10% VOUT to 90% VOUT V _{IN} = 3.3 V, VOUT_Cap = 0.1 μF, R _L = 10 Ω	116	120	131	μs
		10% VOUT to 90% VOUT V _{IN} = 1.5 V, VOUT_Cap = 0.1 μF, R _L = 10 Ω	228	253	296	μs
R _{DIS}	Discharge Resistance	V _{IN} = 1.5 V to 5.5 V, V _{OUT} = 0.4 V Input Bias	65	80	400	Ω
ON_V _{IH}	Initial Turn On Voltage		0.85	--	V _{IN}	V
ON_V _{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
T _{Delay_OFF}	OFF Delay Time	50% ON to V _{OUT} Fall, V _{IN} = 5 V, R _L = 10 Ω, no C _L	6.2	6.5	7.0	μs

VIN vs. Max IDS, Safe Operation Area



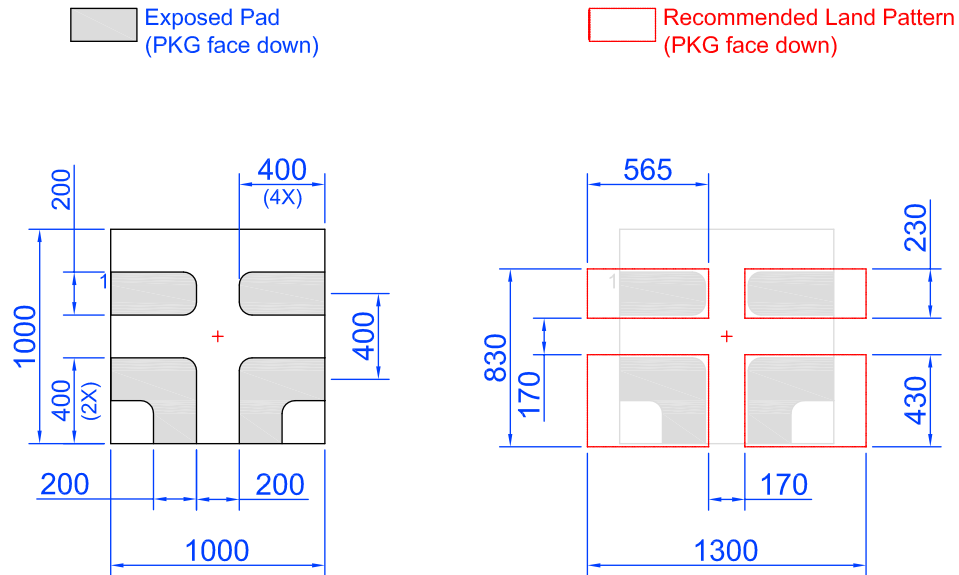
T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



SLG59M1557V Power-Up/Power-Down Sequence Considerations

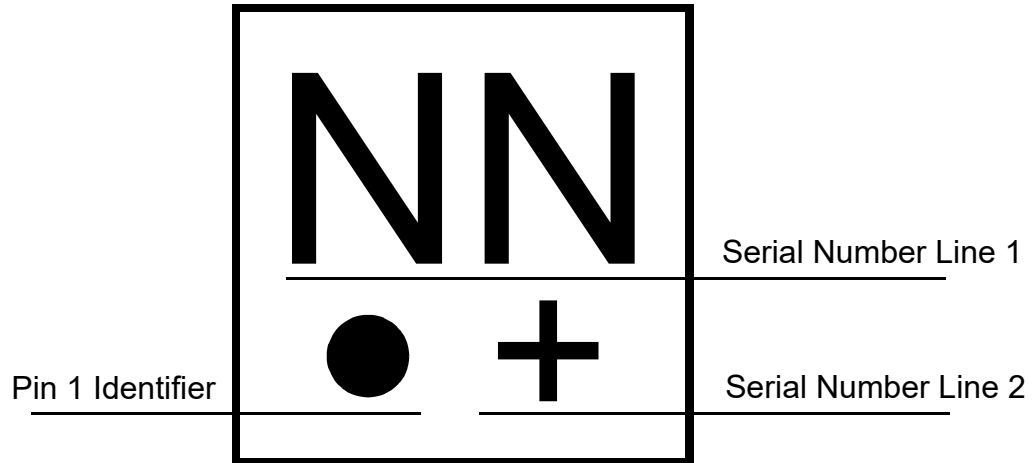
A nominal power-up sequence is to apply VIN and toggle the ON pin LOW-to-HIGH after VIN is at least 90% of its final value. A nominal power-down sequence is the power-up sequence in reverse order. If VIN ramp is too fast, a voltage glitch may appear on the output pin at VOUT. To prevent glitches at the output, it is recommended to connect at least 0.1uF capacitor from the VOUT pin to GND and to keep the VIN ramp time less than 2 ms.

SLG59M1557V Layout Suggestion



Note: All dimensions shown in micrometers (μm)

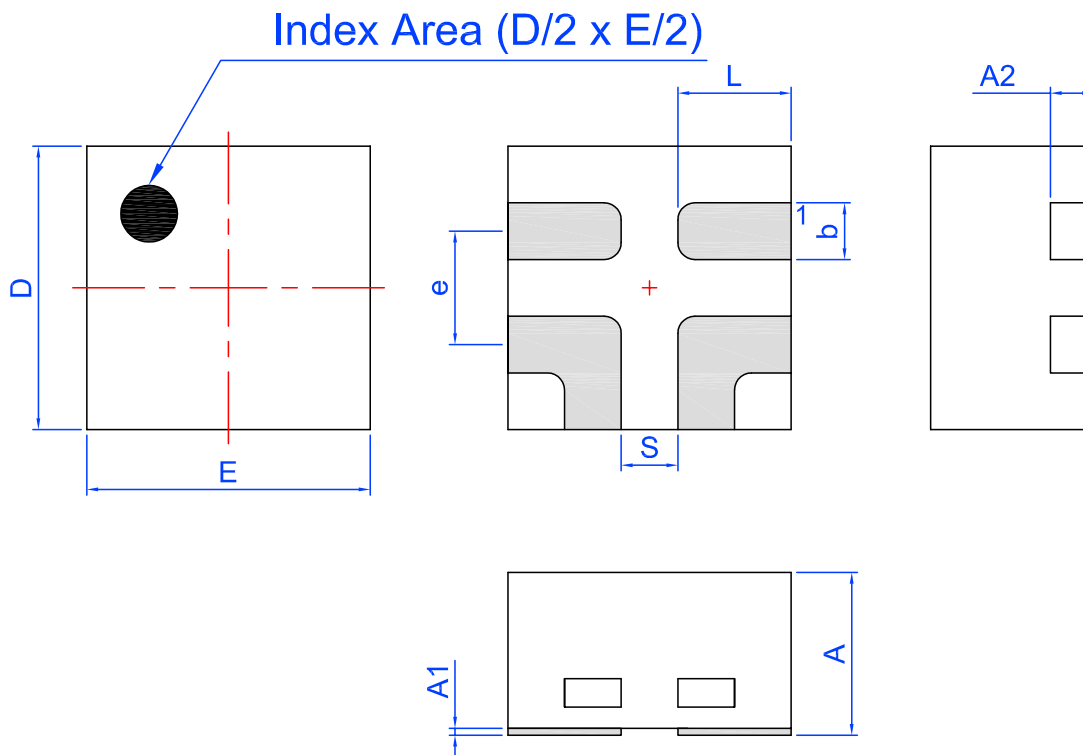
Package Top Marking System Definition



NN -Part Serial Number Field Line 1
 where each "N" character can be A-Z and 0-9
 + -Part Serial Number Field Line 2
 where "+" character can be +, -, =, or blank

Package Drawing and Dimensions

4 Lead STDFN Package 1.0 x 1.0 mm



Unit: mm

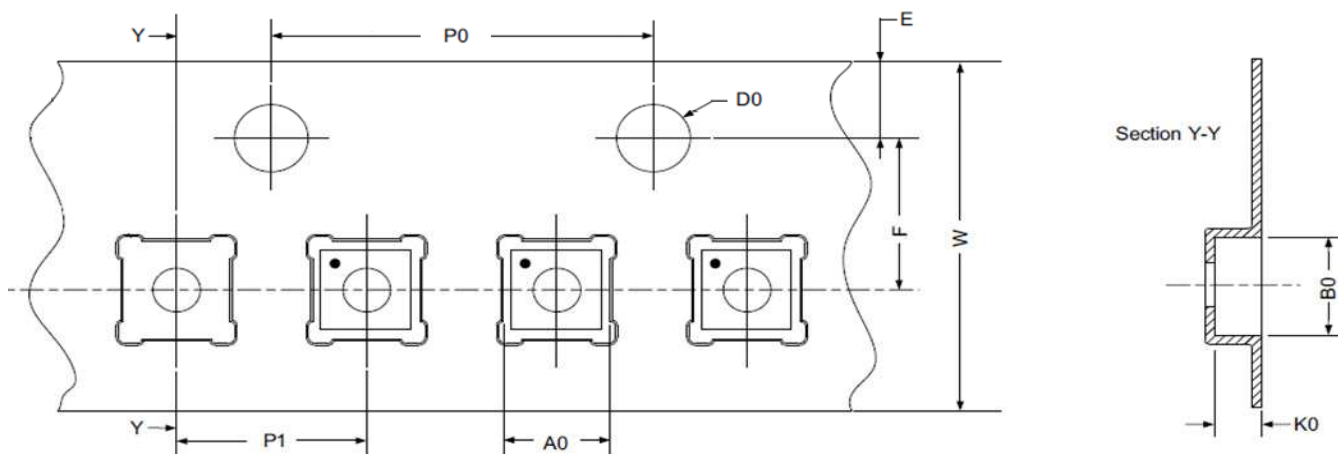
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	0.95	1.00	1.05
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.15	0.20	0.25	S	0.2 REF		
e	0.40 BSC						

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 4L 1x1mm 0.4P FC Green	4	1.0 x 1.0 x 0.55	8000	8000	178 / 60	200	400	200	400	8	2

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 4L 1x1mm 0.4P FC Green	1.16	1.16	0.63	4	2	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.55 mm³ (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/4/2022	1.04	Updated Company name and logo Fixed typos
11/14/2017	1.03	Updated Package Marking Definition
6/22/2016	1.02	Added section on Power Up/Down Sequence Considerations Removed IDS_ikg parameter (same as IDD when OFF) Updated Recommended Layout suggestion
9/11/2015	1.01	Updated IDD and Tdelay_ON

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.