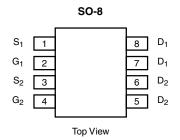




# **Dual N-Channel 30 V (D-S) MOSFET**

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
30	0.014 at V <sub>GS</sub> = 10 V	12.1	5.4 nC		
30	0.017 at V <sub>GS</sub> = 4.5 V	11	5.4110		



Ordering Information: Si4202DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

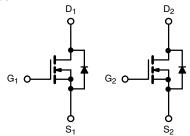
### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> Tested 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

# COMPLIANT HALOGEN **FREE**

### **APPLICATIONS**

- · Synchronous Buck
  - Notebooks
  - Servers
  - STB



N-Channel MOSFET N-Channel MOSFET

ABSOLUTE MAXIMUM RATING	<b>S</b> (T <sub>A</sub> = 25 °C, unle	ess otherwise r	noted)		
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	30	V		
Gate-Source Voltage		V <sub>GS</sub>	± 20	]	
	T <sub>C</sub> = 25 °C		12.1		
Continuous Drain Current /T 150 °C)	T <sub>C</sub> = 70 °C	. [	11		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	9.7 <sup>a, b</sup>	<b>A</b>	
	T <sub>A</sub> = 70 °C		8.2 <sup>a, b</sup>		
Pulsed Drain Current	<u> </u>	I <sub>DM</sub>	50	Α	
Continuous Source Drain Diode Current	T <sub>C</sub> = 25 °C	_	3.1		
Continuous Source Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2 <sup>a, b</sup>		
Avalanche Current	L = 0 1 mH	I <sub>AS</sub>	15		
Single-Pulse Avalanche Energy	L=UIMH	E <sub>AS</sub>	11.25	mJ	
	T <sub>C</sub> = 25 °C		3.7		
Manine Device Disable ation	T <sub>C</sub> = 70 °C		2.6	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	- P <sub>D</sub>	2.4 <sup>a, b</sup>	VV	
	T <sub>A</sub> = 70 °C		1.7 <sup>a, b</sup>		
Operating Junction and Storage Temperature R	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>a, c</sup>	t ≤ 10 s	R <sub>thJA</sub>	50	62.5	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	33	41	- C/VV	

### Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. Maximum under steady state conditions is 110 °C/W.

# Vishay Siliconix



<b>SPECIFICATIONS</b> ( $T_J = 25$ °C	ر, uniess otl	nerwise noted)		T		1	
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		33		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_{J}$	10 = 200 μΛ		- 5.3		mv/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1.0		2.5	V	
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zoro Coto Voltago Droin Current	1	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
	В	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8 A		0.0115	0.0140	_	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$		0.0138	0.0170	Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 8 A		33		S	
Dynamic <sup>b</sup>					•		
Input Capacitance	C <sub>iss</sub>			710		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		146			
Reverse Transfer Capacitance	C <sub>rss</sub>			63			
T. 10 . 0	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$		11.2	17		
Total Gate Charge				5.4	8		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 8 \text{ A}$		1.6		nC	
Gate-Drain Charge	$Q_{gd}$			1.6		1	
Gate Resistance	$R_{g}$	f = 1 MHz	0.5	2.5	5	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			11	22		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 3 $\Omega$		18	35		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 5$ A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 $\Omega$		14	28		
Fall Time	t <sub>f</sub>			8	16		
Turn-On Delay Time	t <sub>d(on)</sub>			8	16	ns	
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_L = 3 \Omega$		9	18	-	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 5$ A, $V_{GEN}=10$ V, $R_g=1$ $\Omega$		17	34		
Fall Time	t <sub>f</sub>			8	16		
<b>Drain-Source Body Diode Characteris</b>	tics						
Continuous Source-Drain Diode Current	Is	T <sub>C</sub> = 25 °C			3.1		
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				50	Α	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 3 A		0.75	1.2	٧	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			13	26	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	L EA di/dt 100 A/ T 05 00		5.5	11	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$		8			
Reverse Recovery Rise Time	t <sub>b</sub>			5	1	ns	

### Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

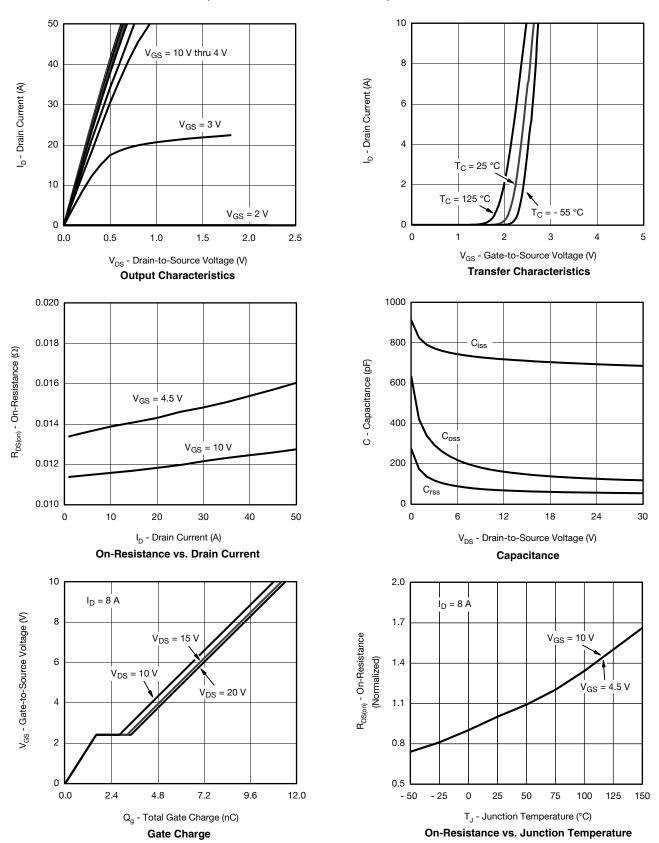
a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.



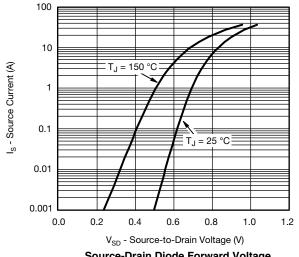


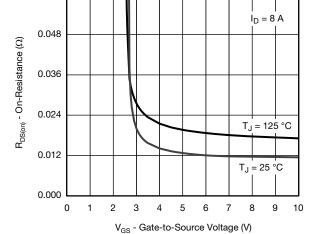
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



# Vishay Siliconix

### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

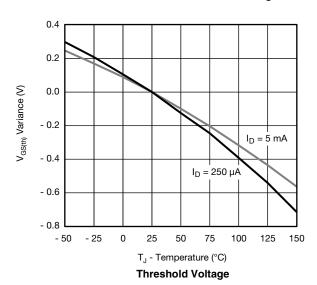


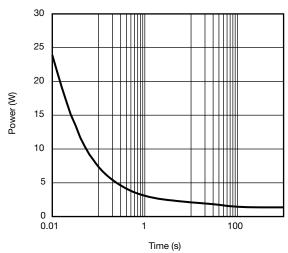


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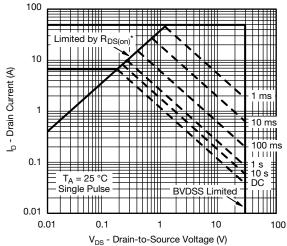
Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage





Single Pulse Power, Junction-to-Ambient

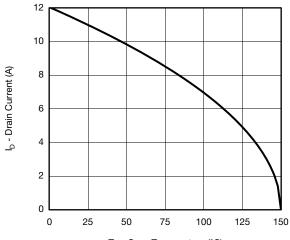


\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area

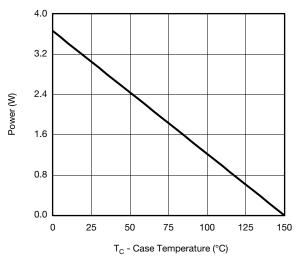


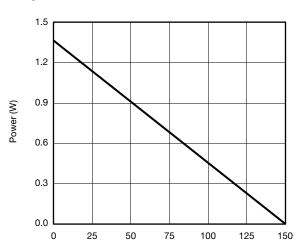
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



T<sub>C</sub> - Case Temperature (°C)

### **Current Derating\***





T<sub>A</sub> - Ambient Temperature (°C)

Power, Junction-to-Case

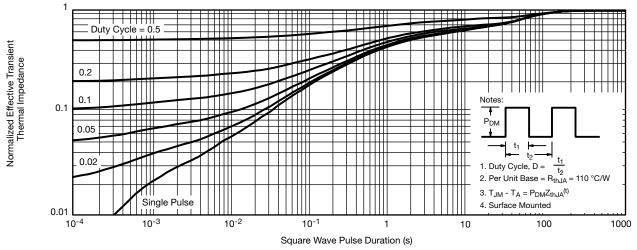
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

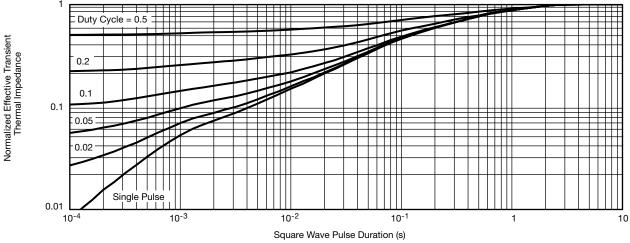
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### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



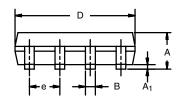
Normalized Thermal Transient Impedance, Junction-to-Foot

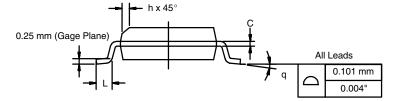
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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIMETERS INCHES			HES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06

# APPLICATION NOTE



### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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Vishay

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