NCV8184

Tracking Regulator/Line Driver - Micropower, Low Dropout

70 mA

The NCV8184 is a monolithic integrated low dropout tracking voltage regulator designed to provide an adjustable buffered output voltage that closely tracks (±3.0 mV) the reference input.

The part can be used in automotive applications with remote sensors, or any situation where it is necessary to isolate the output of your regulator.

The NCV8184 also enables the user to bestow a quick upgrade to their module when added current is needed, and the existing regulator cannot provide.

The versatility of this part also enables it to be used as a high−side driver.

Features

- 70 mA Source Capability
- Output Tracks within ±3.0 mV
- Low Input Voltage Tracking Performance (Works Down to V_{REF} = 2.1 V)
- Low Dropout (0.35 V Typ. @ 50 mA)
- Low Quiescent Current
- Thermal Shutdown
- Wide Operating Range
- Internally Fused Leads in SOIC−8 Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

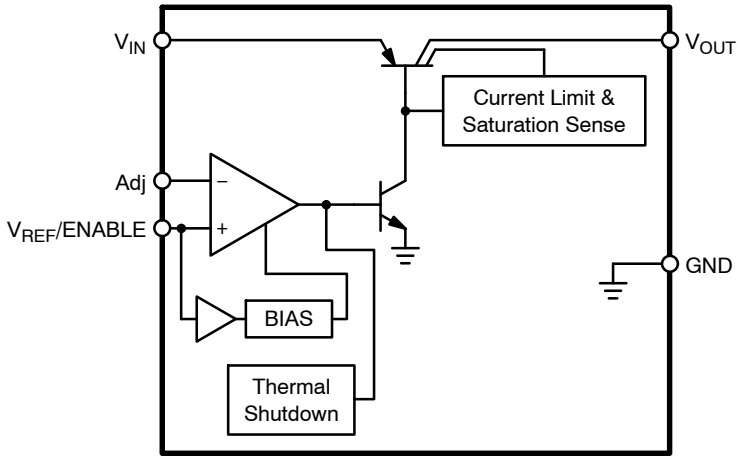

Figure 1. Block Diagram

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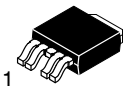
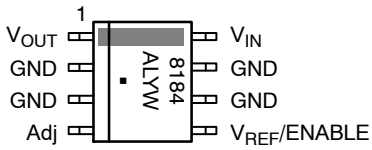
SOIC−8
D SUFFIX
CASE 751

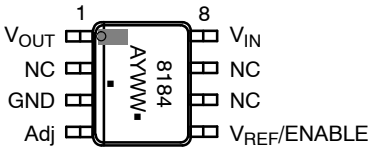
SOIC−8 EP
PD SUFFIX
CASE 751AC

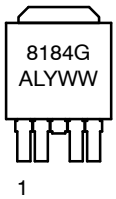


DPAK 5−LEAD
DT SUFFIX
CASE 175AA

PIN CONNECTIONS AND MARKING DIAGRAMS







Pin 1. V_{IN}
2. V_{OUT}
Tab, 3. GND
4. Adj
5. V_{REF}/ENABLE

8184	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W, WW	= Work Week
▪ or G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

MAXIMUM RATINGS

Rating		Value	Unit
Storage Temperature		−65 to 150	°C
Supply Voltage Range (Continuous)		−15 to 45	V
Supply Voltage Operating Range		4.0 to 42	V
Peak Transient Voltage (V_{IN} = 14 V, Load Dump Transient = 31 V)		45	V
Voltage Range (V_{OUT}, Adj)		−3.0 to 45	V
Voltage Range (V_{REF}/ENABLE)		−0.3 to 45	V
Maximum Junction Temperature		150	°C
ESD Capability	Human Body Model Machine Model Charge Device Model	2.5 200 1000	kV V V
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	240 peak 260 peak (Pb−Free) (Note 2)	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 second maximum above 183°C.
2. −5°C / +0°C Allowable Conditions, applies to both Pb and Pb−Free devices.

THERMAL CHARACTERISTICS See Package Thermal Data Section (Page 8)

ELECTRICAL CHARACTERISTICS (V_{IN} = 14 V; V_{REF}/ENABLE > 2.1 V; −40°C < T_J < +150°C; C_{OUT} = 1.0 μF; I_{OUT} = 1.0 mA; Adj = V_{OUT}; $C_{OUT-ESR}$ = 1.0 Ω, unless otherwise specified.)

Parameter	Test Conditions	Min	Typ	Max	Unit
REGULATOR OUTPUT					
V_{REF}/ENABLE − V_{OUT} V_{OUT} Tracking Error	5.7 V ≤ V_{IN} ≤ 26 V, 100 μA ≤ I_{OUT} ≤ 60 mA 2.1 V ≤ V_{REF}/ENABLE ≤ (V_{IN} − 600 mV)	−3.0	–	3.0	mV
Dropout Voltage (V_{IN} − V_{OUT})	I_{OUT} = 100 μA I_{OUT} = 5.0 mA I_{OUT} = 60 mA	– – –	100 250 350	150 500 600	mV mV mV
Line Regulation	5.7 V ≤ V_{IN} ≤ 26 V, V_{REF}/ENABLE = 5.0 V	–	–	3.0	mV
Load Regulation	100 μA ≤ I_{OUT} ≤ 60 mA, V_{REF}/ENABLE = 5.0 V	–	–	3.0	mV
Adj Input Bias Current	V_{REF}/ENABLE = 5.0 V	–	0.2	6.0	μA
Current Limit	V_{IN} = 14 V, V_{REF} = 5.0 V, V_{OUT} = 90% of V_{REF} (Note 3)	70	–	225	mA
Quiescent Current (I_{IN} − I_{OUT})	V_{IN} = 12 V, I_{OUT} = 60 mA V_{IN} = 12 V, I_{OUT} = 100 μA V_{IN} = 12 V, V_{REF}/ENABLE = 0 V	– – –	5.0 50 –	7.0 70 20	mA μA μA
Ripple Rejection	f = 120 Hz, I_{OUT} = 60 mA, 6.0 V ≤ V_{IN} ≤ 26 V	60	–	–	dB
Thermal Shutdown	Guaranteed by Design	150	180	210	°C
V_{REF}/ENABLE					
Enable Voltage	–	0.8	–	2.1	V
Input Bias Current	V_{REF}/ENABLE = 5.0 V	–	0.2	3.0	μA

3. V_{OUT} connected to Adj lead.

PACKAGE PIN DESCRIPTION

Package Lead Number			Lead Symbol	Function
SOIC−8 EPAD	SOIC−8	DPAK, 5−LEAD		
8	8	1	V_{IN}	Battery supply input voltage.
1	1	2	V_{OUT}	Regulated output.
3, EPAD	2, 3, 6, 7	Tab, 3	GND	Ground.
4	4	4	Adj	Adjust lead, noninverting input.
5	5	5	V_{REF}/ENABLE	Reference voltage and ENABLE input.
2, 6, 7	–	–	NC	No Connection. PCB traces allowed.

TYPICAL PERFORMANCE CHARACTERISTICS

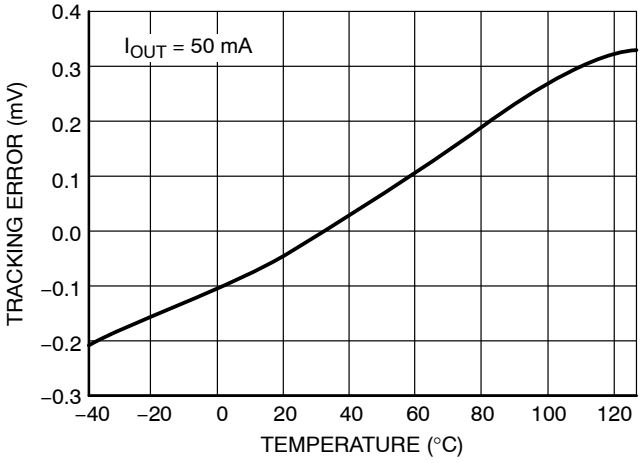


Figure 2. Tracking Error vs. Temperature

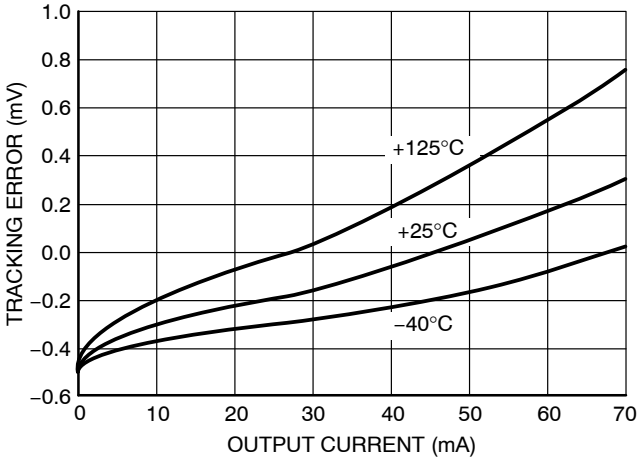


Figure 3. Tracking Error vs. Output Current

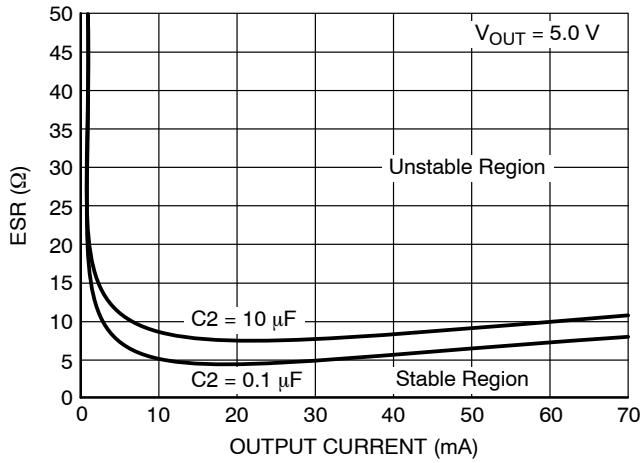


Figure 4. Output Stability with Capacitor Change

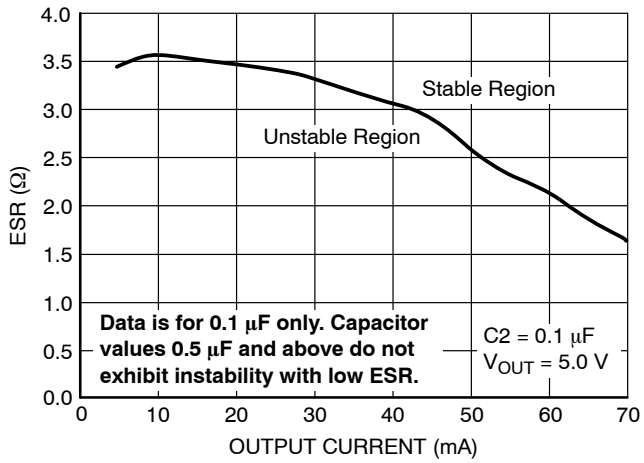


Figure 5. Output Stability with 0.1 μF at Low ESR

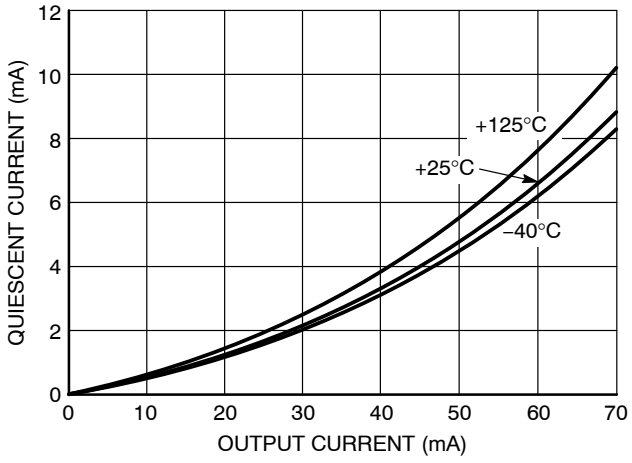


Figure 6. Quiescent Current vs. Output Current

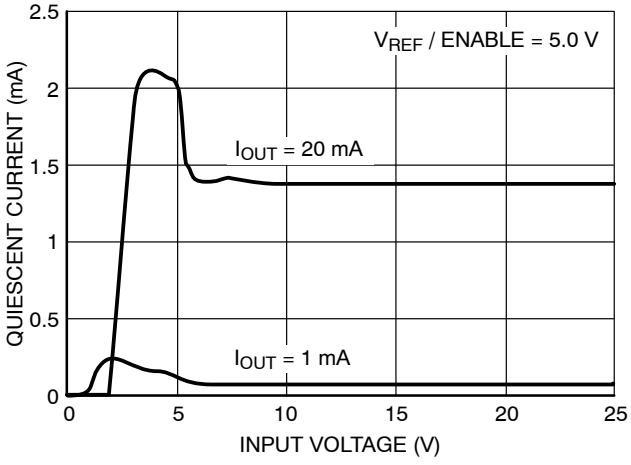


Figure 7. Quiescent Current vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

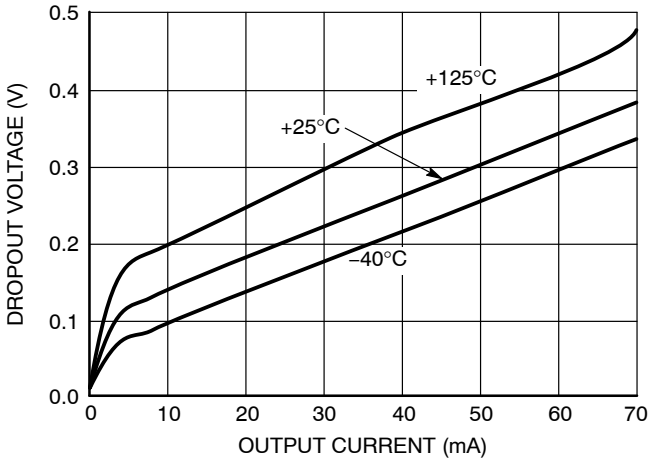


Figure 8. Dropout Voltage vs. Output Current

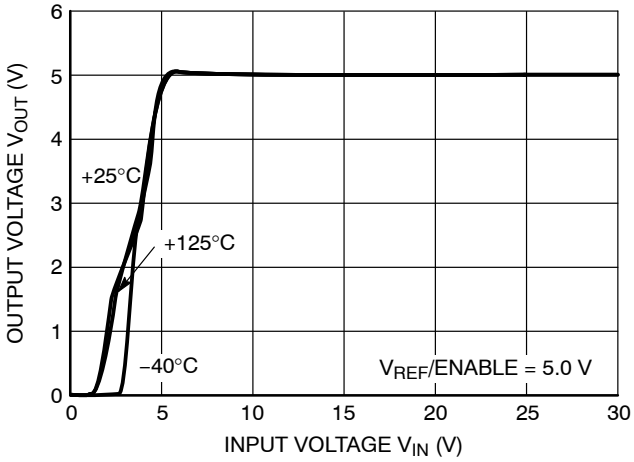


Figure 9. Output Voltage vs. Input Voltage

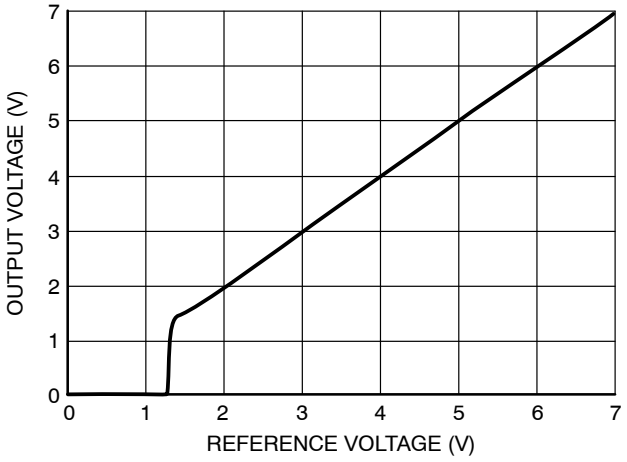


Figure 10. Output Voltage vs. Reference Voltage

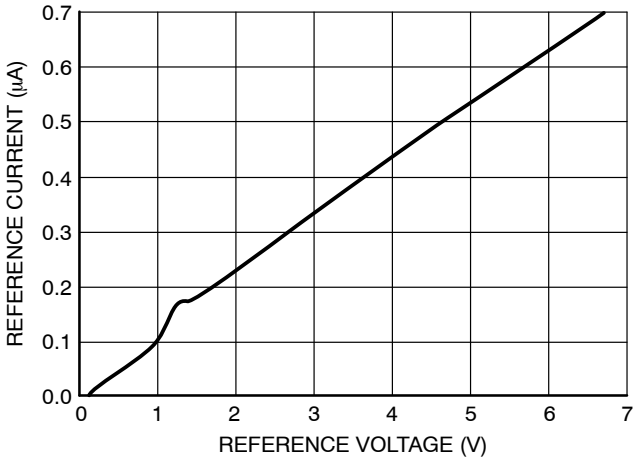


Figure 11. Reference Current vs. Reference Voltage

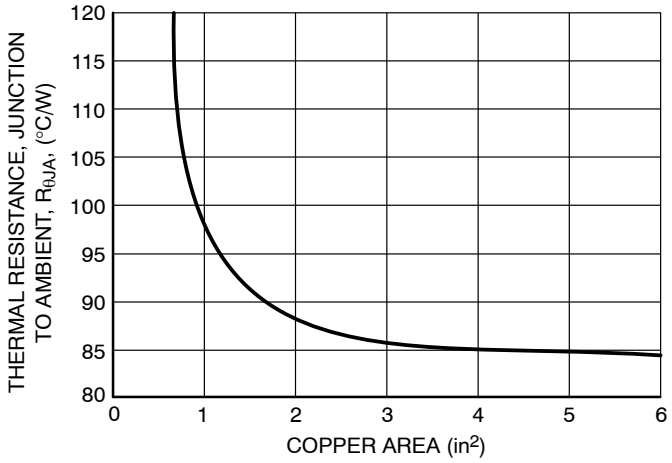


Figure 12. SOIC−8, θJA as a Function of the Pad Copper Area (2.0 oz. Cu Thickness), Board Material = 0.0625 G−10/R−4

CIRCUIT DESCRIPTION

ENABLE Function

By pulling the V_{REF}/ENABLE lead below 0.8 V, (see Figure 16 or Figure 17), the IC is disabled and enters a sleep state where the device draws less than 20 μA from supply. When the V_{REF}/ENABLE lead is greater than 2.1 V, V_{OUT} tracks the V_{REF}/ENABLE lead normally.

Output Voltage

The output is capable of supplying 70 mA to the load while configured as a similar (Figure 13), lower (Figure 15), or higher (Figure 14) voltage as the reference lead. The Adj lead acts as the inverting terminal of the op amp and the V_{REF} lead as the non−inverting.

The device can also be configured as a high−side driver as displayed in Figure 18.

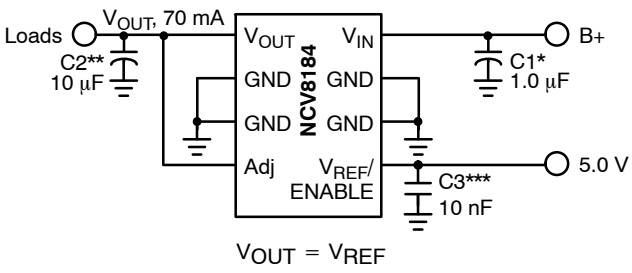


Figure 13. Tracking Regulator at the Same Voltage

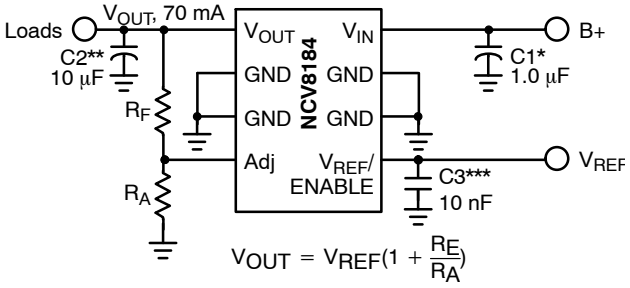


Figure 14. Tracking Regulator at Higher Voltages

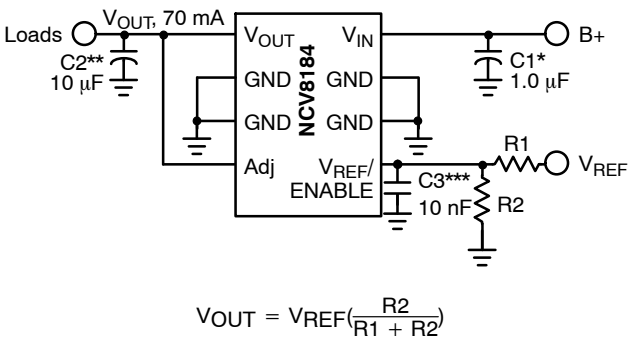


Figure 15. Tracking Regulator at Lower Voltages

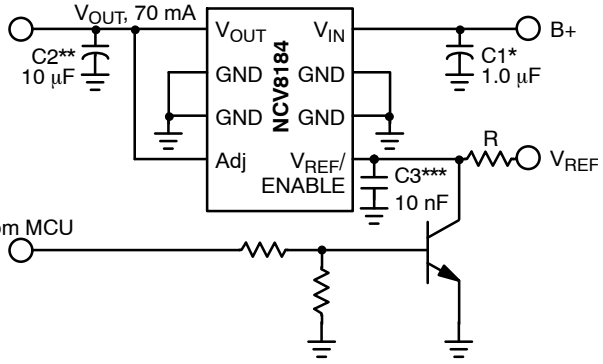


Figure 16. Tracking Regulator with ENABLE Circuit

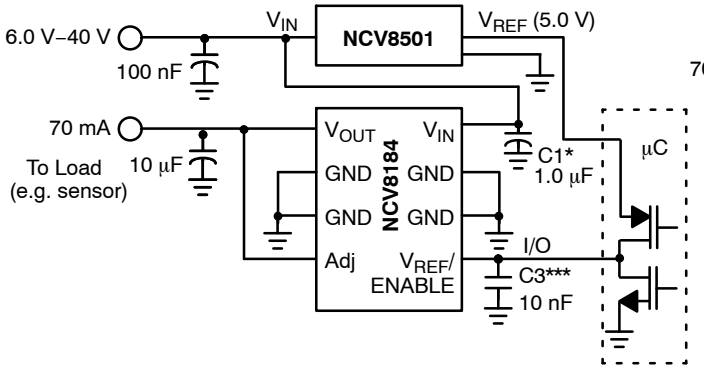


Figure 17. Alternative ENABLE Circuit

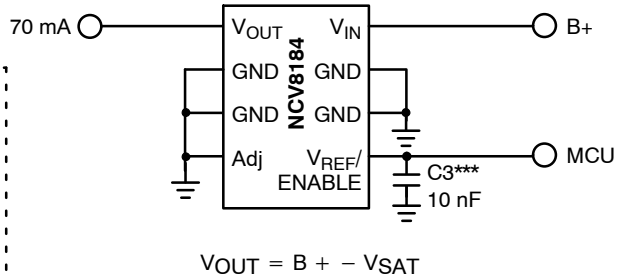


Figure 18. High−Side Driver

* C1 is required if the regulator is far from the power source filter. In case of power supply generates voltage ripple (e.g. DC-DC converter) a passive low pass filter with C1 value at least 1 μF is required to suppress the ripple. The filter should be designed according to particular operating conditions and verified in the application.

** C2 is required for stability.

*** C3 is recommended for EMC susceptibility

APPLICATION NOTES

V_{OUT} Short to Battery

The NCV8184 will survive a short to battery when hooked up the conventional way as shown in Figure 19. No damage to the part will occur. The part also endures a short to battery when powered by an isolated supply at a lower voltage as in Figure 20. In this case the NCV8184 supply input voltage is set at 7.0 V when a short to battery (14 V typical) occurs on V_{OUT} which normally runs at 5.0 V. The current into the device (ammeter in Figure 20) will draw additional current as displayed in Figure 21.

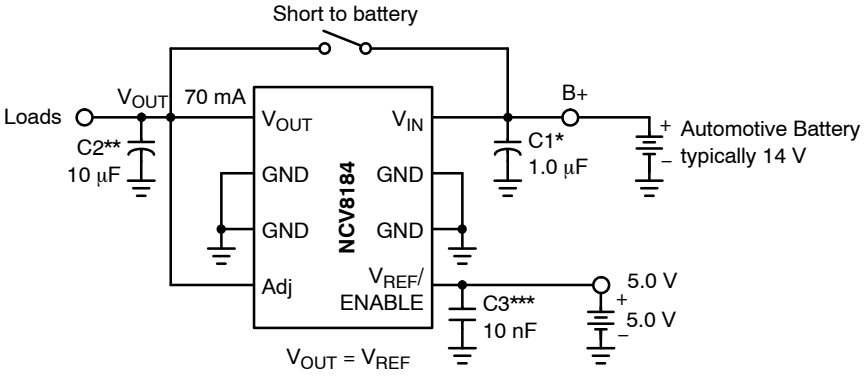
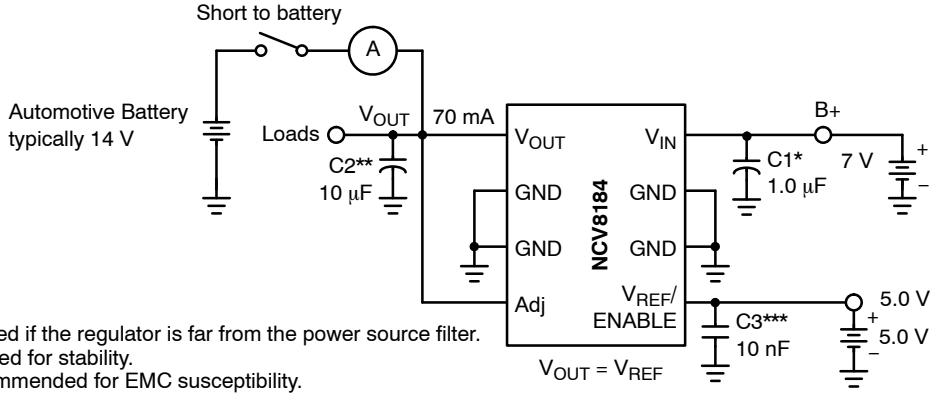


Figure 19.



* C1 is required if the regulator is far from the power source filter.
** C2 is required for stability.
*** C3 is recommended for EMC susceptibility.

Figure 20.

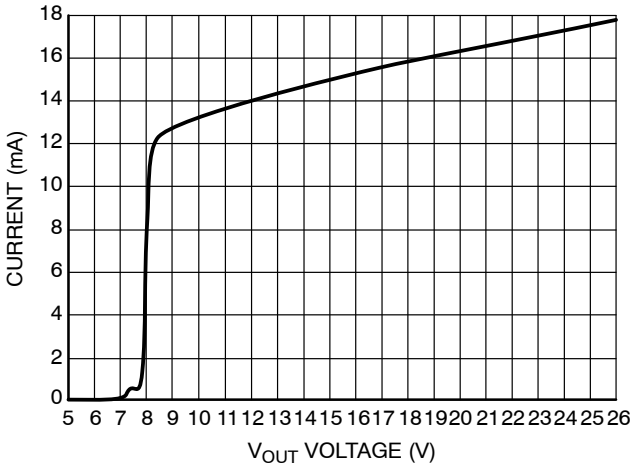


Figure 21. V_{OUT} Short to Battery

Switched Application

The NCV8184 has been designed for use in systems where the reference voltage on the V_{REF}/ENABLE pin is continuously on. Typically, the current into the V_{REF}/ENABLE pin will be less than 1.0 μA when the voltage on the V_{IN} pin (usually the ignition line) has been switched out (V_{IN} can be at high impedance or at ground.) Reference Figure 22.

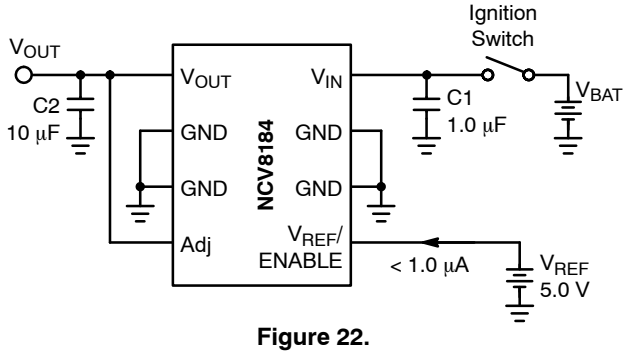


Figure 22.

External Capacitors

The output capacitor for the NCV8184 is required for stability. Without it, the regulator output will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst−case is determined at the minimum ambient temperature and maximum load expected.

The output capacitor can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitor must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to −40°C, a capacitor rated at that temperature must be used.

More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, “Compensation for Linear Regulators,” document number SR003AN/D, available through our website at http://www.onsemi.com.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 23) is:

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT(min)}\} I_{OUT(max)} + V_{IN(max)} I_Q \quad \text{(eq. 1)}$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current, for the application,and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of PD(max) is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the Package Thermal Data Section of the data sheet. Those packages with $R_{\theta JA}$’s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.

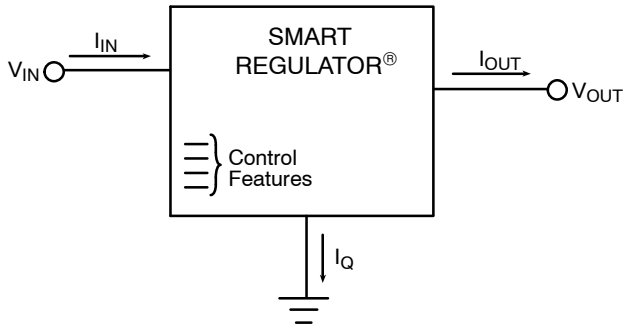


Figure 23. Single Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heatsink manufacturers.

PACKAGE THERMAL DATA

Parameter	Conditions Typical Value				Units
	100 mm² Spreader Board		645 mm² Spreader Board		
SOIC−8 Package	1 oz	2 oz	1 oz	2 oz	
Junction−to−Pin 6 (Ψ−JL6, Ψ_{JL6})	53	51	50	47	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	151	135	111	100	°C/W

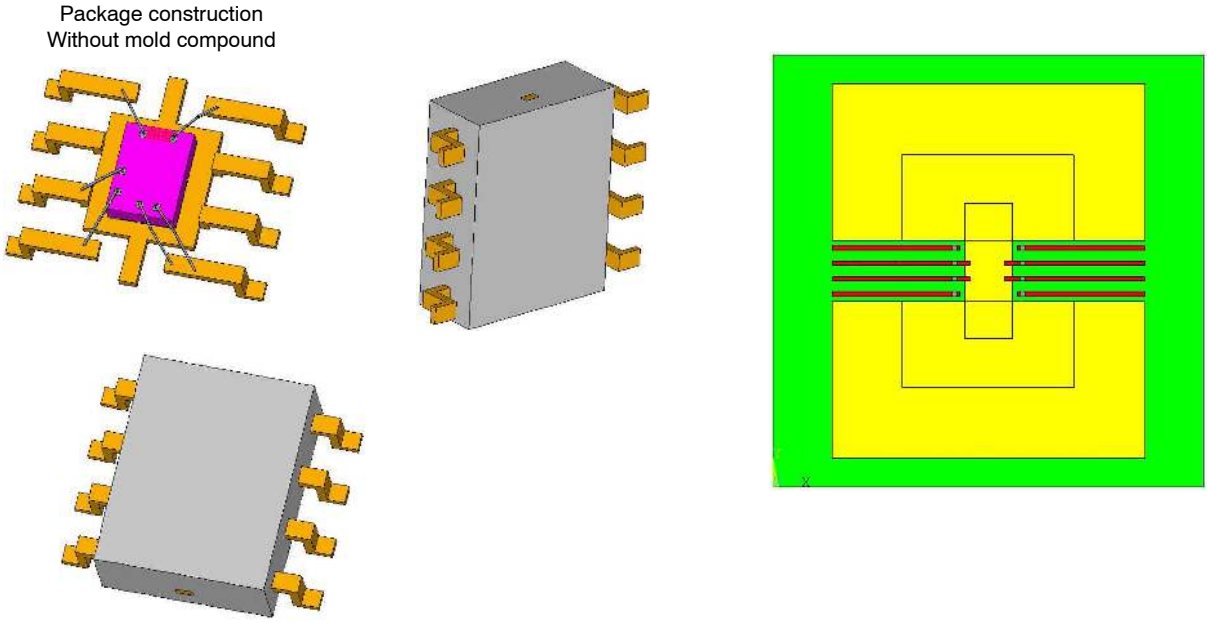


Figure 24. PCB Layout and Package Construction for Simulation

Table 1. SOIC−8 THERMAL RC NETWORK MODELS*

Copper Area (1 oz thick)			100 mm²	645 mm²		100 mm²	645 mm²	
			Cauer Network			Foster Network		
			100 mm²	645 mm²	Units	Tau	Tau	Units
C_C1	**Junction**	**Gnd**	**0.0000015**	**0.0000015**	W−s/C	**1.00E-06**	**1.00E-06**	sec
C_C2	**node1**	**Gnd**	**0.0000059**	**0.0000059**	W−s/C	**1.00E-05**	**1.00E-05**	sec
C_C3	**node2**	**Gnd**	**0.0000171**	**0.0000171**	W−s/C	**1.00E-04**	**1.00E-04**	sec
C_C4	node3	Gnd	0.0001340	0.0001340	W−s/C	1.76E-04	1.76E-04	sec
C_C5	node4	Gnd	0.0001322	0.0001323	W−s/C	0.0010	0.0010	sec
C_C6	node5	Gnd	0.0010797	0.0010811	W−s/C	0.008	0.008	sec
C_C7	node6	Gnd	0.0087127	0.0087918	W−s/C	0.150	0.150	sec
C_C8	node7	Gnd	0.0863882	0.0950421	W−s/C	3.00	3.00	sec
C_C9	node8	Gnd	0.3109255	1.0127094	W−s/C	8.96	5.15	sec
C_C10	node9	Gnd	0.8359004	1.5167041	W−s/C	52.5	68.4	sec
			100 mm²	**645 mm²**		**R's**	**R's**	
R_R1	**Junction**	**node1**	**0.8380955**	**0.8380935**	°C/W	**0.49519**	**0.49519**	°C/W
R_R2	**node1**	**node2**	**1.9719907**	**1.9719679**	°C/W	**1.070738**	**1.070738**	°C/W
R_R3	**node2**	**node3**	**5.0213740**	**5.0211819**	°C/W	**3.385971**	**3.385971**	°C/W
R_R4	**node3**	**node4**	**3.1295806**	**3.1288061**	°C/W	**1.617537**	**1.617537**	°C/W
R_R5	node4	node5	3.2483544	3.2468794	°C/W	5.10	5.10	°C/W
R_R6	node5	node6	6.5922506	6.5781209	°C/W	7.00	7.00	°C/W
R_R7	node6	node7	16.5499898	16.2818051	°C/W	15.00	15.00	°C/W
R_R8	node7	node8	45.3838437	34.7292748	°C/W	20.00	20.00	°C/W
R_R9	node8	node9	32.8928798	7.6862725	°C/W	28.19863	16.67727	°C/W
R_R10	node9	gnd	37.5059686	24.4060143	°C/W	71.26626	33.54171	°C/W

*Bold face items in the tables above represent the package without the external thermal system.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

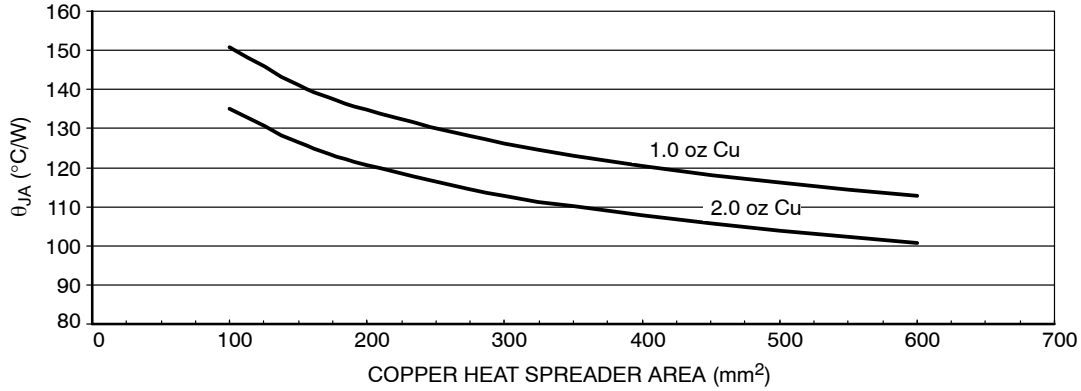


Figure 25. SOIC−8, θ_{JA} as a Function of the Pad Copper Area, Board Material FR4

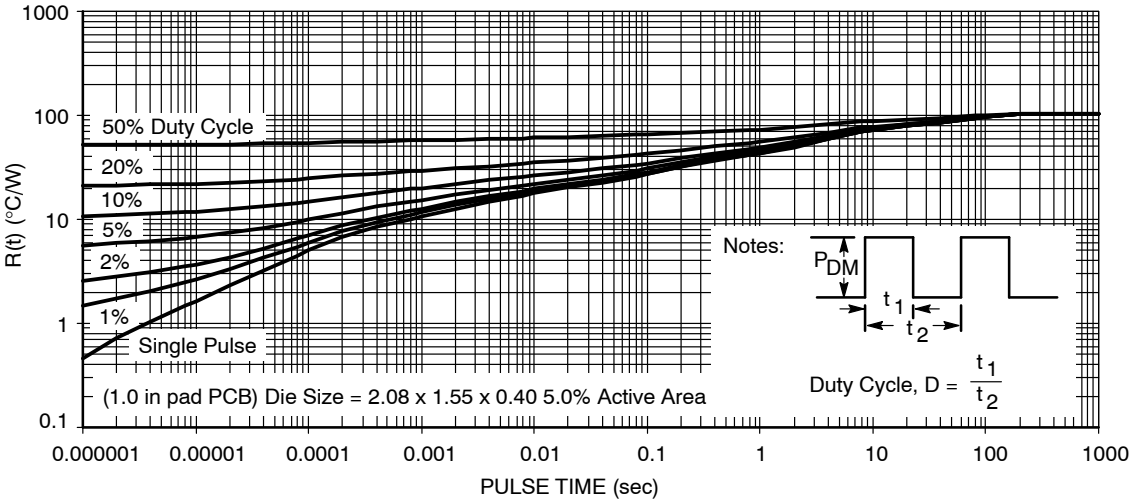


Figure 26. SOIC−8 Thermal Duty Cycle Curves on 1.0 in Spreader Test Board, 1.0 oz Cu

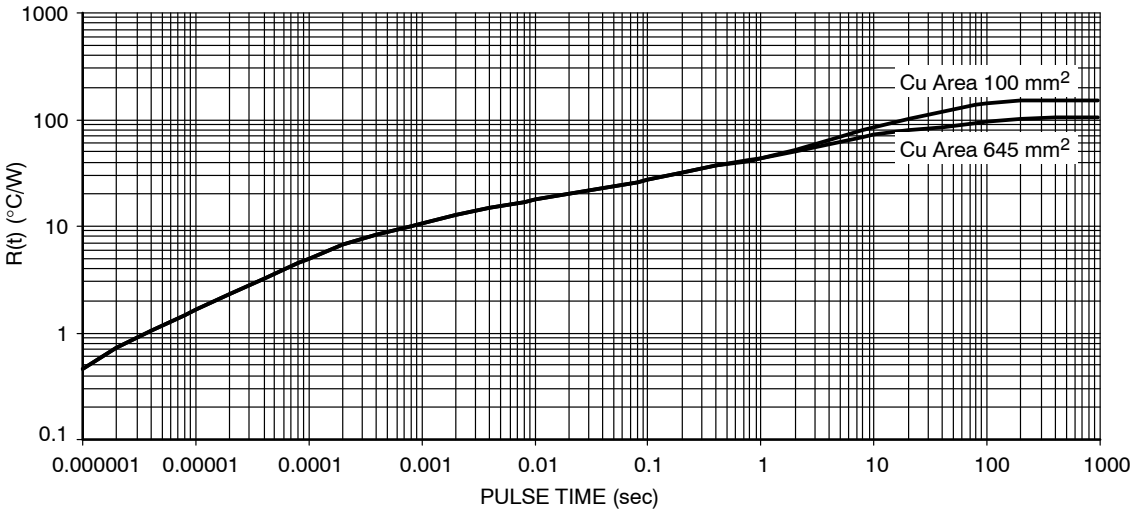


Figure 27. SOIC−8 Single Pulse Heating Curve

PACKAGE THERMAL DATA

Parameter	Conditions Typical Value				Units
	100 mm² Spreader Board		645 mm² Spreader Board		
SOIC−8 EP Package	1 oz	2 oz	1 oz	2 oz	
Junction−to−Board (Ψ−JB, Ψ_{JB})	26	26	26	25	°C/W
Junction−to−Pin 6 (tab) (Ψ−JL6, Ψ_{JL6})	48	45	37	34	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	140	123	88	78	°C/W

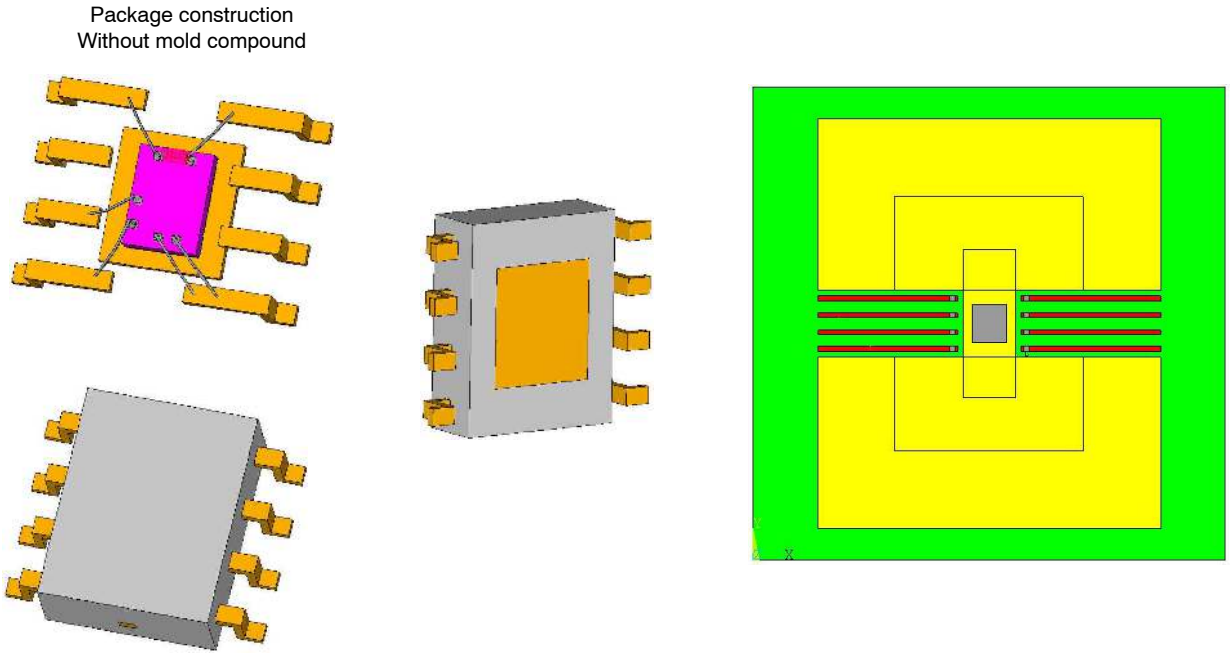


Figure 28. PCB Layout and Package Construction for Simulation

Table 2. SOIC−8 EP THERMAL RC NETWORK MODELS*

Drain Copper Area (1 oz thick)			100 mm²	645 mm²		100 mm²	645 mm²	
(SPICE Deck Format)			Cauer Network			Foster Network		
			100 mm²	645 mm²	Units	Tau	Tau	Units
C_C1	**Junction**	**Gnd**	**0.0000015**	**0.0000015**	W−s/C	**1.00E-06**	**1.00E-06**	sec
C_C2	**node1**	**Gnd**	**0.0000059**	**0.0000059**	W−s/C	**1.00E-05**	**1.00E-05**	sec
C_C3	**node2**	**Gnd**	**0.0000171**	**0.0000172**	W−s/C	**1.00E-04**	**1.00E-04**	sec
C_C4	node3	Gnd	0.0001359	0.0001360	W−s/C	1.76E-04	1.76E-04	sec
C_C5	node4	Gnd	0.0001349	0.0001352	W−s/C	0.0010	0.0010	sec
C_C6	node5	Gnd	0.0011157	0.0011253	W−s/C	0.008	0.008	sec
C_C7	node6	Gnd	0.0110409	0.0118562	W−s/C	0.150	0.150	sec
C_C8	node7	Gnd	0.0963225	0.2080891	W−s/C	3.00	3.00	sec
C_C9	node8	Gnd	0.3406538	1.1005982	W−s/C	9.11	5.12	sec
C_C10	node9	Gnd	0.9202956	0.8512155	W−s/C	52.1	68.6	sec
			100 mm²	**645 mm²**		**R's**	**R's**	
R_R1	**Junction**	**node1**	**0.8378620**	**0.8378491**	°C/W	**0.49519**	**0.49519**	°C/W
R_R2	**node1**	**node2**	**1.9693564**	**1.9692100**	°C/W	**1.070738**	**1.070738**	°C/W
R_R3	**node2**	**node3**	**5.0005397**	**4.9993083**	°C/W	**3.385971**	**3.385971**	°C/W
R_R4	**node3**	**node4**	**3.0695514**	**3.0646169**	°C/W	**1.617537**	**1.617537**	°C/W
R_R5	node4	node5	3.1989711	3.1895109	°C/W	5.030483	5.030483	°C/W
R_R6	node5	node6	6.2274239	6.1397875	°C/W	7.00	7.00	°C/W
R_R7	node6	node7	13.5796441	11.9712961	°C/W	12.00	12.00	°C/W
R_R8	node7	node8	40.4842477	18.5111622	°C/W	17.676107	7.880592	°C/W
R_R9	node8	node9	30.5112160	10.0330297	°C/W	25.169021	8.550583	°C/W
R_R10	node9	gnd	33.6034987	27.3017101	°C/W	65.037264	40.98639	°C/W

*Bold face items in the tables above represent the package without the external thermal system.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

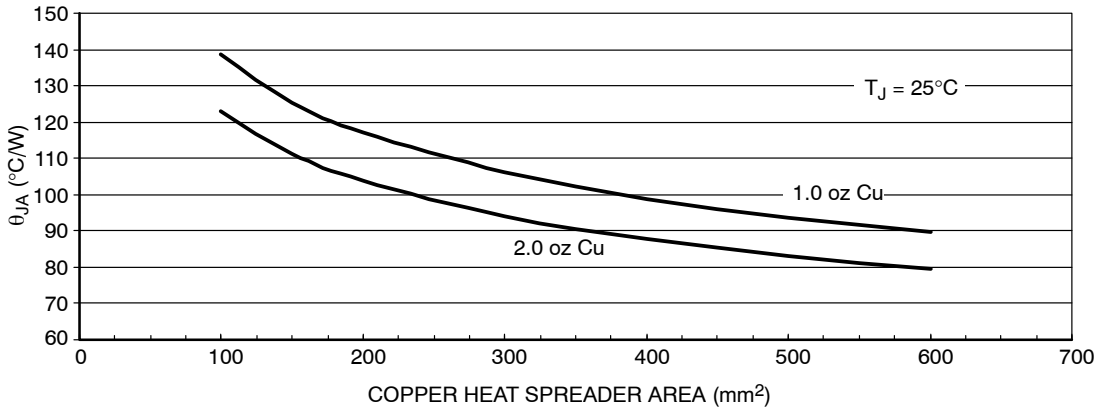


Figure 29. SOIC–8 Exposed Pad, θ_{JA} as a Function of the Pad Copper Area, Board Material FR4

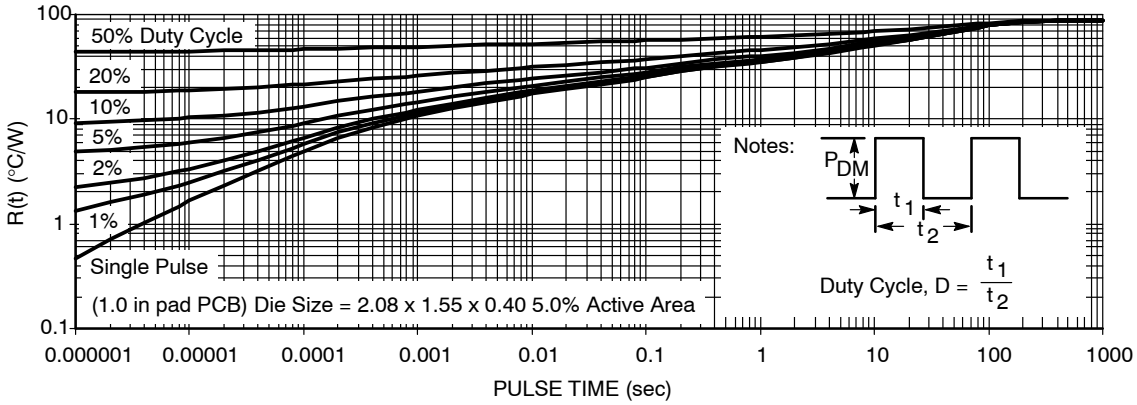


Figure 30. SOIC–8 Exposed Pad Thermal Duty Cycle Curves on 1.0 in Spreader Test Board, 1.0 oz Cu

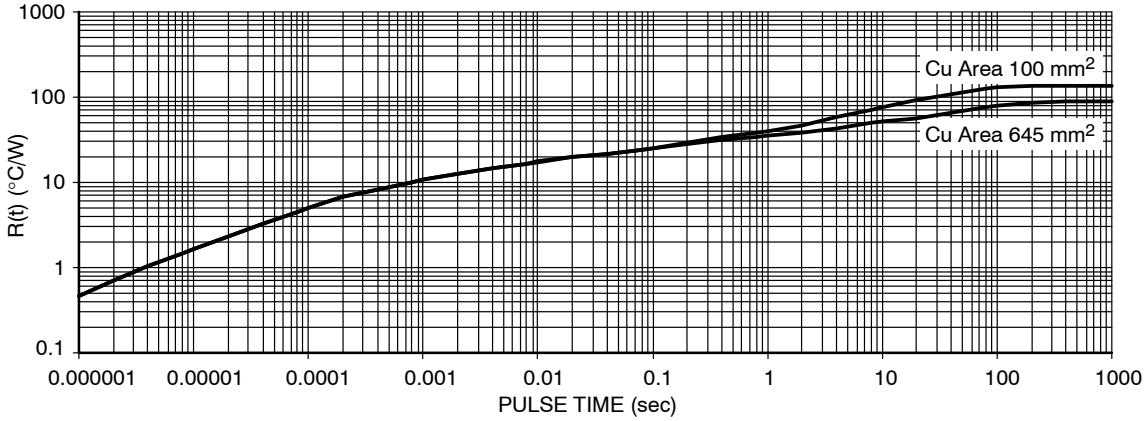


Figure 31. SOIC–8 Exposed Pad Single Pulse Heating Curve

PACKAGE THERMAL DATA

Parameter	Conditions Typical Value				Units
	100 mm² Spreader Board		645 mm² Spreader Board		
DPAK 5−LEAD Package	1 oz	2 oz	1 oz	2 oz	
Junction−to−Board-top (Ψ−JB, Ψ_{JB})	18	18	17	16	°C/W
Junction−to−Pin 3 (tab) (Ψ−JL3, Ψ_{JL3})	16	16	16	16	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	87	77	62	55	°C/W

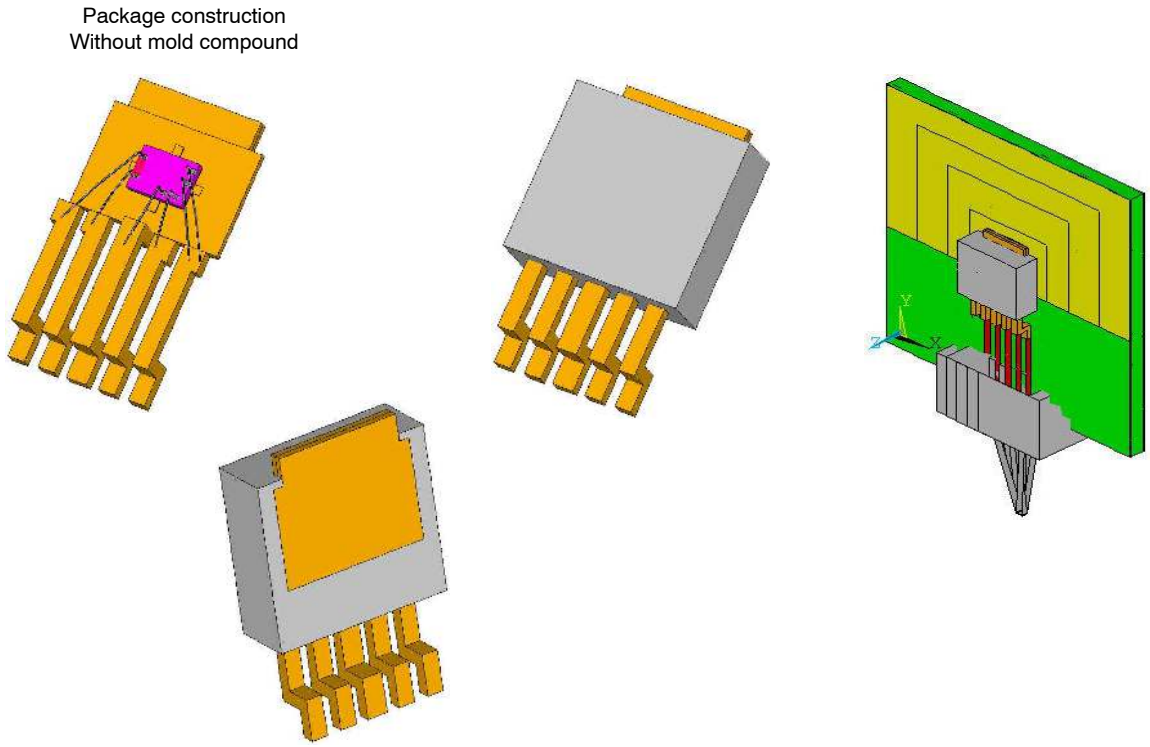


Figure 32. PCB Layout and Package Construction for Simulation

Table 3. DPAK 5−LEAD THERMAL RC NETWORK MODELS*

Drain Copper Area (1 oz thick)			100 mm²	645 mm²		100 mm²	645 mm²	
(SPICE Deck Format)			Cauer Network			Foster Network		
			100 mm²	645 mm²	Units	Tau	Tau	Units
C_C1	**Junction**	**Gnd**	**0.0000016**	**0.0000016**	W−s/C	**1.00E-06**	**1.00E-06**	sec
C_C2	**node1**	**Gnd**	**0.0000060**	**0.0000060**	W−s/C	**1.00E-05**	**1.00E-05**	sec
C_C3	**node2**	**Gnd**	**0.0000177**	**0.0000177**	W−s/C	**1.00E-04**	**1.00E-04**	sec
C_C4	**node3**	**Gnd**	**0.0001586**	**0.0001587**	W−s/C	**1.76E-04**	**1.76E-04**	sec
C_C5	node4	Gnd	0.0001927	0.0001931	W−s/C	0.0010	0.0010	sec
C_C6	node5	Gnd	0.0056684	0.0058019	W−s/C	0.030	0.030	sec
C_C7	node6	Gnd	0.0832719	0.1225791	W−s/C	0.285	0.299	sec
C_C8	node7	Gnd	0.1125429	0.3555671	W−s/C	3.00	3.00	sec
C_C9	node8	Gnd	0.5161495	1.2959188	W−s/C	9.03	11.80	sec
C_C10	node9	Gnd	1.4600223	1.8396650	W−s/C	55.2	79.0	sec
			100 mm²	**645 mm²**		**R's**	**R's**	
R_R1	**Junction**	**node1**	**0.8287213**	**0.8287120**	°C/W	**0.490938**	**0.490938**	°C/W
R_R2	**node1**	**node2**	**1.9304163**	**1.9303119**	°C/W	**1.061544**	**1.061544**	°C/W
R_R3	**node2**	**node3**	**4.7751915**	**4.7743247**	°C/W	**3.356895**	**3.356895**	°C/W
R_R4	**node3**	**node4**	**2.3736457**	**2.3705112**	°C/W	**1.606314**	**1.606314**	°C/W
R_R5	node4	node5	2.0679537	2.0623650	°C/W	5.00	5.00	°C/W
R_R6	node5	node6	5.3364094	5.1102633	°C/W	5.00	5.00	°C/W
R_R7	node6	node7	6.0331860	3.2428679	°C/W	2.00	2.00	°C/W
R_R8	node7	node8	22.7616126	8.6995800	°C/W	9.147005	5.071663	°C/W
R_R9	node8	node9	17.9894079	16.1165074	°C/W	17.23178	3.646957	°C/W
R_R10	node9	gnd	22.7199543	16.7871407	°C/W	41.92202	34.68827	°C/W

*Bold face items in the tables above represent the package without the external thermal system.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

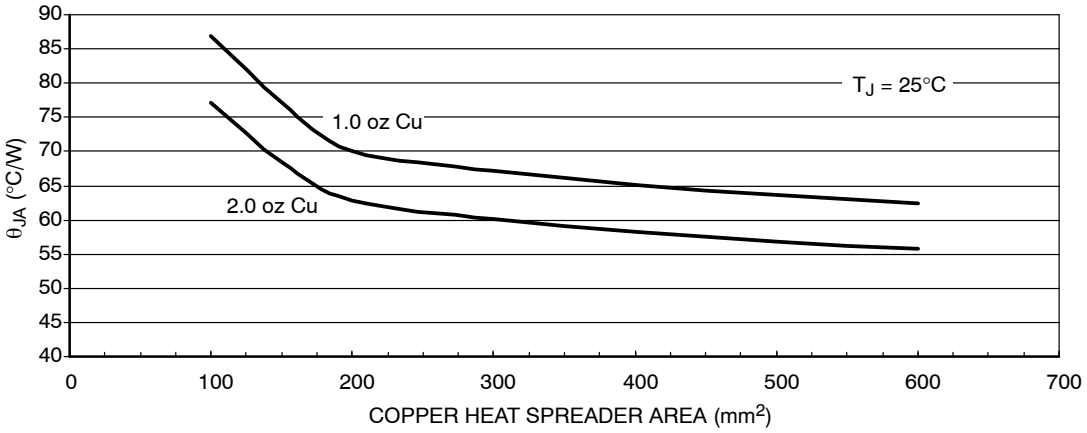


Figure 33. DPAK 5−Lead, θ_{JA} as a Function of the Pad Copper Area, Board Material FR4

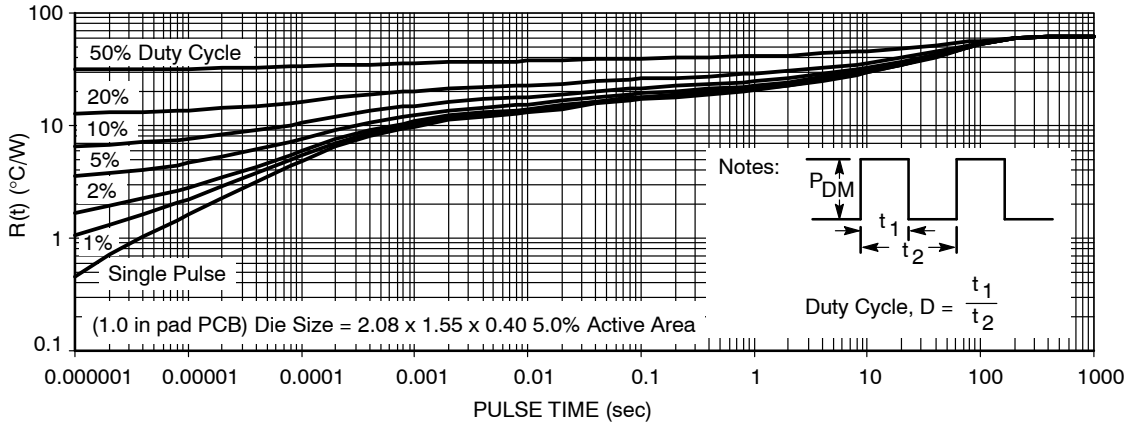


Figure 34. DPAK 5−Lead Thermal Duty Cycle Curves on 1.0 in Spreader Test Board, 1.0 oz Cu

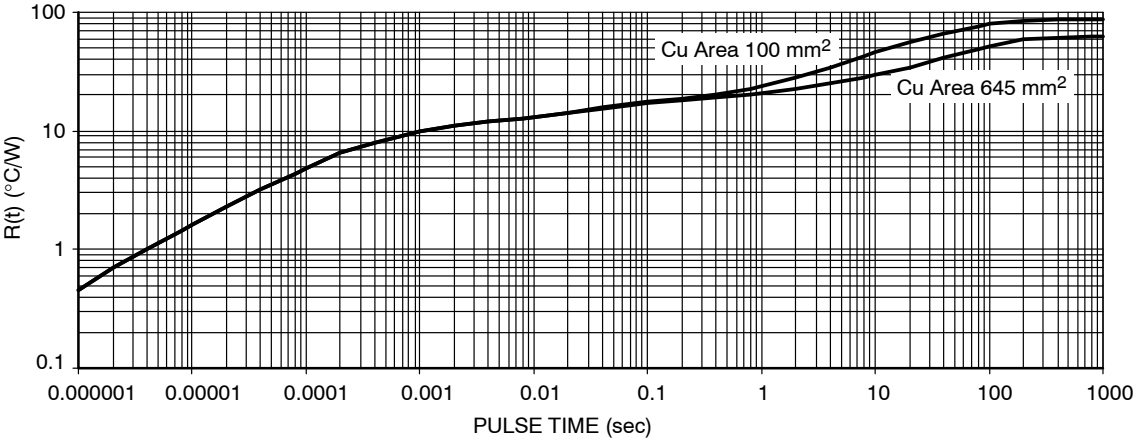


Figure 35. DPAK 5−Lead Single Pulse Heating Curve

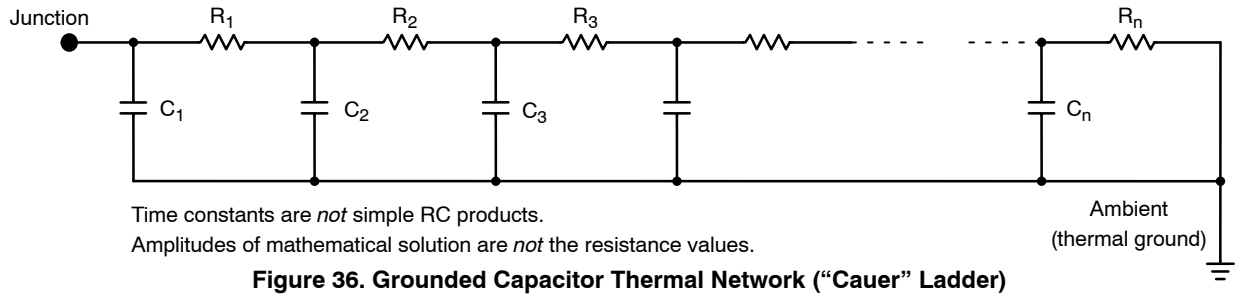


Figure 36. Grounded Capacitor Thermal Network (“Cauer” Ladder)

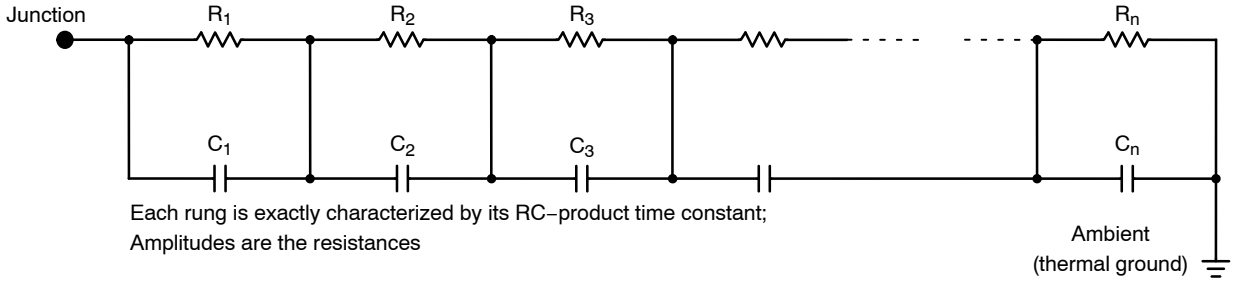


Figure 37. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)

ORDERING INFORMATION

Device Order Number	Package Type	Shipping†
NCV8184DG	SOIC−8 (Pb−Free)	98 Units / Tube
NCV8184DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV8184DTRKG	DPAK (Pb−Free)	2500 / Tape & Reel
NCV8184PDG	SOIC−8 epad (Pb−Free)	98 Units / Tube
NCV8184PDR2G	SOIC−8 epad (Pb−Free)	2500 / Tape & Reel

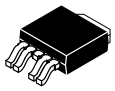
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

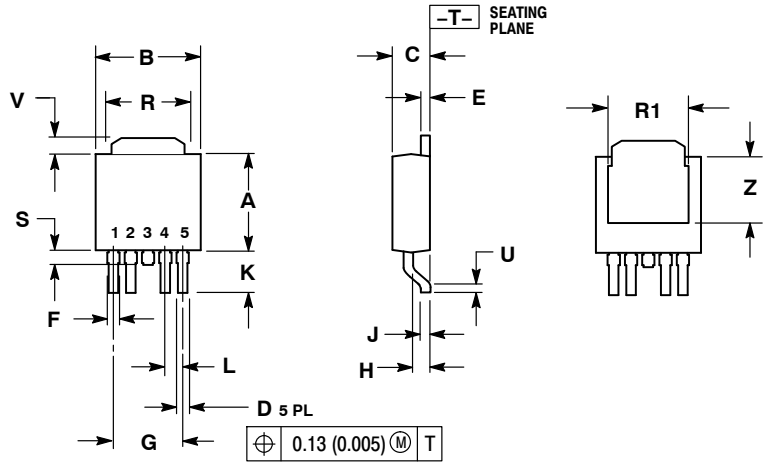
ON Semiconductor®

DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

DATE 15 MAY 2014



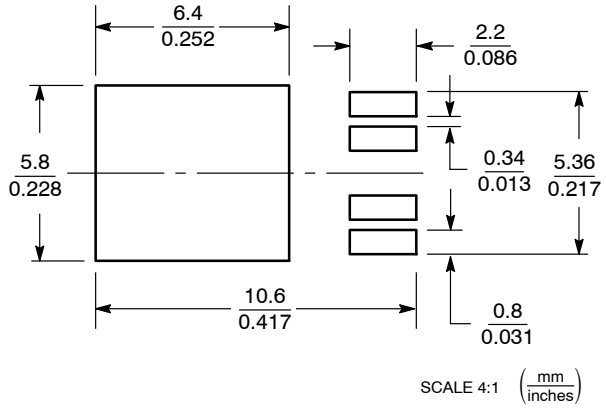
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

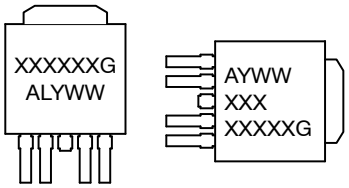
RECOMMENDED SOLDERING FOOTPRINT*



SCALE 4:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

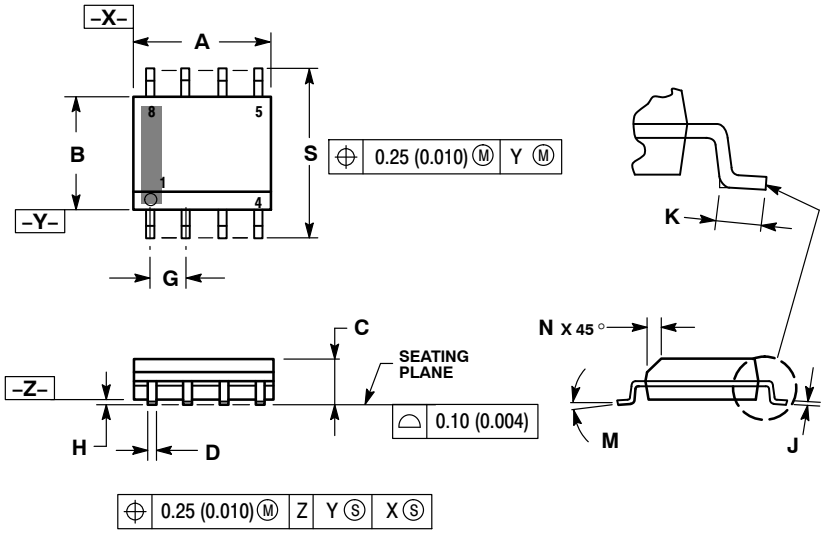
DOCUMENT NUMBER:	**98AON12855D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DPAK−5 CENTER LEAD CROP**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

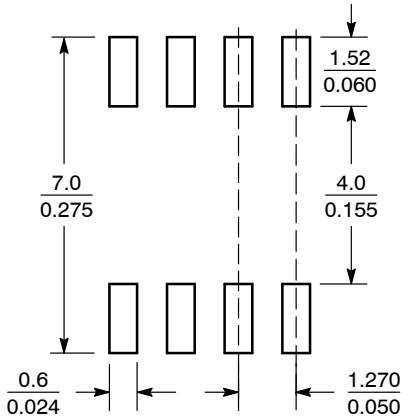
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

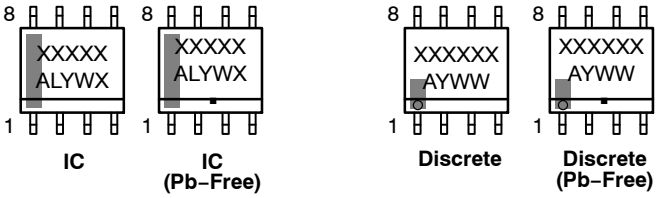
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | **IC (Pb−Free)** | **Discrete** | **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

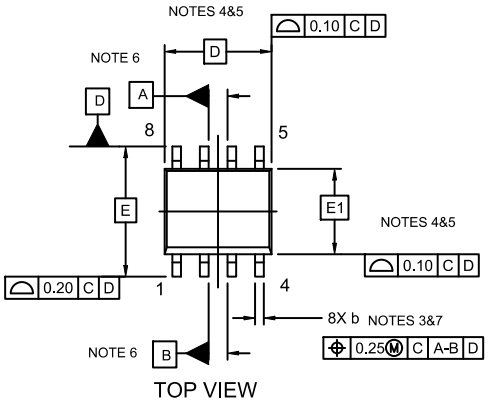
SCALE 1:1

SOIC−8 EP
CASE 751AC
ISSUE E

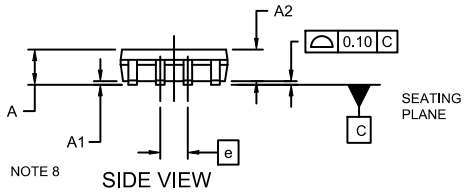
DATE 05 OCT 2022

NOTES:

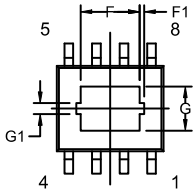
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



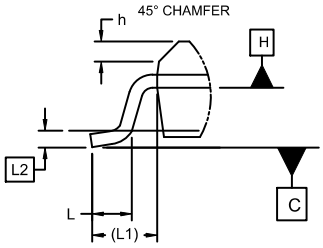
TOP VIEW



SIDE VIEW

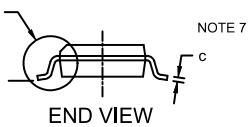


BOTTOM VIEW

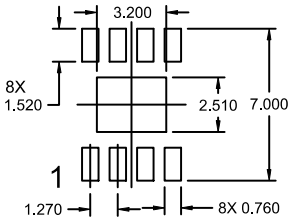


DETAIL A

DETAIL A



END VIEW

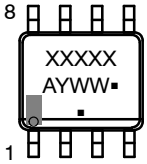


RECOMMENDED
MOUNTING FOOTPRINT*

DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	---	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1		0.20 REF	
G	1.55	2.03	2.51
G1		0.46 REF	
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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