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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR NP60N055KUG

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP60N055KUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance

 $R_{DS(on)} = 9.4 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, \text{ ID} = 30 \text{ A})$

• Low Ciss: Ciss = 3700 pF TYP.

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGs = 0 V)	VDSS	55	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	D(DC)	±60	А
Drain Current (pulse) Note1	D(pulse)	±240	А
Total Power Dissipation (T _A = 25°C)	Pt1	1.8	W
Total Power Dissipation (Tc = 25°C)	Pt2	88	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	–55 to +175	°C
Repetitive Avalanche Current Note2	lar	27	Α
Repetitive Avalanche Energy Note2	Ear	73	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Tch < 150°C, VDD = 28 V, RG = 25 Ω , VGS = 20 \rightarrow 0 V

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	1.70	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W

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ORDERING INFORMATION

PART NUMBER	PACKAGE
NP60N055KUG	TO-263 (MP-25ZK)



(TO-263)

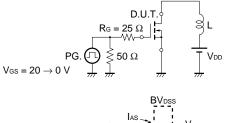
ELECTRICAL CHARACTERISTICS (TA = 25°C)

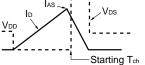
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 55 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	lgss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	Vos = Vgs, Id = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance Note	y _{fs}	Vds = 10 V, Id = 30 A	11	22		S
Drain to Source On-state Resistance Note	RDS(on)	Vgs = 10 V, Id = 30 A		7.4	9.4	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V		3700	5600	pF
Output Capacitance	Coss	V _{GS} = 0 V		270	410	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		160	290	pF
Turn-on Delay Time	td(on)	V _{DD} = 28 V, I _D = 30 A		30	66	ns
Rise Time	tr	V _{GS} = 10 V		44	110	ns
Turn-off Delay Time	td(off)	R _G = 0 Ω		79	160	ns
Fall Time	tr			8	20	ns
Total Gate Charge	QG	V _{DD} = 44 V		61	92	nC
Gate to Source Charge	QGS	V _{GS} = 10 V		14		nC
Gate to Drain Charge	Qgd	I _D = 60 A		20		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 60 A, VGS = 0 V		0.94	1.5	V
Reverse Recovery Time	trr	IF = 60 A, VGS = 0 V		38		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>µ</i> s		41		nC

Note Pulsed

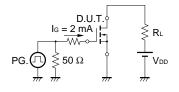
TEST CIRCUIT 1 AVALANCHE CAPABILITY

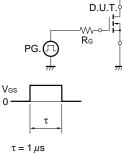
TEST CIRCUIT 2 SWITCHING TIME



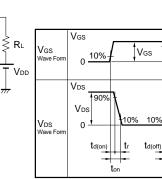


TEST CIRCUIT 3 GATE CHARGE





 $\tau = 1 \,\mu s$ Duty Cycle $\leq 1\%$



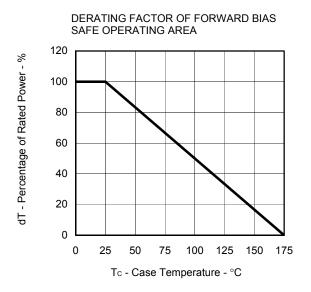
90%

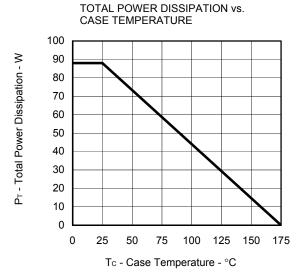
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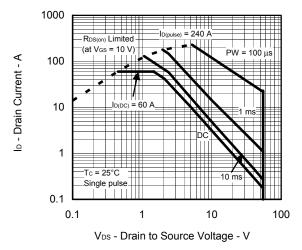
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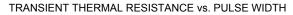
TYPICAL CHARACTERISTICS (TA = 25^{\circ}C)

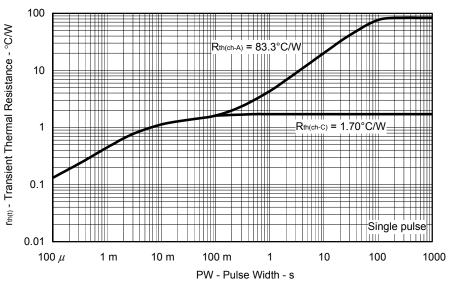


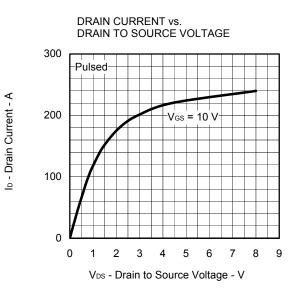


FORWARD BIAS SAFE OPERATING AREA

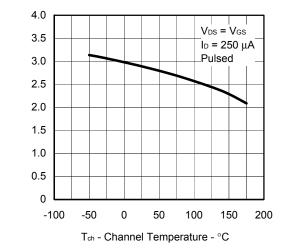




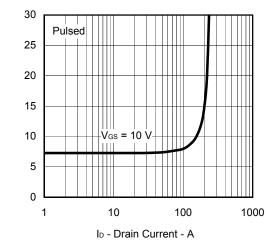




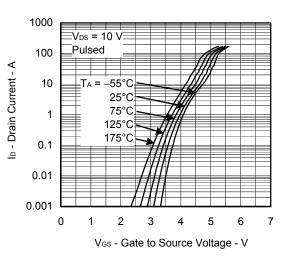
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



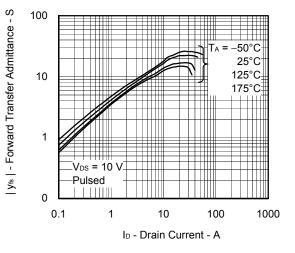
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



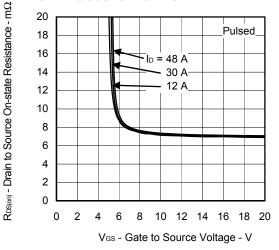




FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



 $R_{\text{DS}(\text{on})}$ - Drain to Source On-state Resistance - $m\Omega$

V_{GS(th)} - Gate to Source Threshold Voltage - V

Cis

Crss

100

10

8

6

4

2

0

70

ID = 60 A

60

Pulsed

V_{GS} - Gate to Source Voltage - V

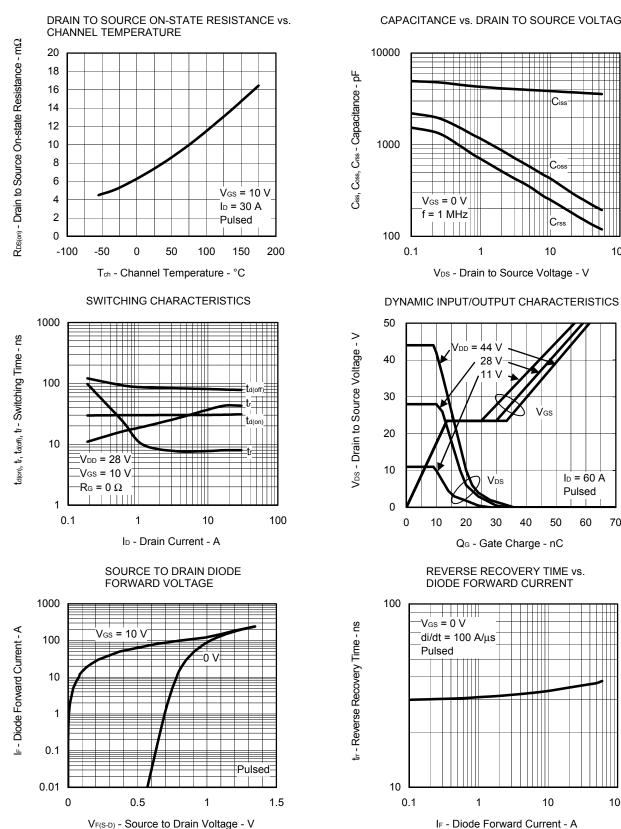
10

Vgs

40

50

10

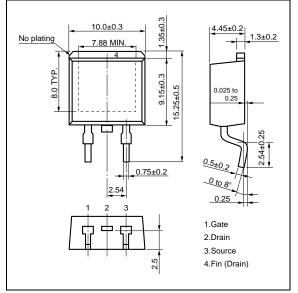


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

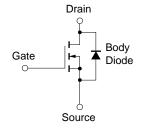
100

PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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