

SN74CBT3861 10-BIT FET BUS SWITCH

SCDS061D – APRIL 1998 – REVISED OCTOBER 2000

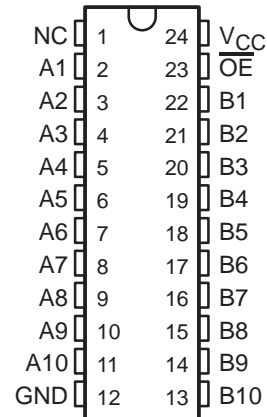
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17

description

The SN74CBT3861 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 10-bit switch with a single output-enable (\overline{OE}) input. When \overline{OE} is low, the switch is on, and port A is connected to port B. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

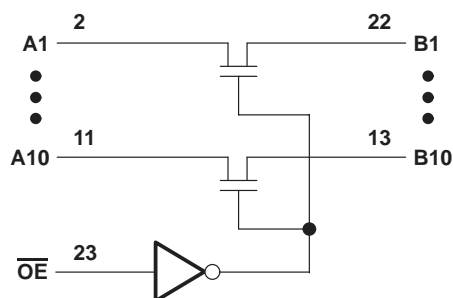
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74CBT3861DW	CBT3861
		Tape and reel	SN74CBT3861DWR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3861DBQR	CBT3861
	TSSOP – PW	Tape and reel	SN74CBT3861PWR	CU861
	TVSOP – DGV	Tape and reel	SN74CBT3861DGV	CU861

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN74CBT3861

10-BIT FET BUS SWITCH

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.2	V
I_I	$V_{CC} = 5.5$ V,	$V_I = 5.5$ V or GND			±1	µA
I_{CC}	$V_{CC} = 5.5$ V,	$I_O = 0$, $V_I = V_{CC}$ or GND			3	µA
ΔI_{CC} §	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	$V_I = 3$ V or 0			3	pF
$C_{io(OFF)}$	$V_O = 3$ V or 0,	$\overline{OE} = V_{CC}$			5	pF
r_{on} ¶	$V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V	$V_I = 2.4$ V,	$I_I = 15$ mA	14	22	Ω
		$V_I = 0$	$I_I = 64$ mA	5	7	
	$V_{CC} = 4.5$ V	$V_I = 0$	$I_I = 30$ mA	5	7	
		$V_I = 2.4$ V,	$I_I = 15$ mA	10	15	

‡ All typical values are at $V_{CC} = 5$ V (unless otherwise noted), $T_A = 25^\circ\text{C}$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

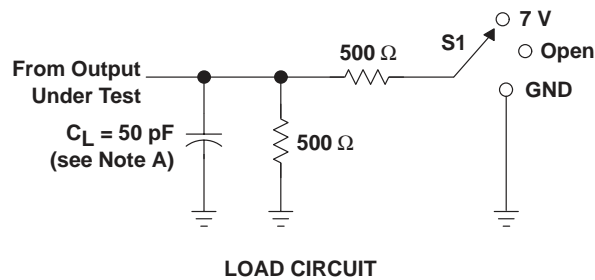


switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

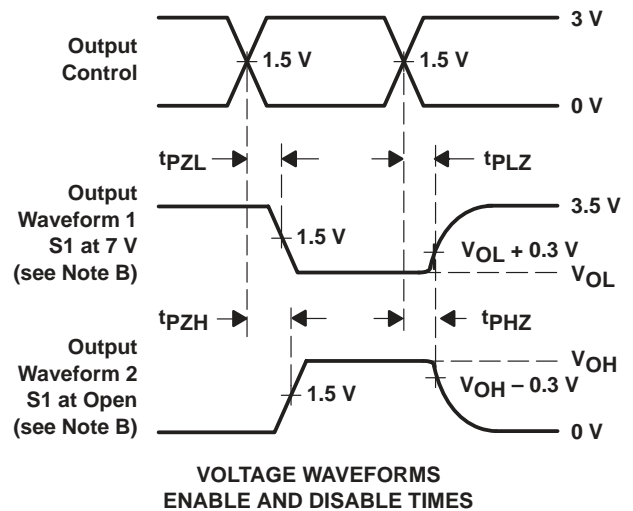
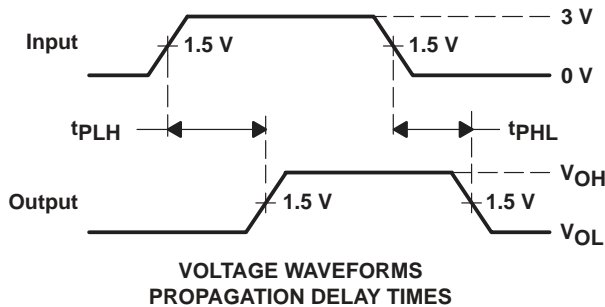
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} [†]	A or B	B or A	0.35		0.25		ns
t _{en}	$\overline{\text{OE}}$	A or B	8.1		3.8	7.5	ns
t _{dis}	$\overline{\text{OE}}$	A or B	6.3		3.4	6.6	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	7 V
t _{PHZ} /t _{PZH}	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.
 G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT3861DBQR	LIFEBUY	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3861	
SN74CBT3861DW	LIFEBUY	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3861	
SN74CBT3861DWR	LIFEBUY	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3861	
SN74CBT3861PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU861	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

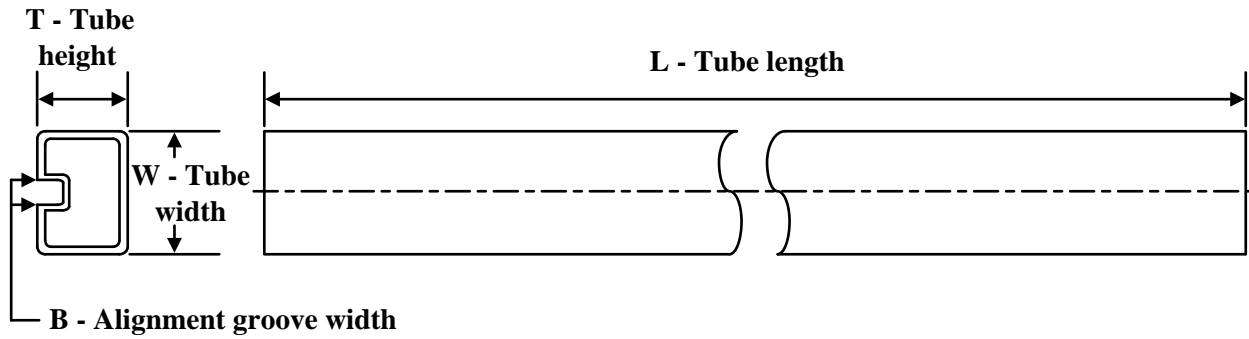

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3861DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBT3861DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBT3861PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3861DBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0
SN74CBT3861DWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74CBT3861PWR	TSSOP	PW	24	2000	356.0	356.0	35.0

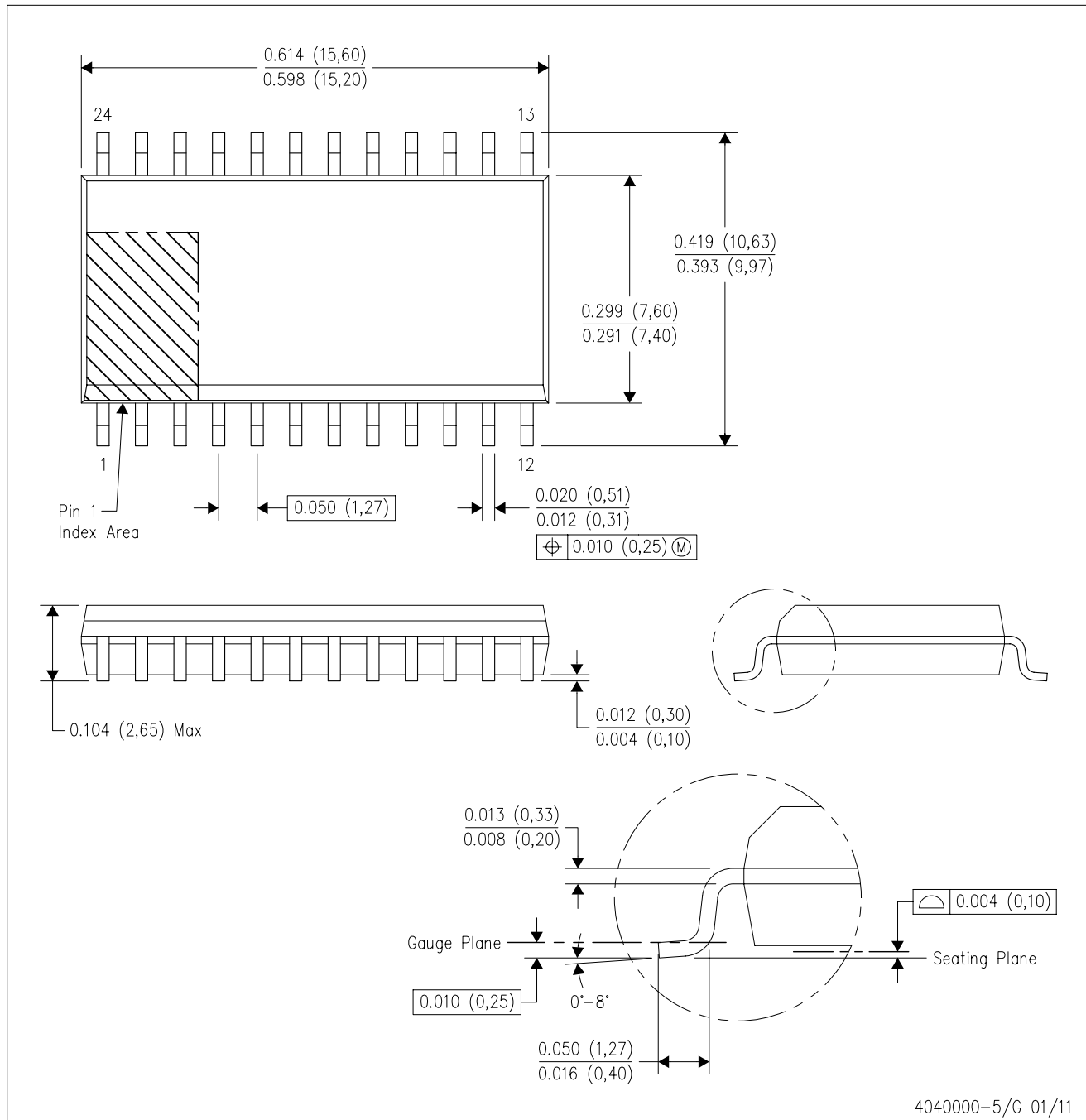
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT3861DW	DW	SOIC	24	25	506.98	12.7	4826	6.6

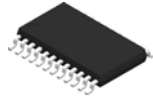
DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



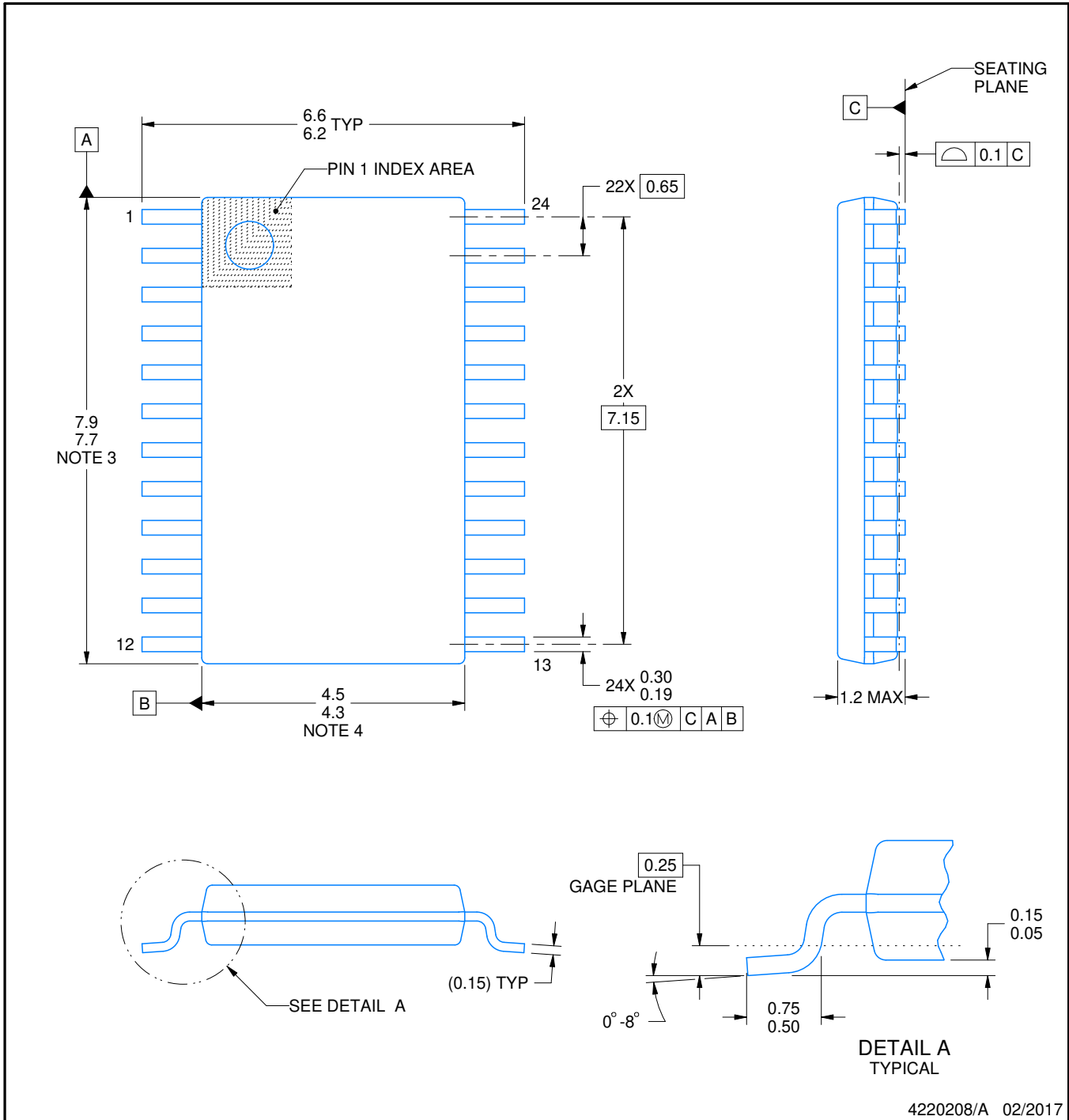
- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

PW0024A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

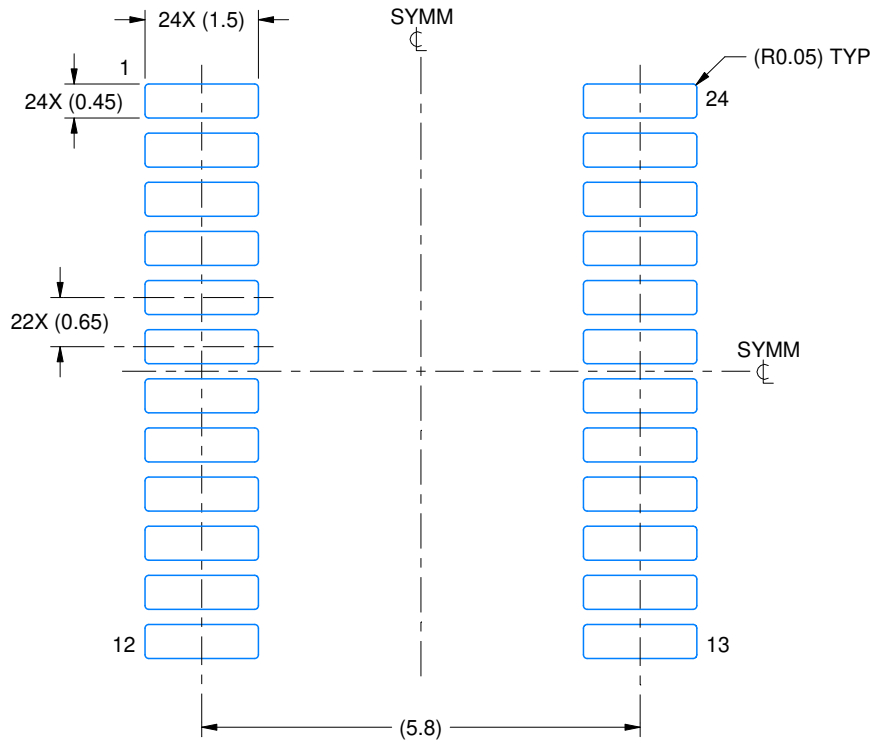
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

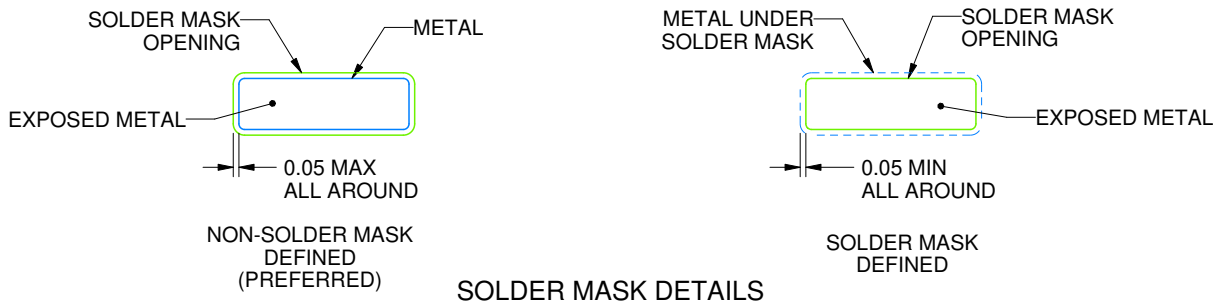
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

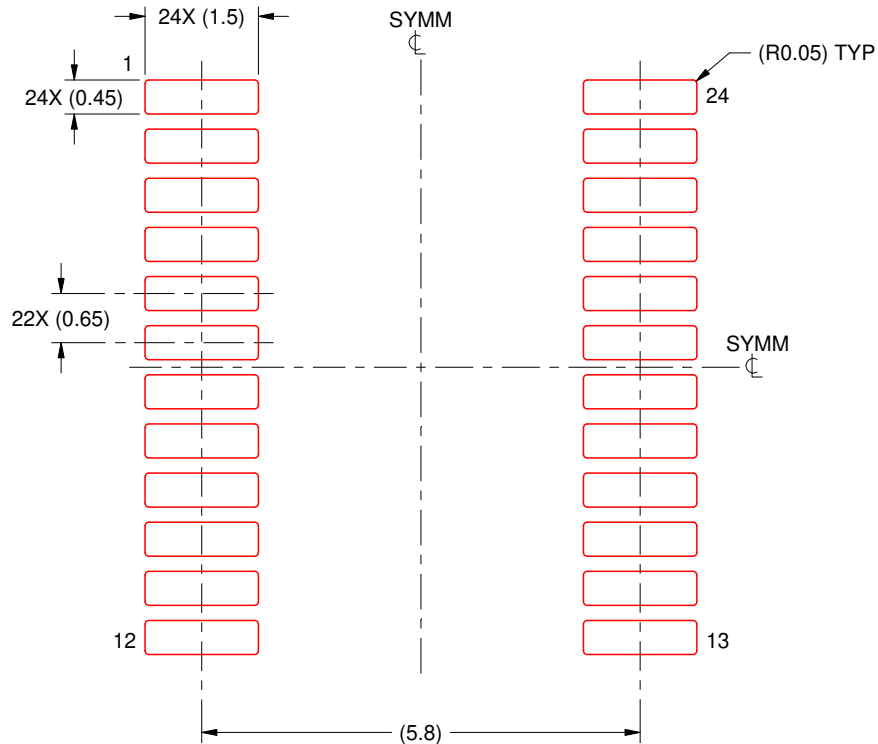
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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