- **Fully Supports Provisions of IEEE 1394-1995 Standard for High Performance Serial Bus† and the P1394a Supplement**
- **Fully Interoperable With FireWire™ and i.LINK™ Implementation of IEEE Std 1394**
- **Fully Compliant With OpenHCI Requirements**
- **Provides One P1394a Fully Compliant Cable Port at 100/200/400 Megabits per Second (Mbits/s)**
- **Full P1394a Support Includes: Connection Debounce, Arbitrated Short Reset, Multispeed Concatenation, Arbitration Acceleration, Fly-By Concatenation, Port Disable/Suspend/Resume**
- **Extended Resume Signaling for Compatibility With Legacy DV Devices**
- **Power-Down Features to Conserve Energy in Battery Powered Applications Include: Automatic Device Power-Down During Suspend, Device Power-Down Pin, Link Interface Disable via LPS, and Inactive Port Powered-Down**
- **Ultralow-Power Sleep Mode**
- **Node Power Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Cable Port Monitors Line Conditions for Active Connection to Remote Node**
- **Register Bits Give Software Control of Contender Bit, Power Class bits, Link Active Control Bit and P1394a Features**
- **Data Interface to Link-Layer Controller Through 2/4/8 Parallel Lines at 49.152 MHz**
- **Interface to Link Layer Controller Supports Low Cost TI Bus-Holder Isolation and Optional Annex J Electrical Isolation**
- **Interoperable With Link-Layer Controllers Using 3.3 V and 5 V Supplies**
- **Interoperable With Other PHYsical Layers (PHYs) Using 3.3 V and 5 V Supplies**
- **Low Cost 24.576-MHz Crystal Provides Transmit, Receive Data at 100/200/400 Mbits/s, and Link-Layer Controller Clock at 49.152 MHz**
- **Incoming Data Resynchronized to Local Clock**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data-Strobe Bit Level Encoding**
- **Single 3.3 Volt Supply Operation**
- **Meets Intel Mobile Power Guideline 2000**
- **Low Cost High Performance 64 Pin TQFP (PAP) Thermally Enhanced Package**

description

The TSB41LV01 provides the digital and analog transceiver functions needed to implement a two-port node in a cable-based IEEE 1394 network. The cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB41LV01 is designed to interface with a link layer controller (LLC), such as the TSB12LV22, TSB12LV21, TSB12LV23, TSB12LV31, TSB12LV41, TSB12LV42, or TSB12LV01A.

The TSB41LV01 requires only an external 24.576 MHz crystal as a reference. An external clock may be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216 MHz reference signal. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded strobe and data information. A 49.152 MHz clock signal is supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

FireWire is a trademark of Apple Computer, Incorporated.
i.LINK is a trademark of SONY.

description (continued)

The TSB41LV01 supports an optional isolation barrier between itself and its LLC. When the /ISO input terminal is tied high, the LLC interface outputs behave normally. When the /ISO terminal is tied low, internal differentiating logic is enabled, and the outputs are driven such that they can be coupled through a capacitive or transformer galvanic isolation barrier as described in Annex J of IEEE Std 1394-1995 and in the P1394a Supplement (section 5.9.4) (hereafter referred to as Annex J type isolation). To operate with TI Bus holder isolation the /ISO terminal on the PHY must be high.

Data bits to be transmitted through the cable port are received from the LLC on two, four or eight parallel paths (depending on the requested transmission speed) and are latched internally in the TSB41LV01 in synchronization with the 49.152 MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304, 196.608, or 393.216 Mbits/s (referred to as S100, S200, and S400 speed respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two, four or eight bit parallel streams (depending upon the indicated receive speed), resynchronized to the local 49.152 MHz system clock and sent to the associated LLC.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage.

The TSB41LV01 provides a 1.86 V nominal bias voltage at the TPBIAS terminal for port termination. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1 μF.

The line drivers in the TSB41LV01 operate in a high-impedance current mode, and are designed to work with external 112-Ω line-termination resistor networks in order to match the 110-Ω cable impedance. One network is provided at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair-B terminals is coupled to ground through a parallel R-C network with recommended values of 5 kΩ and 220 pF. The values of the external line termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. An external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents. This current setting resistor has a value of 6.3-kΩ ±0.5%. This may be accomplished by placing a 6.34-kΩ ±0.5% resistor in parallel with a 1-MΩ resistor.

When the power supply of the TSB41LV01 is 0 V while the twisted-pair cables are connected, the TSB41LV01 transmitter and receiver circuitry will present a high impedance to the cable and will not load the TPBIAS voltage at the other end of the cable.

The TESTM, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM terminal should be connected to V_{DD}, SE should be tied to ground through a 1-kΩ resistor, while SM should be connected directly to ground.

description (continued)

Four package terminals are used as inputs to set the default value for four configuration status bits in the self-ID packet, and are hardwired high or low as a function of the equipment design. The PC0–PC2 terminals are used to indicate the default power-class status for the node (the need for power from the cable or the ability to supply power to the cable). See Table 1 for power-class encoding. The C/LKON terminal is used as an input to indicate that the node is a contender for either isochronous resource manager (IRM) or bus manager (BM).

The TSB41LV01 supports suspend/resume as defined in the IEEE P1394a specification. The suspend mechanism allows pairs of directly-connected ports to be placed into a low power conservation state (suspended state) while maintaining a port-to-port connection between bus segments. While in the suspended state, a port is unable to transmit or receive data transaction packets. However, a port in the suspended state is capable of detecting connection status changes and detecting incoming TPBias. When the port of the TSB41LV01 is suspended all circuits except the bandgap reference generator and bias detection circuits are powered down, resulting in significant power savings. For additional details of suspend/resume operation refer to the P1394a specification. The use of suspend/resume is recommended for new designs.

The port transmitter and receiver circuitry is disabled during power down (when the PD input terminal is asserted high), during reset (when the $\overline{\text{RESET}}$ input terminal is asserted low), when no active cable is connected to the port, or when controlled by the internal arbitration logic. The TPBias output is disabled during power-down, during reset, or when the port is disabled as commanded by the LLC.

The CNA (cable-not-active) output terminal is asserted high when there are no twisted-pair cable ports receiving incoming bias (i.e., they are either disconnected or suspended), and can be used along with LPS to determine when to power down the TSB41LV01. The CNA output is not debounced. When the PD terminal is asserted high, the CNA detection circuitry is enabled (regardless of the previous state of the ports) and a pulldown is activated on the $\overline{\text{RESET}}$ terminal so as to force a reset of the TSB41LV01 internal logic.

The LPS (link power status) terminal works with the C/LKON terminal to manage the power usage in the node. The LPS signal from the LLC is used in conjunction with the LCtrl bit (see Table 4 and Table 5 in the Application Information section) to indicate the active/power status of the LLC. The LPS signal is also used to reset, disable, and initialize the PHY-LLC interface (the state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit).

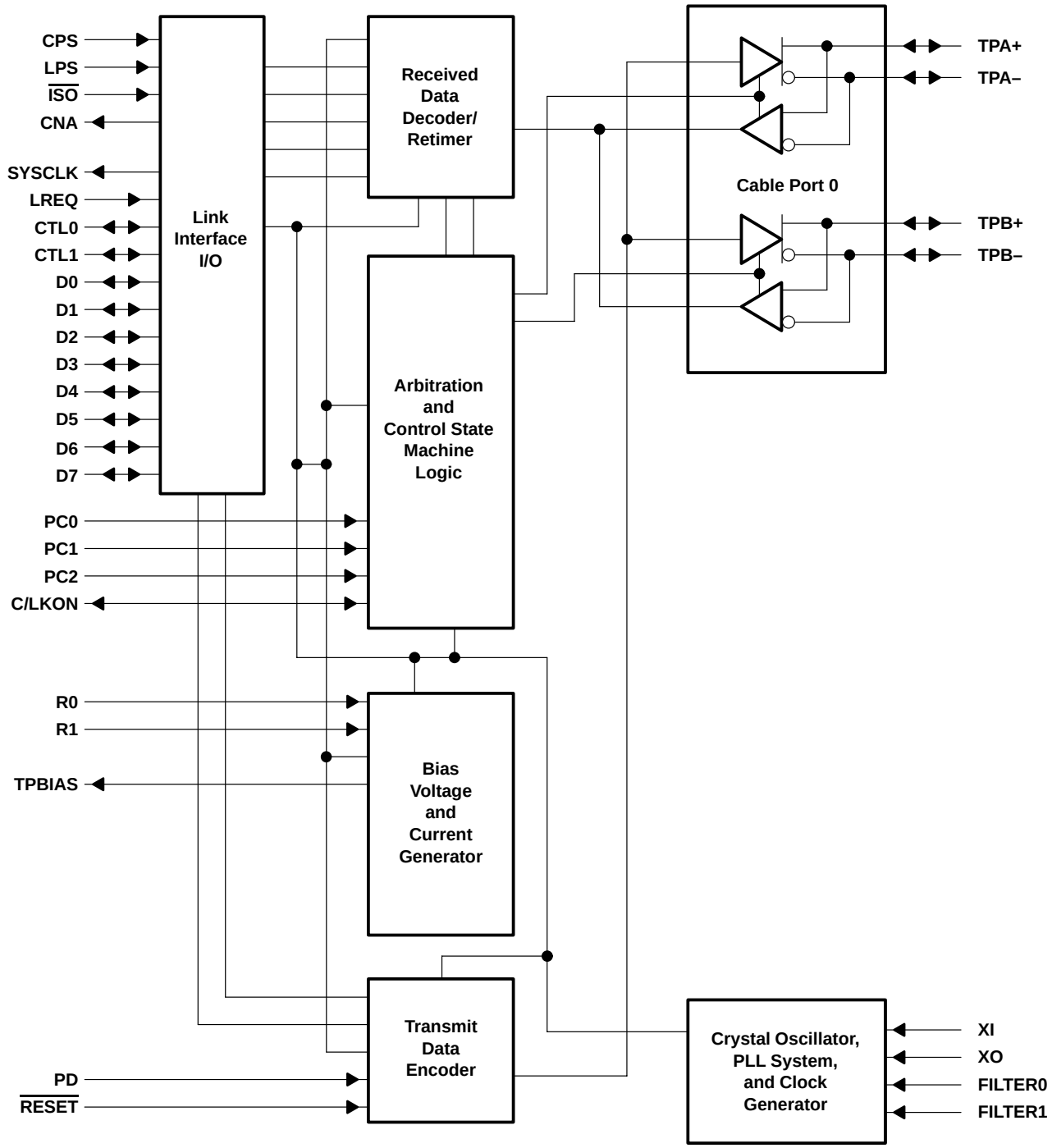
The LPS input is considered inactive if it remains low for more than 2.6 μs and is considered active otherwise. When the TSB41LV01 detects that LPS is inactive, it places the PHY-LLC interface into a low-power reset state in which the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than 26 μs, the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is also held in the disabled state during hardware reset. The TSB41LV01 continues the necessary repeater functions required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and LPS is again observed active, the PHY initializes the interface and return it to normal operation.

When the PHY-LLC interface in the low-power disabled state, the TSB41LV01 automatically enters a low-power mode if the port is inactive (disconnected, disabled, or suspended). In this low-power mode, the TSB41LV01 disables its internal clock generators and also disables various voltage and current reference circuits depending on the state of the port (some reference circuitry must remain active in order to detect new cable connections, disconnections, or incoming TPBias, for example). The lowest power consumption (the *ultralow-power sleep* mode) is attained when the port is either disconnected, or disabled with the port's interrupt enable bit cleared. The TSB41LV01 exits the low-power mode when the LPS input is asserted high or when a port event occurs which requires that the TSB41LV01 become active in order to respond to the event or to notify the LLC of the event (e.g., incoming bias is detected on a suspended port, a disconnection is detected on a suspended port, a new connection is detected on a nondisabled port, etc.). The SYSCLK output becomes active (and the PHY-LLC interface will be initialized and become operative) within 7.3 ms after LPS is asserted high when the TSB41LV01 is in the low-power mode.

description (continued)

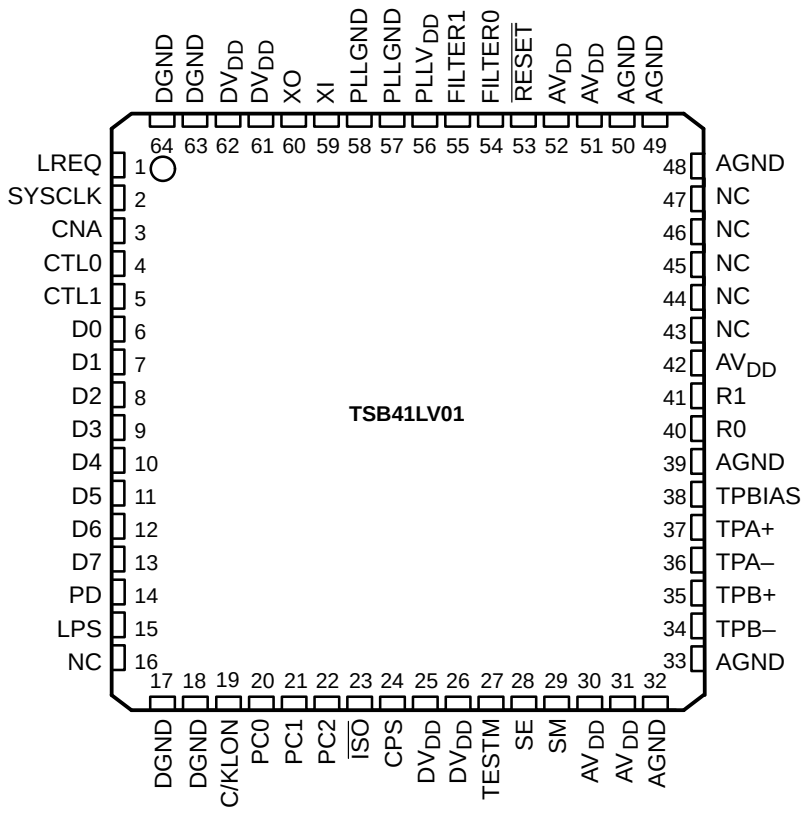
The PHY uses the C/LKON terminal to notify the LLC to power up and become active. When activated, the C/LKON signal is a square wave of approximately 163 ns period. The PHY activates the C/LKON output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as described above, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY deasserts the C/LKON output when the LLC becomes active (both LPS active and the LCtrl bit set to 1). The PHY also deasserts the C/LKON output when a bus-reset occurs unless a PHY interrupt condition exists which would otherwise cause C/LKON to be active.

functional block diagram



pin assignments

PAP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	32, 33, 39, 48, 49, 50	–	Analog circuit ground pins. These pins should be tied together to the low impedance circuit board ground plane.
AV_{DD}	30, 31, 42, 51, 52	–	Analog circuit power pins. A combination of high frequency decoupling capacitors near each pin is suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10 μF filtering capacitors are also recommended. These supply pins are separated from $PLLV_{DD}$ and DV_{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.
C/LKON	19	I/O	Bus manager contender programming input and link-on output. On hardware reset, this pin is used to set the default value of the contender status indicated during self-ID. Programming is done by tying the pin through a 10 kΩ resistor to a high (contender) or low (not contender). The resistor allows the link-on output to override the input. However, it is recommended that this pin should be programmed low, and that the contender status be set via the C register bit. If the TSB41LV01 is used with an LLC that has a dedicated pin for monitoring LKON and also setting the contender status, then a 1-kΩ series resistor should be placed on the LKON line between the PHY and LLC to prevent bus contention. Following hardware reset, this pin is the Link-On output, which is used to notify the LLC to power-up and become active. The Link-On output is a square-wave signal with a period of approximately 163 ns (8 SYSCLK cycles) when active. The Link-On output is otherwise driven low, except during hardware reset when it is high impedance. The Link-On output is activated if the LLC is inactive (LPS inactive or the LCtrl bit cleared) and when: a) the PHY receives a link-on PHY packet addressed to this node, b) the PEI (port-event interrupt) register bit is 1, or c) any of the CTOI (configuration-timeout interrupt), CPSI (cable-power-status interrupt), or STOI (state-timeout interrupt) register bits are 1 and the RPIE (resuming-port interrupt enable) register bit is also 1. Once activated, the link-on output will continue active until the LLC becomes active (both LPS active and the LCtrl bit set). The PHY also deasserts the link-on output when a bus-reset occurs unless the link-on output would otherwise be active because one of the interrupt bits is set (i.e., the link-on output is active due solely to the reception of a link-on PHY packet). NOTE: If an interrupt condition exists which would otherwise cause the link-on output to be activated if the LLC were inactive, the link-on output is activated when the LLC subsequently becomes inactive.
CNA	3	O	Cable not active output. This pin is asserted high when the port is not receiving incoming bias voltage.
CPS	24	I	Cable power status input. This pin is normally connected to cable power through a 400 kΩ resistor. This circuit drives an internal comparator that is used to detect the presence of cable power. This terminal should be tied directly to DV_{DD} supply if application does not require it to be used.
CTL0 CTL1	4 5	I/O	Control I/Os. These bidirectional signals control communication between the TSB41LV01 and the LLC. Bus holders are built into these terminals.
D0 – D7	6, 7, 8, 9, 10, 11, 12, 13	I/O	Data I/Os. These are bidirectional data signals between the TSB41LV01 and the LLC. Bus holders are built into these terminals.
DGND	17, 18, 63, 64	–	Digital circuit ground pins. These pins should be tied together to the low impedance circuit board ground plane.
DV_{DD}	25, 26, 61, 62	–	Digital circuit power pins. A combination of high frequency decoupling capacitors near each pin are suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10 μF filtering capacitors are also recommended. These supply pins are separated from $PLLV_{DD}$ and AV_{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.
FILTER0 FILTER1	54 55	I/O	PLL filter pins. These pins are connected to an external capacitance to form a lag-lead filter required for stable operation of the internal frequency multiplier PLL running off of the crystal oscillator. A 0.1 μF ±10% capacitor is the only external component required to complete this filter.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{ISO}$	23	I	Link interface isolation control input. This pin controls the operation of output differentiation logic on the CTL and D pins. If an optional Annex J type isolation barrier is implemented between the TSB41LV01 and LLC, the $\overline{ISO}$ pin should be tied low to enable the differentiation logic. If no isolation barrier is implemented (direct connection), or TI bus holder isolation is implemented, the $\overline{ISO}$ pin should be tied high to disable the differentiation logic. For additional information refer to TI application note *Serial Bus Galvanic Isolation*, SLLA011.
LPS	15	I	Link power status input. This pin is used to monitor the active/power status of the link layer controller and to control the state of the PHY-LLC interface. This pin should be connected to either the V_{DD} supplying the LLC through a 10 kΩ resistor, or to a pulsed output which is active when the LLC is powered. A pulsed signal should be used when an isolation barrier exists between the LLC and PHY. (See Figure 1). The LPS input is considered inactive if it is sampled low by the PHY for more than 2.6 μs (128 SYSCLK cycles), and is considered active otherwise (i.e., asserted steady high or an oscillating signal with a low time less than 2.6 μs). The LPS input must be high for at least 21 ns in order to be guaranteed to be observed as high by the PHY. When the TSB41LV01 detects that LPS is inactive, it will place the PHY-LLC interface into a low-power reset state. In the reset state, the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than 26 μs (1280 SYSCLK cycles), the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is placed into the disabled state upon hardware reset. The LLC is considered active only if both the LPS input is active and the LCtrl register bit is set to 1, and is considered inactive if either the LPS input is inactive or the LCtrl register bit is cleared to 0.
LREQ	1	I	LLC Request input. The LLC uses this input to initiate a service request to the TSB41LV01. Bus holder is built into this terminal.
PC0 PC1 PC2	20 21 22	I	Power class programming inputs. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying these pins high or low. Refer to Table 2 for encoding.
PD	14	I	Power-down input. A high on this pin turns off all internal circuitry except the cable-active monitor circuits, which controls the CNA output. Asserting the PD input high also activates an internal pulldown on the $\overline{RESET}$ terminal so as to force a reset of the internal control logic.
PLLGND	57, 58	–	PLL circuit ground pins. These pins should be tied together to the low impedance circuit board ground plane.
$PLLV_{DD}$	56	–	PLL circuit power pins. A combination of high frequency decoupling capacitors near each pin are suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10 μF filtering capacitors are also recommended. These supply pins are separated from DV_{DD} and AV_{DD} internal to the device to provide noise isolation. They should be tied at a low-impedance point on the circuit board.
R0 R1	40 41	–	Current setting resistor pins. These pins are connected to an external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.30 kΩ ±0.5% is required to meet the IEEE Std 1394-1995 output voltage limits.
$\overline{RESET}$	53	I	Logic reset input. Asserting this pin low resets the internal logic. An internal pullup resistor to V_{DD} is provided so only an external delay capacitor is required for proper power-up operation (see *power-up reset* in the APPLICATION INFORMATION section). The $\overline{RESET}$ terminal also incorporates an internal pulldown which is activated when the PD input is asserted high. This input is otherwise a standard logic input, and may also be driven by an open-drain type driver.
SE	28	I	Test control input. This input is used in manufacturing test of the TSB41LV01. For normal use this pin should be tied to GND through a 1-kΩ pulldown resistor.
SM	29	I	Test control input. This input is used in manufacturing test of the TSB41LV01. For normal use this pin should be tied to GND.
SYSCLK	2	O	System clock output. Provides a 49.152 MHz clock signal, synchronized with data transfers, to the LLC.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TPA+	37	I/O	Twisted-pair cable A differential signal pins. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA–	36	I/O	
TPB+	35	I/O	Twisted-pair cable B differential signal pins. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB–	34	I/O	
TPBIAS	38	I/O	Twisted-pair bias output. This provides the 1.86 V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection. This pin must be decoupled with a 1.0 μF capacitor to ground.
TESTM	27	I	Test control input. This input is used in manufacturing test of the TSB41LV01. For normal use this pin should be tied to V_{DD}.
XI XO	59 60	–	Crystal oscillator inputs. These pins connect to a 24.576 MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used (see *crystal selection* in the APPLICATIONS INFORMATION section).

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.3 V to 4 V
Input voltage range, V_I . . . . . –0.5 V to V_{DD}+0.5 V
5-V-tolerant I/O supply voltage range, V_{DD_5V} . . . . . –0.3 V to 5.5 V
5-V-tolerant input voltage range, $V_{I\text{-}5V}$ . . . . . –0.5 V to V_{DD_5V}+0.5 V
Output voltage range at any output, V_O . . . . . –0.5 V to V_{DD}+0.5V
Electrostatic discharge (see Note 2) . . . . . HBM:2 kV, MM:200 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free air temperature, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground.
2. HBM is human body model, MM is machine model.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PAP§	3.98 W	39.8 mW/°C	2.19 W
PAP¶	1.76 W	17.6 mW/°C	0.97 W
PAP#	1.62 W	16.2 mW/°C	0.89 W

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).
§ 1 oz. trace and copper pad with solder.
¶ 1 oz. trace and copper pad without solder.
# Standard JEDEC high-K board
For more information, refer to TI application note *PowerPAD™ Thermally Enhanced Package,* TI literature number SLMA002.

PowerPAD is a trademark of Texas Instruments.

recommended operating conditions

PARAMETER		MIN	TYP†	MAX	UNIT
Supply voltage, V_{DD}	Source power node	3	3.3	3.6	V
	Nonsource power node	2.7‡	3	3.6	
High-level input voltage, V_{IH}	Case 1 (Bus holder): $\overline{ISO}$=V_{DD}, V_{DD_5V}=V_{DD} Case 2 (5V Tol): $\overline{ISO}$=V_{DD}, V_{DD_5V}=5V LREQ, CTL0, CTL1, D0–D7	2.6			V
	C/LKON, PC0, PC1, PC2, $\overline{ISO}$, PD	0.7×V_{DD}			
	$\overline{RESET}$	0.6×V_{DD}			
Low-level input voltage, V_{IL}	Case 1 (Bus holder): $\overline{ISO}$=V_{DD}, V_{DD_5V}=V_{DD} Case 2 (5V Tol): $\overline{ISO}$=V_{DD}, V_{DD_5V}=5V LREQ, CTL0, CTL1, D0–D7			1.2	V
	C/LKON, PC0, PC1, PC2, $\overline{ISO}$, PD			0.2×V_{DD}	
	$\overline{RESET}$			0.3×V_{DD}	
Output current, I_O	TPBIAS outputs	–5.6		1.3	mA
Maximum junction temperature, T_J (see $R_{\theta JA}$ values listed in thermal characteristics table)	$R_{\theta JA}$=25.2°C/W, T_A=70°C			92.4	°C
	$R_{\theta JA}$=56.8°C/W, T_A=70°C			120.7	
	$R_{\theta JA}$=61.6°C/W, T_A=70°C			125	
Differential input voltage, V_{ID}	Cable inputs, during data reception	118		260	mV
	Cable inputs, during arbitration	168		265	
Common-mode input voltage, V_{IC}	TPB cable inputs, source power node	0.4706		2.515	V
	TPB cable inputs, nonsource power node	0.4706		2.015‡	
Power-up reset time, t_{pu}	$\overline{RESET}$ input	2			ms
Receive input jitter	TPA, TPB cable inputs, S100 operation			±1.08	ns
	TPA, TPB cable inputs, S200 operation			±0.5	
	TPA, TPB cable inputs, S400 operation			±0.315	
Receive input skew	Between TPA and TPB cable inputs, S100 operation			±0.8	ns
	Between TPA and TPB cable inputs, S200 operation			±0.55	
	Between TPA and TPB cable inputs, S400 operation			±0.5	

† All typical values are at V_{DD} = 3.3 V and T_A = 25°C.
‡ For a node that does not source power; see Section 4.2.2.2 in IEEE P1394A.

electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

driver

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OD}	Differential output voltage	56 Ω,	See Figure 1	172		265	mV
I_{DIFF}	Driver difference current, TPA+, TPA–, TPB+, TPB–	Drivers enabled,	Speed signaling off	–1.05†		1.05†	mA
I_{SP200}	Common mode speed signaling current, TPB+, TPB–	S200 speed signaling enabled		–4.84‡		–2.53‡	mA
I_{SP400}	Common mode speed signaling current, TPB+, TPB–	S400 speed signaling enabled		–12.4‡		–8.10‡	mA
V_{OFF}	Off state differential voltage	Drivers disabled,	See Figure 1			20	mV

† Limits defined as algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– algebraic sum of driver currents.
‡ Limits defined as absolute limit of each of TPB+ and TPB– driver currents.

receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{ID}	Differential impedance	Drivers disabled	10	14		kΩ
					4	pF
Z_{IC}	Common mode impedance		20			kΩ
					24	pF
$V_{TH–R}$	Receiver input threshold voltage		–30		30	mV
$V_{TH–CB}$	Cable bias detect threshold, TPB cable inputs		0.6		1	V
V_{TH+}	Positive arbitration comparator threshold voltage		89		168	mV
$V_{TH–}$	Negative arbitration comparator threshold voltage		–168		–89	mV
$V_{TH–SP200}$	Speed signal threshold	TPBIAS–TPA common mode voltage, drivers disabled	49		131	mV
$V_{TH–SP400}$	Speed signal threshold		314		396	mV

electrical characteristics over recommended ranges of operating conditions (unless otherwise noted) (continued)

device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	See Note 3		69		mA
		See Note 4		52		
		See Note 5		49		
$I_{DD–ULP}$	Supply current – ultralow power mode	V_{DD} = 3.3 V, T_A = 25°C, Port disabled, PD=0V, LPS=0V		150		µA
V_{TH}	Power status threshold, CPS input†	400-kΩ resistor†	4.7		7.5	V
V_{OH}	High-level output voltage, CTL0, CTL1, D0–D7, CNA, C/LKON, SYSCLK outputs	V_{DD}=2.7 V, I_{OH} = –4 mA	2.2			V
		V_{DD}=3 to 3.6 V, I_{OH} = –4 mA	2.8			
V_{OL}	Low-level output voltage, CTL0, CTL1, D0–D7, CNA, C/LKON, SYSCLK outputs	I_{OL} = 4 mA			0.4	V
$V_{OH–AJ}$	High-level Annex J output voltage, CTL0, CTL1, D0–D7, C/LKON, SYSCLK outputs	Annex J: I_{OH}= –9 mA, $\overline{ISO}$ = 0V, V_{DD_5V} = V_{DD}, V_{DD} ≥ 3 V	V_{DD}–0.4			V
$V_{OL–AJ}$	Low-level Annex J output voltage, CTL0, CTL1, D0–D7, $\overline{CLKON}$, SYSCLK outputs	Annex J: I_{OL}= 9 mA, $\overline{ISO}$ = 0V, V_{DD_5V} = V_{DD}, V_{DD} ≥ 3 V			0.4	V
I_{BH+}	Positive peak bus holder current, D0–D7, CTL0–CTL1, LREQ	$\overline{ISO}$ = 3.6 V, V_{DD} = 3.6 V, V_I = 0 V to V_{DD}, V_{DD_5V} = V_{DD}	0.05		1	mA
$I_{BH–}$	Negative peak bus holder current, D0–D7, CTL0–CTL1, LREQ	$\overline{ISO}$ = 3.6 V, V_{DD} = 3.6 V, V_I = 0 V to V_{DD}, V_{DD_5V} = V_{DD}	–1		–0.05	mA
I_I	Input current, LREQ, LPS, PD, TESTM, SM, PC0–PC2 inputs	$\overline{ISO}$=0 V, V_{DD} = 3.6 V			5	µA
I_{OZ}	Off-state output current, CTL0, CTL1, D0–D7, C/LKON I/Os	V_O= V_{DD} or 0 V			±5	µA
I_{IRST}	Pullup current, $\overline{RESET}$ input	V_I=1.5 V or 0 V	–90		–20	µA
$I_{SE–PU}$	Pullup current, SE input	V_I=1.5 V or 0 V	–50		–5	µA
V_{IT+}	Positive input threshold voltage, LREQ, CTL0, CTL1, D0–D7 inputs‡	V_{DD_5V}=V_{DD}, $\overline{ISO}$= 0 V	V_{DD}/2+0.3		V_{DD}/2+0.9	V
	Positive input threshold voltage, LPS inputs	V_{DD_5V}=V_{DD}, V_{ref} = V_{DD}×0.42, $\overline{ISO}$= 0 V			V_{ref}+1	
$V_{IT–}$	Negative input threshold voltage, LREQ, CTL0, CTL1, D0–D7 inputs‡	$\overline{ISO}$= 0 V, V_{DD_5V}=V_{DD}	V_{DD}/2–0.9		V_{DD}/2–0.3	V
	Negative input threshold voltage, LPS inputs	$\overline{ISO}$= 0 V, V_{DD_5V}=V_{DD}, V_{ref} = V_{DD}×0.42	V_{ref}+0.2			
V_O	TPBIAS output voltage	At rated I_O current	1.665		2.015	V

† This parameter applicable only when $\overline{ISO}$ low.
‡ Measured at cable power side of resistor.

NOTES: 3. Transmit max packet (1 port transmitting max size isochronous packet – 4096 bytes, sent on every isochronous interval, s400, data value of 0xCCCCCCCCh), V_{DD} = 3.3 V, T_A = 25°C
4. Repeat typical packet (1 port receiving DV packets on every isochronous interval, S100), V_{DD} = 3.3 V, T_A = 25°C
5. Idle (1 port transmitting cycle starts), V_{DD} = 3.3 V, T_A = 25°C

electrical characteristics over recommended ranges of operating conditions (unless otherwise noted) (continued)

thermal characteristics

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
RθJA	Junction-to-free-air thermal resistance	Board mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land with 1 oz. copper		25.15		°C/W
RθJC	Junction-to-case-thermal resistance			1.2		
RθJA	Junction-to-free-air thermal resistance	Board mounted, no air flow, high conductivity TI recommended test board with thermal land, but no solder or grease thermal connection to thermal land with 1 oz. copper		56.78		°C/W
RθJC	Junction-to-case-thermal resistance			1.2		
RθJA	Junction-to-free-air thermal resistance	Board mounted, no air flow, high conductivity JEDEC test board with 1 oz. copper		61.63		°C/W
RθJC	Junction-to-free-air thermal resistance			1.2		°C/W

† Usage of thermally enhanced PowerPad™ PAP package is assumed in all three test conditions.

switching characteristics

driver

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Jitter, transmit	Between TPA and TPB				±0.15	ns
	Skew, transmit	Between TPA and TPB				±0.10	ns
t_r	TP differential rise time, transmit	10% to 90%,	At 1394 connector	0.5		1.2	ns
t_f	TP differential fall time, transmit	90% to 10%,	At 1394 connector	0.5		1.2	ns
t_{su}	Setup time, CTL0, CTL1, D0–D7, LREQ to SYSCLK	50% to 50%,	See Figure 2	5			ns
t_h	Hold time, CTL0, CTL1, D0–D7, LREQ after SYSCLK	50% to 50%,	See Figure 2	2			ns
t_d	Delay time, SYSCLK to CTL0, CTL1, D0–D7	50% to 50%,	See Figure 3	2*			ns

* Test Conditions: 3.3 V_{CC}, T_A = 25°C

PARAMETER MEASUREMENT INFORMATION

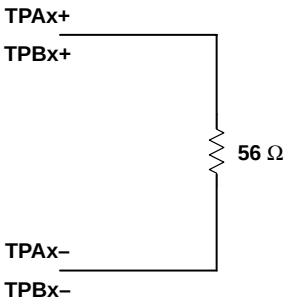


Figure 1. Test Load Diagram

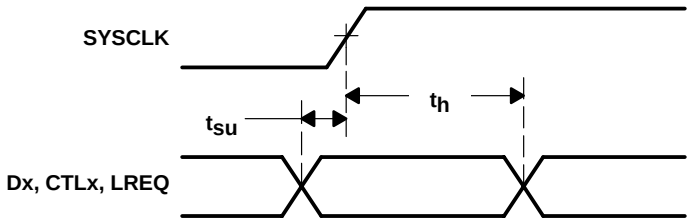


Figure 2. Dx, CTLx, LREQ Input Setup and Hold Time Waveforms

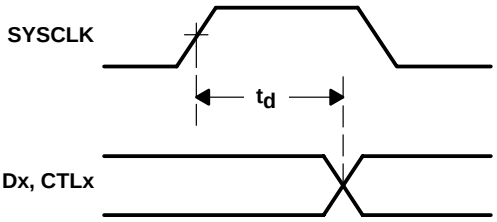


Figure 3. Dx and CTLx Output Delay Relative to SYSCLK Waveforms

APPLICATION INFORMATION

internal register configuration

There are 16 accessible internal registers in the TSB41LV01. The configuration of the registers at addresses 0 through 7 (the base registers) is fixed, while the configuration of the registers at addresses 8 through Fh (the paged registers) is dependent upon which one of eight pages, numbered 0 through 7, is currently selected. The selected page is set in base register 7.

The configuration of the base registers is shown in Table 1, and corresponding field descriptions given in Table 5. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as Reserved or Rsvd in the register configuration tables below) is read as 0, but is subject to future usage. All registers in pages 2 through 6 are reserved.

Table 1. Base Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	PHYsical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (‘b111)			Rsvd	Num_Ports (‘b0010)			
0011	PHY_Speed (‘b010)			Rsvd	Delay (‘b0000)			
0100	LCtrl	C	Jitter (‘b000)			Pwr_Class		
0101	RPIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Reserved							
0111	Page_Select			Rsvd	Port_Select			

Table 2. Base Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
PHYsical ID	6	Rd	This field contains the physical address ID of this node determined during self-ID. The physical-ID is invalid after a bus-reset until self-ID has completed as indicated by an unsolicited register-0 status transfer.
R	1	Rd	Root. This bit indicates that this node is the root node. The R bit is reset to 0 by bus-reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	Rd	Cable-power-status. This bit indicates the state of the CPS input pin. The CPS pin is normally tied to serial bus cable power through a 400 kΩ resistor. A 0 in this bit indicates that the cable power voltage has dropped below its threshold for guaranteed reliable operation.
RHB	1	Rd/Wr	Root-holdoff bit. This bit instructs the PHY to attempt to become root after the next bus-reset. The RHB bit is reset to 0 by hardware reset and is unaffected by bus-reset.
IBR	1	Rd/Wr	Initiate bus-reset. This bit instructs the PHY to initiate a long (166 µs) bus-reset at the next opportunity. Any receive or transmit operation in progress when this bit is set completes before the bus-reset is initiated. The IBR bit is reset to 0 by hardware reset or bus-reset.
Gap_Count	6	Rd/Wr	Arbitration gap count. This value is used to set the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count may be set either by a write to this register or by reception or transmission of a PHY_CONFIG packet. The gap count is set to 3Fh by hardware reset or after two consecutive bus-resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet).
Extended	3	Rd	Extended register definition. For the TSB41LV01 this field is ‘b111, indicating that the extended register set is implemented.
Num_Ports	4	Rd	Number of ports. This field indicates the number of ports implemented in the PHY. For the TSB41LV01 this field is 1.

APPLICATION INFORMATION

internal register configuration

Table 2. Base Register Field Descriptions (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
PHY_Speed	3	Rd	PHY speed capability. For the TSB41LV01 PHY this field is ‘b010, indicating S400 speed capability.
Delay	4	Rd	PHY repeater data delay. This field indicates the worst case repeater data delay of the PHY, expressed as 144+(delay*20) ns. For the TSB41LV01 this field is 0.
LCtrl	1	Rd/Wr	Link-active status control. This bit is used to control the active status of the LLC as indicated during self-ID. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. The LLC is considered active only if both the LPS input is active and the LCtrl bit is set. The LCtrl bit provides a software controllable means to indicate the LLC active status in lieu of using the LPS input. The LCtrl bit is set to 1 by hardware reset and is unaffected by bus-reset. NOTE: The state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY-LLC interface is operational as determined by the LPS input being active, then received packets and status information continues to be presented on the interface, and any requests indicated on the LREQ input will be processed, even if the LCtrl bit is cleared to 0.
C	1	Rd/Wr	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the c field (bit 20) of the self-ID packet. This bit is set to the state specified by the C/LKON input pin upon hardware reset and is unaffected by bus-reset.
Jitter	3	Rd	PHY repeater jitter. This field indicates the worst case difference between the fastest and slowest repeater data delay, expressed as (JITTER+1)*20 ns. For the TSB41LV01 this field is 0.
Pwr_Class	3	Rd/Wr	Node power class. This field indicates this node’s power consumption and source characteristics, and is replicated in the pwr field (bits 21–23) of the self-ID packet. This field is set to the state specified by the PC0 – PC2 input pins upon hardware reset and is unaffected by bus-reset. See Table 9.
RPIE	1	Rd/Wr	Resuming port interrupt enable. This bit, if set to 1, enables the port event interrupt (PEI) bit to be set whenever resume operations begin on any port. This bit also enables the C/LKON output signal to be activated whenever the LLC is inactive and any of the CTOI, CPSI, or STOI interrupt bits are set. This bit is reset to 0 by hardware reset and is unaffected by bus-reset.
ISBR	1	Rd/Wr	Initiate short arbitrated bus-reset. This bit, if set to 1, instructs the PHY to initiate a short (1.30 μs) arbitrated bus-reset at the next opportunity. This bit is reset to 0 by bus-reset. NOTE: Legacy IEEE Std 1394-1995 compliant PHYs may not be capable of performing short bus-resets. Therefore, initiation of a short bus-reset in a network that contains such a legacy device results in a long bus-reset being performed.
CTOI	1	Rd/Wr	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times-out during tree-ID start, and may indicate that the bus is configured in a loop. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit. If the CTOI and RPIE bits are both set and the LLC is or becomes inactive, the PHY activates the C/LKON output to notify the LLC to service the interrupt. NOTE: If the network is configured in a loop, only those nodes that are part of the loop generates a configuration time-out interrupt. All other nodes will instead time-out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus-reset.
CPSI	1	Rd/Wr	Cable power status interrupt. This bit is set to 1 whenever the CPS input transitions from high to low indicating that cable power may be too low for reliable operation. This bit is reset to 1 by hardware reset. It can be cleared by writing a 1 to this register bit. If the CPSI and RPIE bits are both set and the LLC is or becomes inactive, the PHY activates the $\overline{\text{C/LKON}}$ output to notify the LLC to service the interrupt.
STOI	1	Rd/Wr	State time-out interrupt. This bit indicates that a state time-out has occurred (which also causes a bus-reset to occur). This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit. If the STOI and RPIE bits are both set and the LLC is or becomes inactive, the PHY activates the $\overline{\text{C/LKON}}$ output to notify the LLC to service the interrupt.

APPLICATION INFORMATION

internal register configuration

Table 2. Base Register Field Descriptions (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
PEI	1	Rd/Wr	Port event interrupt. This bit is set to 1 upon a change in the bias (unless disabled), connected, disabled, or fault bits for any port for which the port interrupt enable (PIE) bit is set. Additionally, if the resuming port interrupt enable (RPIE) bit is set, the PEI bit is set to 1 at the start of resume operations on any port. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit. If the PEI bit is set (regardless of the state of the RPEI bit) and the LLC is or becomes inactive, the PHY activates the C/LKON output to notify the LLC to service the interrupt.
EAA	1	Rd/Wr	Enable accelerated arbitration. This bit enables the PHY to perform the various arbitration acceleration enhancements defined in P1394a (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is reset to 0 by hardware reset and is unaffected by bus-reset. NOTE: The EAA bit should be set only if the attached LLC is P1394a compliant. If the LLC is not P1394a compliant, use of the arbitration acceleration enhancements may interfere with isochronous traffic by excessively delaying the transmission of cycle-start packets.
EMC	1	Rd/Wr	Enable multi-speed concatenated packets. This bit enables the PHY to transmit concatenated packets of differing speeds in accordance with the protocols defined in P1394a. This bit is reset to 0 by hardware reset and is unaffected by bus-reset. NOTE: The use of multispeed concatenation is completely compatible with networks containing legacy IEEE Std 1394-1995 PHYs. However, use of multispeed concatenation requires that the attached LLC be P1394a compliant.
Page_Select	3	Rd/Wr	Page-select. This field selects the register page to use when accessing register addresses 8 through 15. This field is reset to 0 by hardware reset and is unaffected by bus-reset.
Port_Select	4	Rd/Wr	Port-select. This field selects the port when accessing per-port status or control (e.g., when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is reset to 0 by hardware reset and is unaffected by bus-reset.

The port status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. The configuration of the port status page registers is shown in Table 3, and corresponding field descriptions given in Table 4. If the selected port is unimplemented, all registers in the port status page are read as 0.

Table 3. Page 0 (Port Status) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	AStat		Bstat		Ch	Con	Bias	Dis
1001	Peer_Speed			PIE	Fault	Reserved		
1010	Reserved							
1011	Reserved							
1100	Reserved							
1101	Reserved							
1110	Reserved							
1111	Reserved							

APPLICATION INFORMATION

internal register configuration (continued)

Table 4. Page 0 (Port Status) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
AStat	2	Rd	TPA line state. This field indicates the TPA line state of the selected port, encoded as follows: **Code** **Line State** 11 Z 01 1 10 0 00 invalid
Bstat	2	Rd	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the ASTAT field.
Ch	1	Rd	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus-reset until tree-ID has completed.
Con	1	Rd	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341 ms for the Con bit to be set to 1. The Con bit is reset to 0 by hardware reset and is unaffected by bus-reset. NOTE: The Con bit indicates that the port is physically connected to a peer PHY, but the port is not necessarily active.
Bias	1	Rd	Debounced incoming cable bias status. A 1 indicates that the selected port is detecting incoming cable bias. The incoming cable bias must be stable for the debounce time of 52 μs for the bias bit to be set to 1.
Dis	1	Rd/Wr	Port disabled control. If 1, the selected port is disabled. The Dis bit is reset to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus-reset.
Peer_Speed	3	Rd	Port peer speed. This field indicates the highest speed capability of the peer PHY connected to the selected port, encoded as follows: **Code** **Peer Speed** 000 S100 001 S200 010 S400 011–111 invalid The Peer_Speed field is invalid after a bus-reset until self-ID has completed. NOTE: Peer speed codes higher than ‘b010 (S400) are defined in P1394a. However, the TSB41LV01 is only capable of detecting peer speeds up to S400.
PIE	1	Rd/Wr	Port event interrupt enable. When set to 1, a port event on the selected port will set the port event interrupt (PEI) bit and notify the link. This bit is reset to 0 by hardware reset and is unaffected by bus-reset.
Fault	1	Rd/Wr	Fault. This bit indicates that a resume-fault or suspend-fault has occurred on the selected port and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend-fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the fault bit to 0. This bit is reset to 0 by hardware reset and is unaffected by bus-reset.

The vendor identification page is used to identify the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select field in base register 7. The configuration of the vendor identification page is shown in Table 5, and corresponding field descriptions given in Table 6.

APPLICATION INFORMATION

internal register configuration (continued)

Table 5. Page 1 (Vendor ID) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID[0]							
1011	Vendor_ID[1]							
1100	Vendor_ID[2]							
1101	Product_ID[0]							
1110	Product_ID[1]							
1111	Product_ID[2]							

Table 6. Page 1 (Vendor ID) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	Rd	Compliance level. For the TSB41LV01 this field is 01h, indicating compliance with the P1394a specification.
Vendor_ID	24	Rd	Manufacturer's organizationally unique identifier (OUI). For the TSB41LV01 this field is 08_00_28h (Texas Instruments) (the MSB is at register address 'b1010).
Product_ID	24	Rd	Product identifier. For the TSB41LV01 this field is 42_xx_xxh (the MSB is at register address 'b1101).

The vendor-dependent page provides access to the special control features of the TSB41LV01, as well as configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page_Select field in base register 7. The configuration of the vendor-dependent page is shown in Table 7, and corresponding field descriptions given in Table 8.

Table 7. Page 7 (Vendor-Dependent) Register Configuration)

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	NPA	Reserved					Link_Speed	
1001	Reserved for test							
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	Reserved for test							
1111	Reserved for test							

APPLICATION INFORMATION

internal register configuration (continued)

Table 8. Page 7 (Vendor-Dependent) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
NPA	1	Rd/Wr	Null-packet actions flag. This bit instructs the PHY to not clear fair and priority requests when a null packet is received with arbitration acceleration enabled. If 1, then fair and priority requests are cleared only when a packet of more than 8 bits is received; ACK packets (exactly 8 data bits), null packets (no data bits), and malformed packets (less than 8 data bits) will not clear fair and priority requests. If 0, then fair and priority requests are cleared when any non-ACK packet is received, including null-packets or malformed packets of less than 8 bits. This bit is cleared to 0 by hardware reset and is unaffected by bus-reset.
Link_Speed	2	Rd/Wr	Link speed. This field indicates the top speed capability of the attached LLC. Encoding is as follows: **Code** **Speed** 00 S100 01 S200 10 S400 11 illegal This field is replicated in the sp field of the self-ID packet to indicate the speed capability of the node (PHY and LLC in combination). However, this field does not affect the PHY speed capability indicated to peer PHYs during self-ID; the TSB41LV01 PHY identifies itself as S400 capable to its peers regardless of the value in this field. This field is set to ‘b10 (S400) by hardware reset and is unaffected by bus-reset.

power-class programming

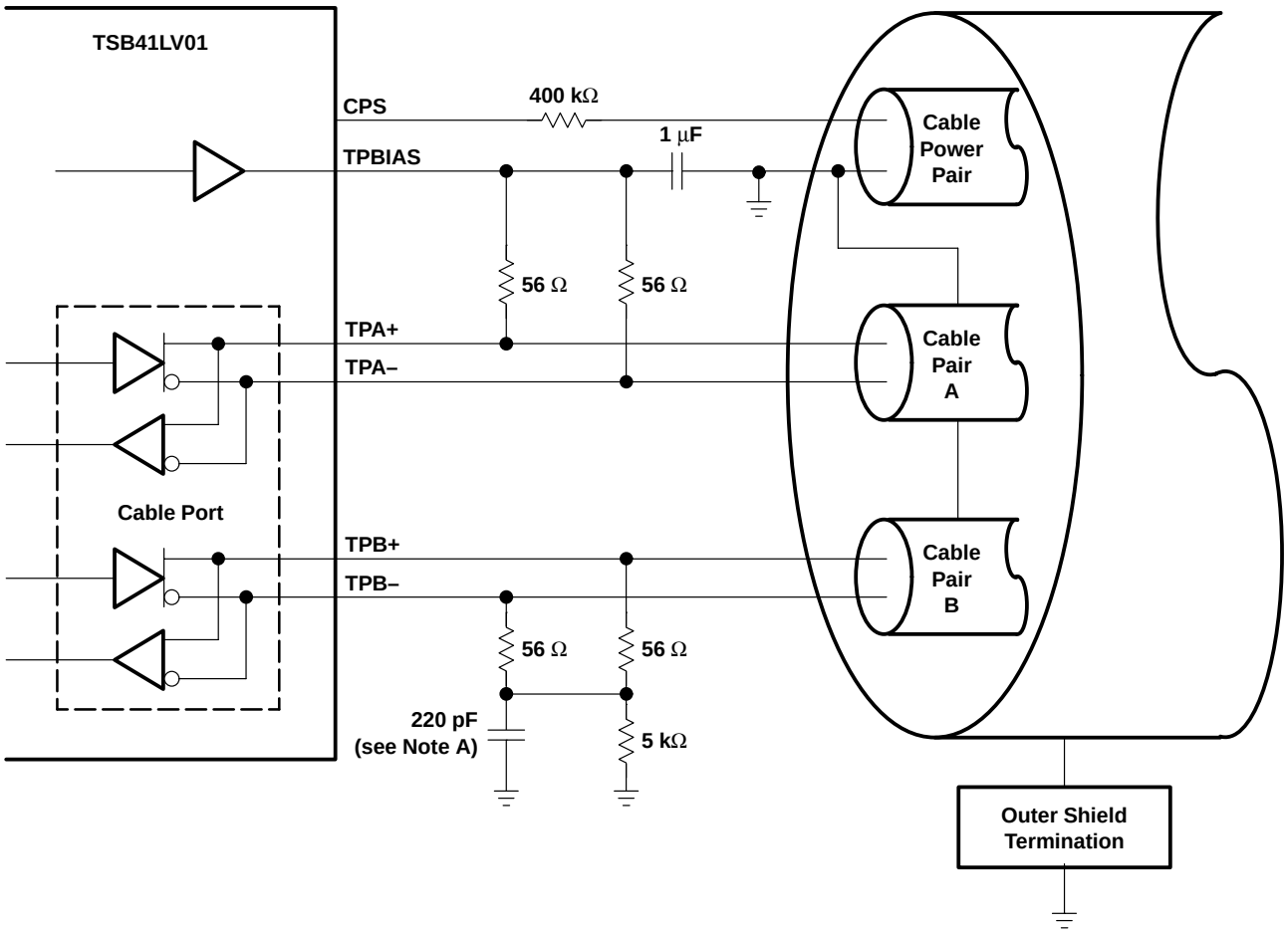
The PC0–PC2 pins are programmed to set the default value of the power-class indicated in the pwr field (bits 21–23) of the transmitted self-ID packet. Descriptions of the various power-classes are given in Table 9. The default power-class value is loaded following a hardware reset, but is overridden by any value subsequently loaded into the Pwr_Class field in register 4.

Table 9. Power-Class Descriptions

PC0–PC2	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self-powered and provides a minimum of 15W to the bus.
010	Node is self-powered and provides a minimum of 30W to the bus.
011	Node is self-powered and provides a minimum of 45W to the bus.
100	Node may be powered from the bus for the PHY only using up to 3W and may also provide power to the bus. The amount of bus power that it provides can be found in the configuration ROM.
101	Node is powered from the bus and uses up to 3W. An additional 2W is needed to enable the link and higher layers of the node.
110	Node is powered from the bus and uses up to 3W. An additional 3W is needed to enable the link.
111	Node is powered from the bus and uses up to 3W. An additional 7W is needed to enable the link.

APPLICATION INFORMATION

internal register configuration (continued)



NOTE A: The IEEE Std 1394-1995 calls for a 250 pF capacitor, which is a nonstandard component value. A 220 pF capacitor is recommended.

Figure 4. TP Cable Connections

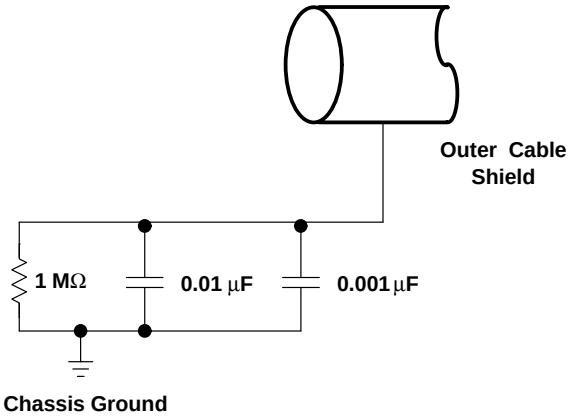


Figure 5. Compliant DC Isolated Outer Shield Termination

APPLICATION INFORMATION

internal register configuration (continued)

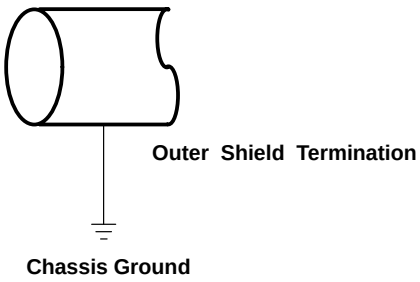


Figure 6. Non-Isolated Outer Shield Termination

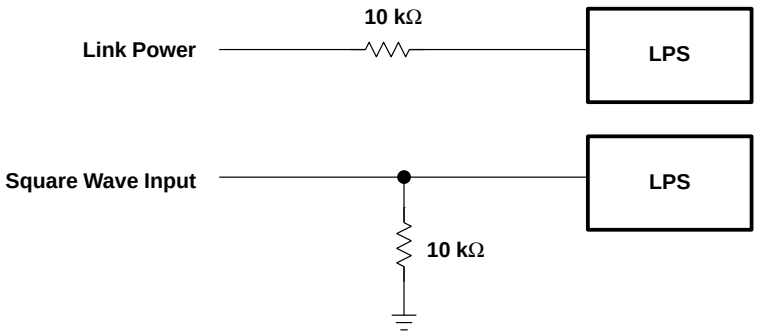


Figure 7. Non-Isolated Circuit Connection Variations for LPS

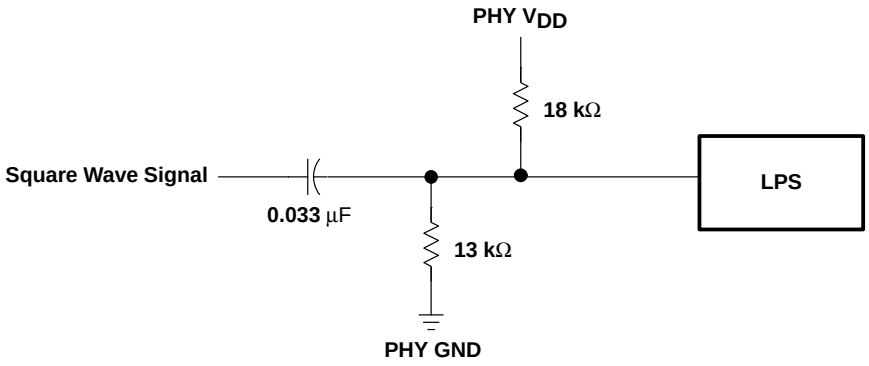


Figure 8. Isolated Circuit Connection for LPS

APPLICATION INFORMATION

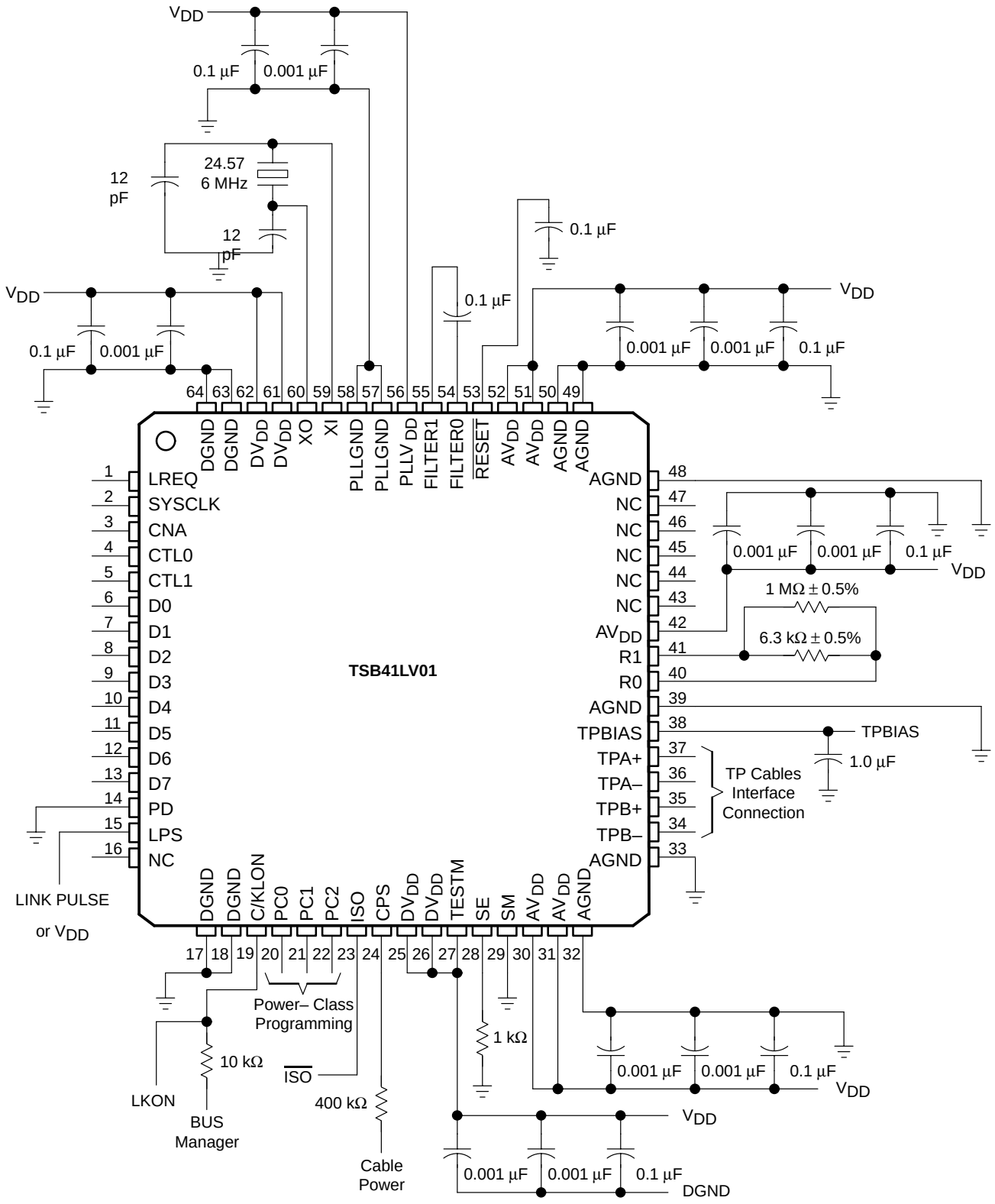


Figure 9. External Component Connections

APPLICATION INFORMATION

designing with PowerPAD

The TSB41LV01 is housed in a high performance, thermally enhanced, 64-pin PAP PowerPAD™ package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed metallic pad on the bottom of the device, is a thermal and electrical conductor. This exposed pad is connected internally to the package to the substrate of the silicon die, it is not connected to any pin of the package. Therefore, if not implementing PowerPAD PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD of connection etches or vias under the package. The recommended option, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keepout area for the 64-pin PAP PowerPAD package is 8 mm X 8 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land will vary in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web. Pages beginning at URL: http://www.ti.com. Figure 1. Example of a Thermal Land for the TSB41LV01 PHY.

For the TSB41LV01, this thermal land should be grounded to the low impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground pin landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal pins. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout*, TI literature number SLLA020.

using the TSB41LV01 with a non-P1394a link layer

The TSB41LV01 implements the PHY-LLC interface specified in the P1394a Supplement. This interface is based upon the interface described in informative Annex J of IEEE Std 1394-1995, which is the interface used in older TI PHY devices. The PHY-LLC interface specified in P1394a is completely compatible with the older Annex J interface.

The P1394a supplement includes enhancements to the Annex J interface that must be comprehended when using the TSB41LV01 with a non-P1394a LLC device.

- A new LLC service request was added which allows the LLC to temporarily enable and disable asynchronous arbitration accelerations. If the LLC does not implement this new service request, the arbitration enhancements should not be enabled (see the EAA bit in PHY register 5).
- The capability to perform multispeed concatenation (the concatenation of packets of differing speeds) was added in order to improve bus efficiency (primarily during isochronous transmission). If the LLC does not support multispeed concatenation, multispeed concatenation should not be enabled in the PHY (see the EMC bit in PHY register 5).

APPLICATION INFORMATION

using the TSB41LV01 with a non-P1394a link layer (continued)

- In order to accommodate the higher transmission speeds expected in future revisions of the standard, P1394A extended the speed code in bus requests from 2 bits to 3 bits, increasing the length of the bus request from 7 bits to 8 bits. The new speed codes were carefully selected so that new P1394a PHY and LLC devices would be compatible, for speeds from S100 to S400, with legacy PHY and LLC devices that use the 2-bit speed codes. The TSB41LV01 correctly interprets both 7-bit bus requests (with 2-bit speed codes) and 8-bit bus requests (with 3-bit speed codes). Moreover, if a 7-bit bus request is immediately followed by another request (e.g., a register read or write request), the TSB41LV01 correctly interprets both requests. Although the TSB41LV01 correctly interprets 8-bit bus requests, a request with a speed code exceeding S400 results in the TSB41LV01 transmitting a null packet (data-prefix followed by data-end, with no data in the packet).

More explanation is included in the TI application note *IEEE 1394a Features Supported by TI TSB41LV0X PHYsical Layer Devices,* TI literature number SLL019.

using the TSB41LV01 with a lower-speed link layer

Although the TSB41LV01 is an S400 capable PHY, it may be used with lower speed LLCs, such as the S200 capable TSB12LV31. In such a case, the LLC has fewer data terminals than the PHY, and some Dn terminals on the TSB41LV01 will be unused. Unused Dn terminals should be pulled to ground through 10-kΩ resistors.

The TSB41LV01 transfers all received packet data to the LLC, even if the speed of the packet exceeds the capability of the LLC to accept it. Some lower speed LLC designs do not properly ignore packet data in such cases. On the rare occasions that the first 16 bits of partial data accepted by such a LLC match a node's bus and node ID, spurious header CRC or tcode errors may result.

During bus initialization following a bus-reset, each PHY transmits a self-ID packet that indicates, among other information, the speed capability of the PHY. The bus manager (if one exists) builds a speed-map from the collected self-ID packets. This speed-map gives the highest possible speed that can be used on the node-to-node communication paths between every pair of nodes in the network.

In the case of a node consisting of a higher-speed PHY and a lower-speed LLC, the speed capability of the node (PHY and LLC in combination) is that of the lower-speed LLC. A sophisticated bus manager may be able to determine the LLC speed capability by reading the configuration ROM Bus_Info_Block, or by sending asynchronous request packets at different speeds to the node and checking for an acknowledge; the speed-map may then be adjusted accordingly. The speed-map should reflect that communication to such a node must be done at the lower speed of the LLC, instead of the higher speed of the PHY. However, speed-map entries for paths that merely pass through the node's PHY, but do not terminate at that node, should not be restricted by the lower speed of the LLC.

To assist in building an accurate speed-map, the TSB41LV01 has the capability of indicating a speed capability other than S400 in its transmitted self-ID packet. This is controlled by the Link_Speed field in register 8 of the vendor-dependent page (page 7). Setting the Link_Speed field affects only the speed indicated in the self-ID packet; it has no effect on the speed signaled to peer PHYs during self-ID. The TSB41LV01 identifies itself as S400 capable to its peers regardless of the value in the Link_Speed field.

Generally, the Link_Speed field should not be changed from its power-on default value of S400 unless it is determined that the speed-map (if one exists) is incorrect for path entries terminating in the local node. If the speed-map is incorrect, it can be assumed that the bus manager has used only the self-ID packet information to build the speed-map. In this case, the node may update the Link_Speed field to reflect the lower speed capability of the LLC and then initiate another bus-reset to cause the speed-map to be rebuilt. Note that in this scenario any speed-map entries for node-to-node communication paths that pass through the local node's PHY is restricted by the lower speed.

APPLICATION INFORMATION

using the TSB41LV01 with a lower-speed link layer (continued)

In the case of a leaf node (which has only one active port) the Link_Speed field may be set to indicate the speed of the LLC without first checking the speed-map. Changing the Link_Speed field in a leaf node can only affect those paths that terminate at that node, since no other paths can pass through a leaf node; it can have no effect on other paths in the speed-map. For hardware configurations, which can only be a leaf node (all ports but one are unimplemented), it is recommended that the Link_Speed field be updated immediately after power-on or hardware reset.

power-up reset

To ensure proper operation of the TSB41LV01 the $\overline{\text{RESET}}$ pin must be asserted low for a minimum of 2 ms from the time that PHY power reaches the minimum required supply voltage. When using a passive capacitor on the $\overline{\text{RESET}}$ pin to generate a power-on reset signal, the minimum reset time will be assured if the capacitor has a minimum value of 0.1 μF and also satisfies the following equation:

$$C_{min} = 0.0077 \times T + 0.085 \quad (1)$$

where C_{min} is the minimum capacitance on the $\overline{\text{RESET}}$ pin in μF, and T is the V_{DD} ramp time, 10%–90%, in ms.

crystal selection

The TSB41LV01 and other TI PHY devices are designed to use an external 24.576 MHz crystal connected between the XI and XO pins to provide the reference for an internal oscillator circuit. This oscillator in turn drives a PLL circuit that generates the various clocks required for transmission and resynchronization of data at the S100 through S400 media data rates.

A variation of less than ±100 ppm from nominal for the media data rates is required by IEEE Std 1394. Adjacent PHYs may therefore have a difference of up to 200 ppm from each other in their internal clocks, and PHYs must be able to compensate for this difference over the maximum packet length. Larger clock variations may cause resynchronization overflows or underflows, resulting in corrupted packet data.

For the TSB41LV01, the SYSCLK output may be used to measure the frequency accuracy and stability of the internal oscillator and PLL from which it is derived. The frequency of the SYSCLK output must be within ±100 ppm of the nominal frequency of 49.152 MHz.

The following are some typical specifications for crystals used with the physical layers from TI in order to achieve the required frequency accuracy and stability:

- Crystal mode of operation: Fundamental
- Frequency tolerance at 25°C: Total frequency variation for the complete circuit is ±100 ppm. A crystal with ±30 ppm frequency tolerance is recommended for adequate margin.
- Frequency stability (over temperature and age): A crystal with ±30 ppm frequency stability is recommended for adequate margin.

NOTE:

The total frequency variation must be kept below ±100 ppm from nominal with some allowance for error introduced by board and device variations. Trade-offs between frequency tolerance and stability may be made as long as the total frequency variation is less than ±100 ppm. For example, the frequency tolerance of the crystal may be specified at 50 ppm and the temperature tolerance may be specified at 30 ppm to give a total of 80 ppm possible variation due to the crystal alone. Crystal aging also contributes to the frequency variation.

APPLICATION INFORMATION

crystal selection (continued)

- Load capacitance: For parallel resonant mode crystal circuits, the frequency of oscillation is dependent upon the load capacitance specified for the crystal. Total load capacitance (C_L) is a function of not only the discrete load capacitors, but also board layout and circuit. It may be necessary to iteratively select discrete load capacitors until the SYSCLK output is within specification. It is recommended that load capacitors with a maximum of ±5% tolerance be used.

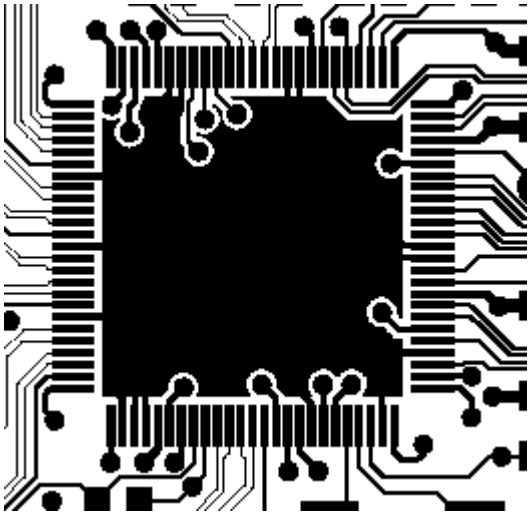


Figure 10

As an example, for the OHCI + 41LV02 evaluation module (EVM) which uses a crystal specified for 12 pF loading, load capacitors (C9 and C10 in 1) of 16 pF each were appropriate for the layout of that particular board. The load specified for the crystal includes the load capacitors (C9, C10), the loading of the PHY pins (C_{PHY}), and the loading of the board itself (C_{BD}). The value of C_{PHY} is typically about 1 pF, and C_{BD} is typically 0.8 pF per centimeter of board etch; a typical board can have 3 pF to 6 pF or more. The load capacitors C9 and C10 combine as capacitors in series so that the total load capacitance is:

$$C_L = [(C9 \times C10)/(C9 + C10)] + C_{PHY} + C_{BD} \quad (2)$$

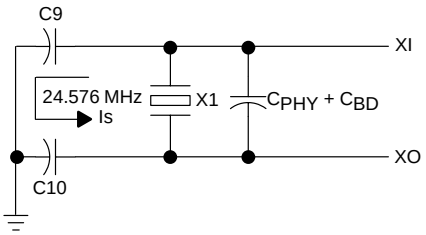


Figure 11. Load Capacitance for the TSB41LV01 PHY

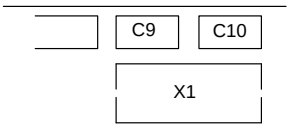


Figure 12. Recommended Crystal and Capacitor Layout

APPLICATION INFORMATION

crystal-selection (continued)

It is strongly recommended that part of the verification process for the design be to measure the frequency of the SYSCLK output of the PHY. This should be done with a frequency counter with an accuracy of 6 digits or better. If the SYSCLK frequency is more than the crystal's tolerance from 49.152 MHz, the load capacitance of the crystal may be varied to improve frequency accuracy. If the frequency is too high add more load capacitance; if the frequency is too low decrease load capacitance. Typically, changes should be done to both load capacitors (C9 and C10 above) at the same time, and both should be of the same value. Additional design details and requirements may be provided by the crystal vendor.

bus reset

In the TSB41LV01, the initiate bus reset (IBR) bit may be set to 1 in order to initiate a bus reset and initialization sequence. The IBR bit is located in PHY register 1, along with the root-holdoff (RHB) bit and gap-count register, as required by the P1394a Supplement (this configuration also maintains compatibility with older TI PHY designs which were based upon the suggested register set defined in Annex J of IEEE Std 1394-1995). Therefore, whenever the IBR bit is written, the RHB bit and gap-count are also necessarily written.

The RHB bit and gap-count may also be updated by PHY-config packets. The TSB41LV01 is P1394a compliant, and therefore both the reception and transmission of PHY-config packets cause the RHB and gap-count to be loaded, unlike older IEEE Std 1394-1995 compliant PHYs, which decode only received PHY-config packets.

The gap-count will be set to the maximum value of 63 after two consecutive bus resets without an intervening write to the gap-count, either by a write to PHY register 1 or by a PHY-config packet. This mechanism allows a PHY-config packet to be transmitted and then a bus reset initiated so as to verify that all nodes on the bus have updated their RHB bits and gap-count values, without having the gap-count set back to 63 by the bus reset. The subsequent connection of a new node to the bus, which initiates a bus reset, will then cause the gap-count of each node to be set to 63. Note, however, that if a subsequent bus reset is instead initiated by a write to register 1 to set the IBR bit, all other nodes on the bus will have their gap-count values set to 63, while this node's gap-count remains set to the value just loaded by the write to PHY register 1.

Therefore, in order to maintain consistent gap-counts throughout the bus, the following rules apply to the use of the IBR bit, RHB bit, and gap-count in PHY register 1:

- Following the transmission of a PHY-config packet, a bus reset must be initiated in order to verify that all nodes have correctly updated their RHB bits and gap-count values, and to ensure that a subsequent new connection to the bus will cause the gap-count to be set to 63 on all nodes in the bus. If this bus reset is initiated by setting the IBR bit to 1, the RHB bit and gap-count register must also be loaded with the correct values consistent with the just transmitted PHY-config packet. In the TSB41LV01, the RHB bit and gap-count will have been updated to their correct values upon the transmission of the PHY-config packet, and so these values may first be read from register 1 and then rewritten.
- Other than to initiate the bus reset which must follow the transmission of a PHY-config packet, whenever the IBR bit is set to 1 in order to initiate a bus reset, the gap-count value must also be set to 63 so as to be consistent with other nodes on the bus, and the RHB bit should be maintained with its current value.
- The PHY register 1 should not be written to except to set the IBR bit. The RHB bit and gap-count should not be written without also setting the IBR bit to 1.

PRINCIPLES OF OPERATION

bus reset (continued)

The TSB41LV01 is designed to operate with an LLC such as the Texas Instruments TSB12LV21, TSB12LV31, TSB12LV41, TSB12LV01, or TSB12LV22. Details of operation for the Texas Instruments LLC devices are found in the respective LLC data sheets. The following paragraphs describe the operation of the PHY-LLC interface.

The interface to the LLC consists of the SYSCLK, CTL0–CTL1, D0–D7, LREQ, LPS, C$\overline{\text{LKON}}$, and $\overline{\text{ISO}}$ terminals on the TSB41LV01, as shown in Figure 13.

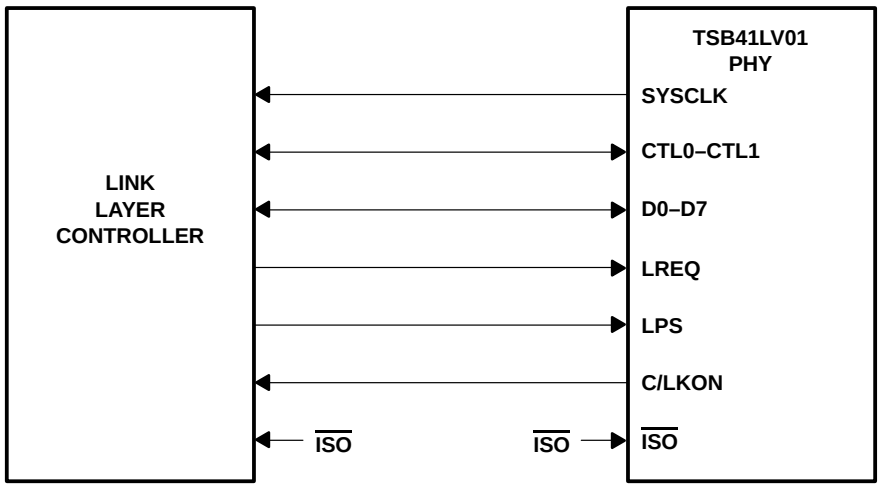


Figure 13. PHY-LLC Interface

The SYSCLK terminal provides a 49.152 MHz interface clock. All control and data signals are synchronized to, and sampled on, the rising edge of SYSCLK.

The CTL0 and CTL1 terminals form a bidirectional control bus, which controls the flow of information and data between the TSB41LV01 and LLC.

The D0–D7 terminals form a bidirectional data bus, which is used to transfer status information, control information, or packet data between the devices. The TSB41LV01 supports S100, S200, and S400 data transfers over the D0–D7 data bus. In S100 operation only the D0 and D1 terminals are used; in S200 operation only the D0–D3 terminals are used; and in S400 operation all D0–D7 terminals are used for data transfer. When the TSB41LV01 is in control of the D0–D7 bus, unused Dn terminals are driven low during S100 and S200 operations. When the LLC is in control of the D0–D7 bus, unused Dn terminals are ignored by the TSB41LV01.

The LREQ terminal is controlled by the LLC to send serial service requests to the PHY in order to request access to the serial-bus for packet transmission, read or write PHY registers, or control arbitration acceleration.

The LPS and C/LKON terminals are used for power management of the PHY and LLC. The LPS terminal indicates the power status of the LLC, and may be used to reset the PHY-LLC interface or to disable SYSCLK. The C/LKON terminal is used to send a wake-up notification to the LLC and to indicate an interrupt to the LLC when either LPS is inactive or the PHY register LCtrl bit is zero.

The $\overline{\text{ISO}}$ terminal is used to enable the output differentiation logic on the CTL0–CTL1 and D0–D7 terminals. Output differentiation is required when an Annex J type isolation barrier is implemented between the PHY and LLC.

The TSB41LV01 normally controls the CTL0–CTL1 and D0–D7 bidirectional buses. The LLC is allowed to drive these buses only after the LLC has been granted permission to do so by the PHY.

PRINCIPLES OF OPERATION

bus reset (continued)

There are four operations that may occur on the PHY-LLC interface: link service request, status transfer, data transmit, and data receive. The LLC issues a service request to read or write a PHY register, to request the PHY to gain control of the serial-bus in order to transmit a packet, or to control arbitration acceleration.

The PHY may initiate a status transfer either autonomously or in response to a register read request from the LLC.

The PHY initiates a receive operation whenever a packet is received from the serial-bus.

The PHY initiates a transmit operation after winning control of the serial-bus following a bus-request by the LLC. The transmit operation is initiated when the PHY grants control of the interface to the LLC.

The encoding of the CTL0–CTL1 bus is shown in Table 10 and Table 11.

Table 10. CTL Encoding When PHY has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	No activity (this is the default mode)
0	1	Status	Status information is being sent from the PHY to the LLC
1	0	Receive	An incoming packet is being sent from the PHY to the LLC
1	1	Grant	The LLC has been given control of the bus to send an outgoing packet

Table 11. CTL Encoding When LLC has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	The LLC releases the bus (transmission has been completed)
0	1	Hold	The LLC is holding the bus while data is being prepared for transmission, or indicating that another packet is to be transmitted (concatenated) without arbitrating
1	0	Transmit	An outgoing packet is being sent from the LLC to the PHY
1	1	Reserved	None

output differentiation

When an Annex J type isolation barrier is implemented between the PHY and LLC, the CTL0–CTL1, D0–D7, and LREQ signals must be digitally differentiated so that the isolation circuits function correctly. Digital differentiation is enabled on the TSB41LV01 when the $\overline{\text{ISO}}$ terminal is low.

The differentiation operates such that the output is driven either low or high for one clock period whenever the signal changes logic state, but otherwise places the output in a high-impedance state for as long as the signal logic state remains constant. On input, hysteresis buffers are used to convert the signal to the correct logic state when the signal is high-impedance; the biasing network of the Annex J type isolation circuit pulls the signal voltage level between the hysteresis thresholds of the input buffer so that the previous logic state is maintained.

The correspondence between output logic state and output signal level is illustrated in Figure 14.

PRINCIPLES OF OPERATION

bus reset (continued)

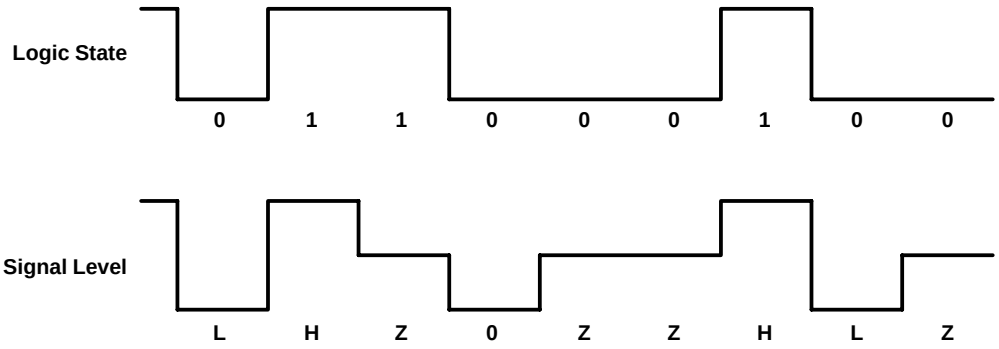


Figure 14. Input/Output Differentiation Logic

The TSB41LV01 implements differentiation circuitry functionally equivalent to that shown in Figure 15 on the bidirectional CTL0–CTL1and D0–D7 terminals. The TSB41LV01 also implements an input hysteresis buffer on the LREQ input to convert this signal to the correct logic level when differentiated. The LLC must also implement similar output differentiation and input hysteresis circuitry on its CTL and D terminals, and output differentiation circuitry on its LREQ terminal.

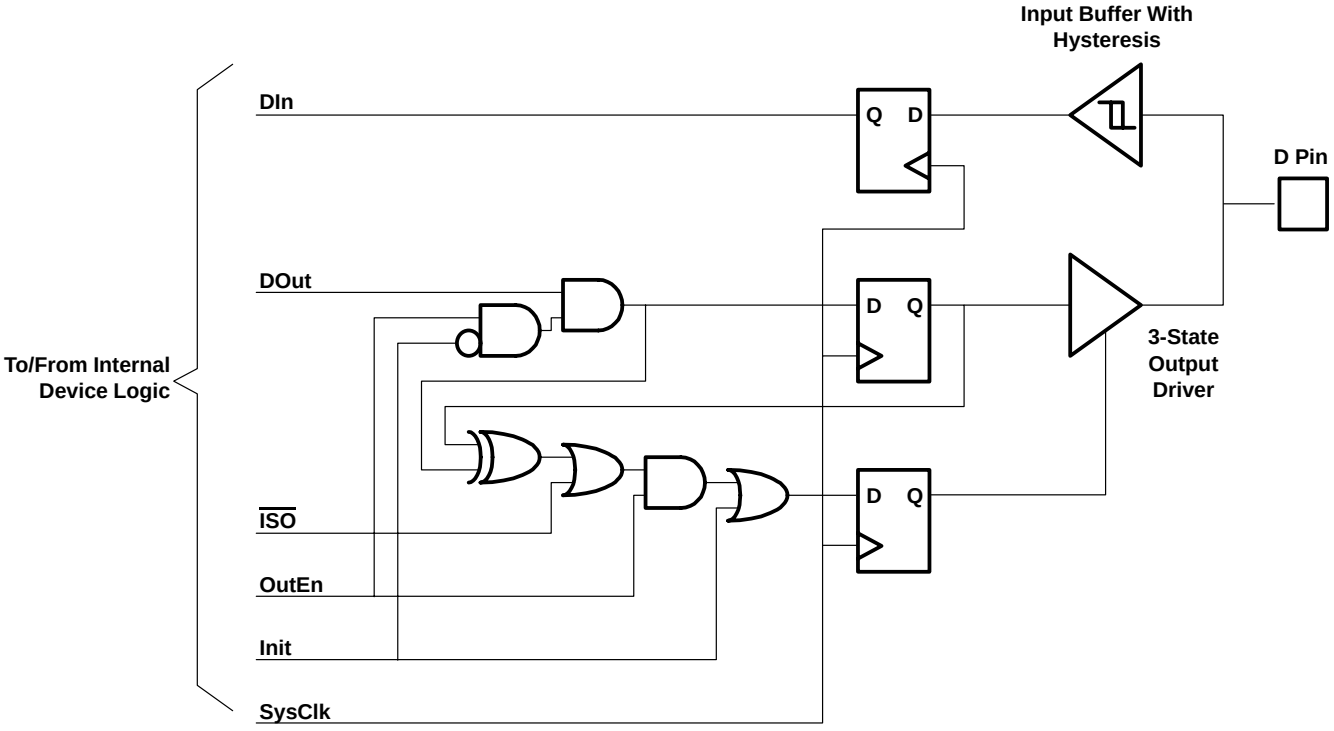


Figure 15. Input/Output Differentiation Logic

PRINCIPLES OF OPERATION

LLC service request

To request access to the bus, to read or write a PHY register, or to control arbitration acceleration, the LLC sends a serial bit stream on the LREQ terminal as shown in Figure 16. LREQ request stream 13.

NOTE: Each cell represents one clock sample time, and n is the number of bits in the request stream.

Figure 16. LREQ Request Stream

The length of the stream will vary depending on the type of request as shown in Table 12.

Table 12. Request Stream Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request	7 or 8
Read register request	9
Write register request	17
Acceleration control request	6

Regardless of the type of request, a start-bit of 1 is required at the beginning of the stream, and a stop-bit of 0 is required at the end of the stream. The second through fourth bits of the request stream indicate the type of the request. In the descriptions below, bit 0 is the most significant and is transmitted first in the request bit stream. The LREQ terminal is normally low.

Encoding for the request type is shown in Table 13.

Table 13. Request Type Encoding

LR1 – LR3	NAME	DESCRIPTION
000	ImmReq	Immediate bus request. Upon detection of idle, the PHY takes control of the bus immediately without arbitration.
001	IsoReq	Isochronous bus request. Upon detection of idle, the PHY arbitrates for the bus without waiting for a subaction gap.
010	PriReq	Priority bus request. The PHY arbitrates for the bus after a subaction gap, ignores the fair protocol.
011	FairReq	Fair bus request. The PHY arbitrates for the bus after a subaction gap, follows the fair protocol.
100	RdReg	The PHY returns the specified register contents through a status transfer.
101	WrReg	Write to the specified register.
110	AccelCtl	Enable or disable asynchronous arbitration acceleration.
111	Reserved	Reserved

PRINCIPLES OF OPERATION

LLC service request (continued)

For a bus request the length of the LREQ bit stream is 7 or 8 bits as shown in Table 14.

Table 14. Bus Request

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	Indicates the type of bus request. See Table 13.
4–6	Request Speed	Indicates the speed at which the PHY sends the data for this request. See Table 15 for the encoding of this field.
7	Stop Bit	Indicates the end of the transfer (always 0). If bit 6 is 0, this bit may be omitted.

The 3-bit request speed field used in bus requests is shown in Table 15.

Table 15. Bus Request Speed Encoding

LR4–LR6	DATA RATE
000	S100
010	S200
100	S400
All Others	Invalid

NOTE: The TSB41LV01 will accept a bus request with an invalid speed code and process the bus request normally. However, during packet transmission for such a request, the TSB41LV01 ignores any data presented by the LLC and transmits a null packet.

For a read register request the length of the LREQ bit stream is 9 bits as shown in Table 16.

Table 16. Read Register Request

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	A 100 indicating this is a read register request.
4–7	Address	Identifies the address of the PHY register to be read.
8	Stop Bit	Indicates the end of the transfer (always 0).

For a write register request the length of the LREQ bit stream is 17 bits as shown in Table 17.

Table 17. Write Register Request

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	A 101 indicating this is a write register request.
4–7	Address	Identifies the address of the PHY register to be written to.
8–15	Data	Gives the data that is to be written to the specified register address.
16	Stop Bit	Indicates the end of the transfer (always 0).

PRINCIPLES OF OPERATION

LLC service request (continued)

For an Acceleration Control Request the Length of the LREQ bit stream is 6 bits as shown in Table 18.

Table 18. Acceleration Control Request

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	A 110 indicating this is an acceleration control request.
4	Control	Asynchronous period arbitration acceleration is enabled if 1, and disabled if 0.
5	Stop Bit	Indicates the end of the transfer (always 0).

For fair or priority access, the LLC sends the bus request (FairReq or PriReq) at least one clock after the PHY-LLC interface becomes idle. If the CTL terminals are asserted to the receive state (’b10) by the PHY, then any pending fair or priority request is lost (cleared). Additionally, the PHY ignores any fair or priority requests if the receive state is asserted while the LLC is sending the request. The LLC may then reissue the request one clock after the next interface idle.

The cycle master node uses a priority bus request (PriReq) to send a cycle start message. After receiving or transmitting a cycle start message, the LLC can issue an isochronous bus request (IsoReq). The PHY clears an isochronous request only when the serial bus has been won.

To send an acknowledge packet, the LLC must issue an immediate bus request (ImmReq) during the reception of the packet addressed to it. This is required to minimize the idle gap between the end of the received packet and the start of the transmitted acknowledge packet. As soon as the receive packet ends, the PHY immediately grants control of the bus to the LLC. The LLC sends an acknowledgment to the sender unless the header CRC of the received packet is corrupted. In this case, the LLC does not transmit an acknowledge, but instead cancels the transmit operation and releases the interface immediately; the LLC must not use this grant to send another type of packet. After the interface is released the LLC may proceed with another request.

The LLC may make only one bus request at a time. Once the LLC issues any request for bus access (ImmReq, IsoReq, FairReq, or PriReq), it cannot issue another bus request until the PHY indicates that the bus request was lost (bus arbitration lost and another packet received), or won (bus arbitration won and the LLC granted control). The PHY ignores new bus requests while a previous bus request is pending. All bus requests are cleared upon a bus reset.

For write register requests, the PHY loads the specified data into the addressed register as soon as the request transfer is complete. For read register requests, the PHY returns the contents of the addressed register to the LLC at the next opportunity through a status transfer. If a received packet interrupts the status transfer, then the PHY continues to attempt the transfer of the requested register until it is successful. A write or read register request may be made at any time, including while a bus request is pending. Once a read register request is made, the PHY ignores further read register requests until the register contents are successfully transferred to the LLC. A bus reset does not clear a pending read register request.

The TSB41LV01 includes several arbitration acceleration enhancements, which allow the PHY to improve bus performance and throughput by reducing the number and length of inter-packet gaps. These enhancements include autonomous (flyby) isochronous packet concatenation, autonomous fair and priority packet concatenation onto acknowledge packets, and accelerated fair and priority request arbitration following acknowledge packets. The enhancements are enabled when the EAA bit in PHY register 5 is set.

PRINCIPLES OF OPERATION

LLC service request (continued)

The arbitration acceleration enhancements may interfere with the ability of the cycle master node to transmit the cycle start message under certain circumstances. The acceleration control request is therefore provided to allow the LLC to temporarily enable or disable the arbitration acceleration enhancements of the TSB41LV01 during the asynchronous period. The LLC typically disables the enhancements when its internal cycle counter rolls over indicating that a cycle start message is imminent, and then re-enables the enhancements when it receives a cycle start message. The acceleration control request may be made at any time, however, and is immediately serviced by the PHY. Additionally, a bus reset or isochronous bus request causes the enhancements to be re-enabled, if the EAA bit is set.

status transfer

A status transfer is initiated by the PHY when there is status information to be transferred to the LLC. The PHY waits until the interface is idle before starting the transfer. The transfer is initiated by the PHY asserting status (‘b01) on the CTL terminals, along with the first two bits of status information on the D[0:1] terminals. The PHY maintains CTL = status for the duration of the status transfer. The PHY may prematurely end a status transfer by asserting something other than status on the CTL terminals. This occurs if a packet is received before the status transfer completes. The PHY continues to attempt to complete the transfer until all status information has been successfully transmitted. There is at least one idle cycle between consecutive status transfers.

The PHY normally sends just the first four bits of status to the LLC. These bits are status flags that are needed by the LLC state machines. The PHY sends an entire 16-bit status packet to the LLC after a read register request, or when the PHY has pertinent information to send to the LLC or transaction layers. The only defined condition where the PHY automatically sends a register to the LLC is after self-ID, where the PHY sends the physical-ID register that contains the new node address. All status transfers are either 4 or 16 bits unless interrupted by a received packet. The status flags are considered to have been successfully transmitted to the LLC immediately upon being sent, even if a received packet subsequently interrupts the status transfer. Register contents are considered to have been successfully transmitted only when all 8 bits of the register have been sent. A status transfer is retried after being interrupted only if any status flags remain to be sent, or if a register transfer has not yet completed.

The definition of the bits in the status transfer are shown in Table 19.

Table 19. Status Bits

BIT(S)	NAME	DESCRIPTION
0	Arbitration reset gap	Indicates that the PHY has detected that the bus has been idle for an arbitration reset gap time (as defined in IEEE Std 1394-1995). This bit is used by the LLC in the busy/retry state machine.
1	Subaction gap	Indicates that the PHY has detected that the bus has been idle for a subaction gap time (as defined in IEEE Std 1394-1995). This bit is used by the LLC to detect the completion of an isochronous cycle.
2	Bus reset	Indicates that the PHY has entered the bus reset start state.
3	Interrupt	Indicates that a PHY interrupt event has occurred. An interrupt event may be a configuration time-out, cable-power voltage falling too low, a state time-out, or a port status change.
4–7	Address	This field holds the address of the PHY register whose contents are being transferred to the LLC.
8–15	Data	This field holds the register contents.

status transfer (continued)

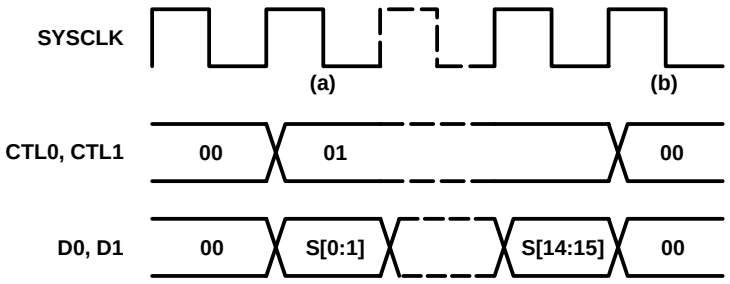


Figure 17. Status Transfer Timing

The sequence of events for a status transfer is as follows:

a. Status transfer initiated. The PHY indicates a status transfer by asserting status on the CTL lines along with the status data on the D0 and D1 lines (only 2 bits of status are transferred per cycle). Normally (unless interrupted by a receive operation), a status transfer will be either 2 or 8 cycles long. A 2-cycle (4-bit) transfer occurs when only status information is to be sent. An 8-cycle (16-bit) transfer occurs when register data is to be sent in addition to any status information.

b. Status transfer terminated. The PHY normally terminates a status transfer by asserting idle on the CTL lines. The PHY may also interrupt a status transfer at any cycle by asserting receive on the CTL lines to begin a receive operation. The PHY shall assert at least one cycle of idle between consecutive status transfers.

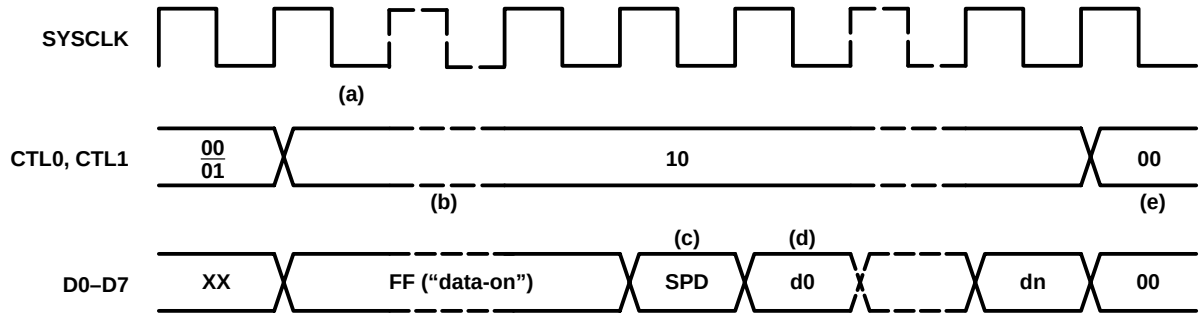
PRINCIPLES OF OPERATION

receive

Whenever the PHY detects the data-prefix state on the serial bus, it initiates a receive operation by asserting receive on the CTL terminals and a logic 1 on each of the D terminals (data-on indication). The PHY indicates the start of a packet by placing the speed code (encoded as shown in Table 21 on the D terminals, followed by packet data. The PHY holds the CTL terminals in the receive state until the last symbol of the packet has been transferred. The PHY indicates the end of packet data by asserting idle on the CTL terminals. All received packets are transferred to the LLC. Note that the speed code is part of the PHY-LLC protocol and is not included in the calculation of CRC or any other data protection mechanisms.

It is possible for the PHY to receive a null packet, which consists of the data-prefix state on the serial bus followed by the data-end state, without any packet data. A null packet is transmitted whenever the packet speed exceeds the capability of the receiving PHY, or whenever the LLC immediately releases the bus without transmitting any data. In this case, the PHY will assert receive on the CTL terminals with the data-on indication (all 1s) on the D terminals, followed by idle on the CTL terminals, without any speed code or data being transferred. In all cases, the TSB41LV01 sends at least one data-on indication before sending the speed code or terminating the receive operation.

The TSB41LV01 also transfers its own self-ID packet, transmitted during the self-ID phase of bus initialization, to the LLC. This packet it transferred to the LLC just as any other received self-ID packet.



NOTE A: SPD = Speed code, see Table 20 d0–dn = Packet data

Figure 18. Normal Packet Reception Timing

The sequence of events for a normal packet reception is as follows:

a. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation may interrupt a status transfer operation that is in progress so that the CTL lines may change from status to receive without an intervening idle.

b. Data-on indication. The PHY asserts the data-on indication code on the D lines for one or more cycles preceding the speed-code.

c. Speed-code. The PHY indicates the speed of the received packet by asserting a speed-code on the D lines for one cycle immediately preceding packet data. The link decodes the speed-code on the first receive cycle for which the D lines are not the data-on code. If the speed-code is invalid, or indicates a speed higher than that which the link is capable of handling, the link should ignore the subsequent data.

d. Receive data. Following the data-on indication (if any) and the speed-code, the PHY asserts packet data on the D lines with receive on the CTL lines for the remainder of the receive operation.

e. Receive operation terminated. The PHY terminates the receive operation by asserting idle on the CTL lines. The PHY asserts at least one cycle of idle following a receive operation.

PRINCIPLES OF OPERATION

receive (continued)

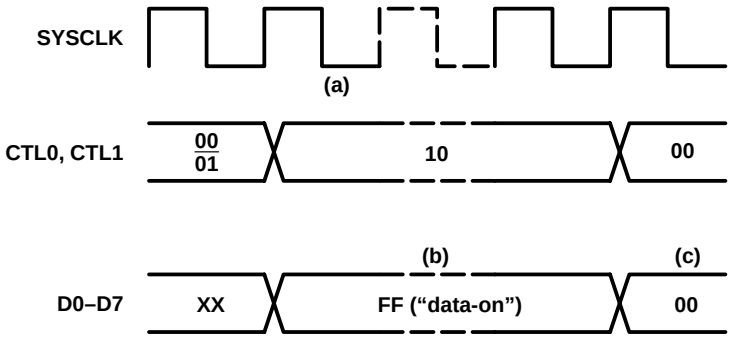


Figure 19. Null Packet Reception Timing

The sequence of events for a null packet reception is as follows:

a. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation may interrupt a status transfer operation that is in progress so that the CTL lines may change from status to receive without an intervening idle.

b. Data-on indication. The PHY asserts the data-on indication code on the D lines for one or more cycles.

c. Data-on indication. The PHY asserts the data-on indication code on the D lines for one or more cycles.

Table 20. Receive Speed Codes

D0–D7	DATA RATE
00XX XXXX	S100
0100 XXXX	S200
0101 0000	S400
1YYY YYYY	*data-on* indication

NOTE: X = Output as 0 by PHY, ignored by LLC.
Y = Output as 1 by PHY, ignored by LLC.

transmit

When the LLC issues a bus request through the LREQ terminal, the PHY arbitrates to gain control of the bus. If the PHY wins arbitration for the serial bus, the PHY-LLC interface bus is granted to the LLC by asserting the Grant state (’b11) on the CTL terminals for one SYSCLK cycle, followed by idle for one clock cycle. The LLC then takes control of the bus by asserting either idle (’b00), hold (’b01) or transmit (’b10) on the CTL terminals. Unless the LLC is immediately releasing the interface, the LLC may assert the idle state for at most one clock before it must assert either hold or transmit on the CTL terminals. The hold state is used by the LLC to retain control of the bus while it prepares data for transmission. The LLC may assert hold for zero or more clock cycles (i.e., the LLC need not assert hold before transmit). The PHY asserts data-prefix on the serial bus during this time.

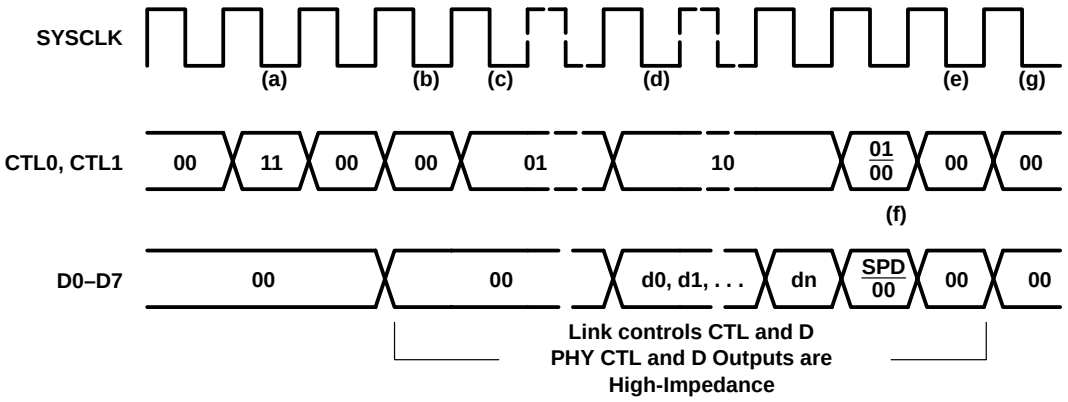
When the LLC is ready to send data, the LLC asserts transmit on the CTL terminals as well as sending the first bits of packet data on the D lines. The transmit state is held on the CTL terminals until the last bits of data have been sent. The LLC then asserts either hold or idle on the CTL terminals for one clock cycle, and then asserts idle for one additional cycle before releasing the interface bus and placing its CTL and D terminals in high-impedance. The PHY then regains control of the interface bus.

The hold state asserted at the end of packet transmission indicates to the PHY that the LLC requests to send another packet (concatenated packet) without releasing the serial bus. The PHY responds to this concatenation request by waiting the required minimum packet separation time and then asserting grant as before. This function may be used to send a unified response after sending an acknowledge, or to send consecutive isochronous packets during a single isochronous period. Unless multispeed concatenation is enabled, all packets transmitted during a single bus ownership must be of the same speed (since the speed of the packet is set before the first packet). If multispeed concatenation is enabled (when the EMSC bit of PHY register 5 is set), the LLC must specify the speed code of the next concatenated packet on the D terminals when it asserts hold on the CTL terminals at the end of a packet. The encoding for this speed code is the same as the speed code that precedes received packet data as given in Table 21.

After sending the last packet for the current bus ownership, the LLC releases the bus by asserting idle on the CTL terminals for two clock cycles. The PHY begins asserting idle on the CTL terminals one clock after sampling idle from the link. Note that whenever the D and CTL terminals change direction between the PHY and the LLC, there is an extra clock period allowed so that both sides of the interface can operate on registered versions of the interface signals.

PRINCIPLES OF OPERATION

transmit (continued)



NOTE A: SPD = Speed code, see Table 20 d0–dn = Packet data

Figure 20. Normal Packet Transmission Timing

The sequence of events for a normal packet transmission is as follows:

a. Transmit operation initiated. The PHY asserts grant on the CTL lines followed by idle to hand over control of the interface to the link so that the link may transmit a packet. The PHY releases control of the interface (i.e., it places its CTL and D outputs in a high-impedance state) following the idle cycle.

b. Optional idle cycle. The link may assert at most one idle cycle preceding assertion of either hold or transmit. This idle cycle is optional; the link is not required to assert idle preceding either hold or transmit.

c. Optional Hold cycles. The link may assert hold for up to 47 cycles preceding assertion of transmit. These hold cycle(s) are optional; the link is not required to assert hold preceding transmit.

d. Transmit data. When data is ready to be transmitted, the link asserts transmit on the CTL lines along with the data on the D lines.

e. Transmit operation terminated. The transmit operation is terminated by the link asserting hold or idle on the CTL lines. The link asserts hold to indicate that the PHY is to retain control of the serial bus in order to transmit a concatenated packet. The link asserts idle to indicate that packet transmission is complete and the PHY may release the serial bus. The link then asserts idle for one more cycle following this cycle of hold or idle before releasing the interface and returning control to the PHY.

f. Concatenated packet speed-code. If multispeed concatenation is enabled in the PHY, the link shall assert a speed-code on the D lines when it asserts hold to terminate packet transmission. This speed-code indicates the transmission speed for the concatenated packet that is to follow. The encoding for this concatenated packet speed-code is the same as the encoding for the received packet speed-code (see Table 21). The link may not concatenate an S100 packet onto any higher-speed packet.

g. After regaining control of the interface, the PHY asserts at least one cycle of idle before any subsequent status transfer, receive operation, or transmit operation.

PRINCIPLES OF OPERATION

transmit (continued)

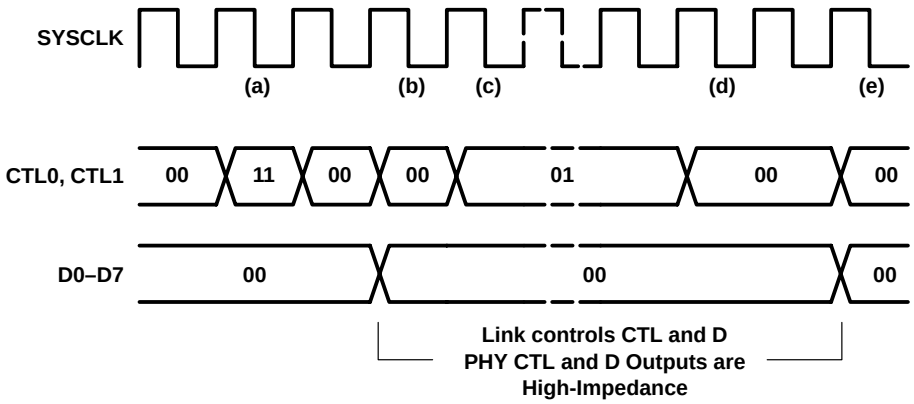


Figure 21. Cancelled/Null Packet Transmission

The sequence of events for a cancelled/null packet transmission is as follows:

a. Transmit operation initiated. PHY asserts grant on the CTL lines followed by idle to hand over control of the interface to the link.

b. Optional idle cycle. The link may assert at most one idle cycle preceding assertion of hold. This idle cycle is optional; the link is not required to assert idle preceding hold.

c. Optional hold cycles. The link may assert hold for up to 47 cycles preceding assertion of idle. These hold cycle(s) are optional; the link is not required to assert hold preceding idle.

d. Null transmit termination. The null transmit operation is terminated by the link asserting two cycles of idle on the CTL lines and then releasing the interface and returning control to the PHY. Note that the link may assert idle for a total of 3 consecutive cycles if it asserts the optional first idle cycle but does not assert hold. (It is recommended that the link assert 3 cycles of idle to cancel a packet transmission if no hold cycles are asserted. This guarantees that either the link or PHY controls the interface in all cycles.)

e. After regaining control of the interface, the PHY shall assert at least one cycle of idle before any subsequent status transfer, receive operation, or transmit operation.

interface reset and disable

The LLC controls the state of the PHY-LLC interface using the LPS signal. The interface may be placed into a reset state, a disabled state, or be made to initialize and then return to normal operation. When the interface is not operational (whether reset, disabled, or in the process of initialization) the PHY cancels any outstanding bus request or register read request, and ignores any requests made via the LREQ line. Additionally, any status information generated by the PHY are not queued and do not cause a status transfer upon restoration of the interface to normal operation.

The LPS signal may be either a level signal or a pulsed signal, depending upon whether the PHY-LLC interface is a direct connection or is made across an isolation barrier. When an isolation barrier exists between the PHY and LLC (whether of the TI bus-holder type or Annex J type) the LPS signal must be pulsed. In a direct connection, the LPS signal may be either a pulsed or a level signal. Timing parameters for the LPS signal are given in Table 21.

PRINCIPLES OF OPERATION

interface reset and disable (continued)

Table 21. LPS Timing Parameters

PARAMETER	DESCRIPTION		MIN	MAX	UNIT
T_{LPSL}	LPS low time (when pulsed)†		0.09	2.60	µs
T_{LPSH}	LPS high time (when pulsed)†		0.021	2.60	µs
	LPS duty cycle (when pulsed)‡		20	55	%
T_{LPS_RESET}	Time for PHY to recognize LPS deasserted and reset the interface		2.60	2.68	µs
$T_{LPS\_DISABLE}$	Time for PHY to recognize LPS deasserted and disable the interface		26.03	26.11	µs
$T_{RESTORE}$	Time to permit optional isolation circuits to restore during an interface reset		15	23§	µs
$T_{CLK\_ACTIVATE}$	Time for SYSCLK to be activated from reassertion of LPS	PHY not in low-power state		60	ns
		PHY in low-power state	5.3	7.3	ms

† The specified T_{LPSL} and T_{LPSH} times are worst-case values appropriate for operation with the TSB41LV01. These values are broader than those specified for the same parameters in the P1394a Supplement (i.e., an implementation of LPS that meets the requirements of P1394a will operate correctly with the TSB41LV01).

‡ A pulsed LPS signal must have a duty cycle (ratio of T_{LPSH} to cycle period) in the specified range to ensure proper operation when using an isolation barrier on the LPS signal (e.g., as shown in Figure 8).

§ The maximum value for $T_{RESTORE}$ does not apply when the PHY-LLC interface is disabled, in which case an indefinite time may elapse before LPS is reasserted. Otherwise, in order to reset but not disable the interface it is necessary that the LLC ensure that LPS is deasserted for less than $T_{LPS\_DISABLE}$

The LLC requests that the interface be reset by deasserting the LPS signal and terminating all bus and request activity. When the PHY observes that LPS has been deasserted for T_{LPS_RESET}, it resets the interface. When the interface is in the reset state, the PHY sets its CTL and D outputs in the logic 0 state and ignores any activity on the LREQ signal. The timing for interface reset is shown in Figure 22 and Figure 23.

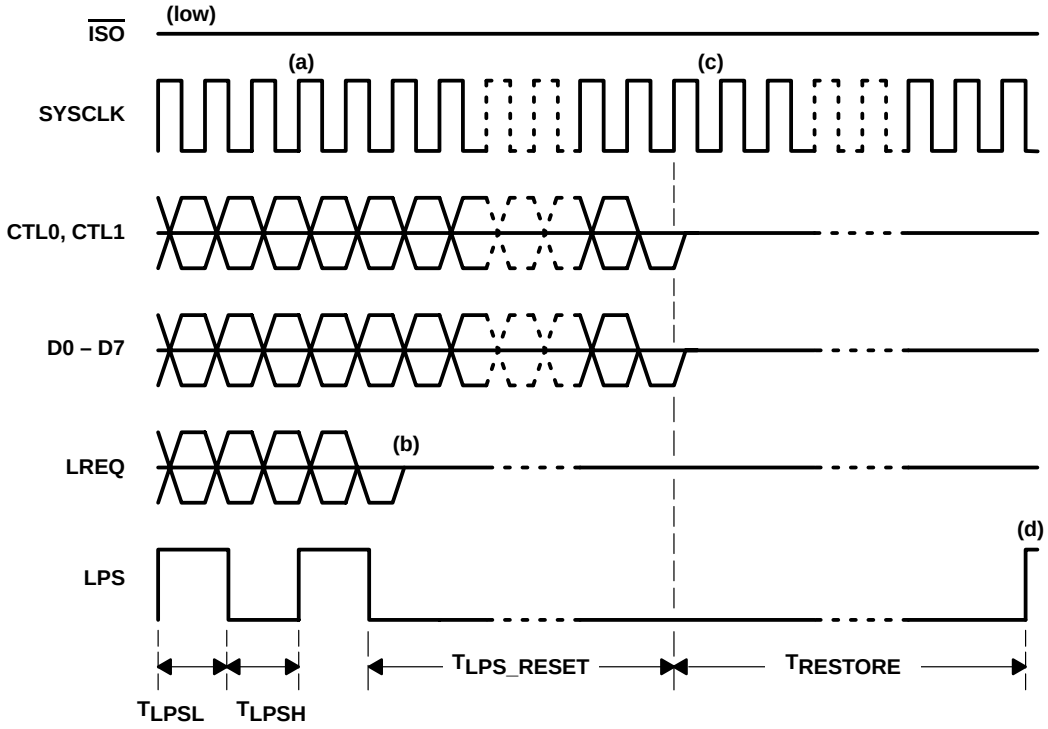


Figure 22. Interface Reset, $\overline{ISO}$ Low

PRINCIPLES OF OPERATION

interface reset and disable (continued)

The sequence of events for resetting the PHY-LLC interface when it is in the differentiated mode of operation ($\overline{ISO}$ pin is low) is as follows:

a. Normal operation. Interface is operating normally, with LPS active, SYSCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line.

b. LPS deasserted. The LLC deasserts the LPS signal and, within 1.0 μs, terminates any request or interface bus activity, and places its LREQ, CTL, and D outputs into a high-impedance state (the LLC should terminate any output signal activity such that signals end in a logic 0 state).

c. Interface reset. After T_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and places its CTL and D outputs into a high-impedance state (the PHY terminates any output signal activity such that signals end in a logic 0 state). The PHY-LLC interface is now in the reset state.

d. Interface restored. After the minimum $T_{RESTORE}$ time, the LLC may again assert LPS active. (The minimum $T_{RESTORE}$ interval provides sufficient time for the biasing networks used in Annex J type isolation barrier circuits to stabilize and reach a quiescent state if the isolation barrier has somehow become unbalanced.) When LPS is asserted, the interface is initialized as described in Figure 23.

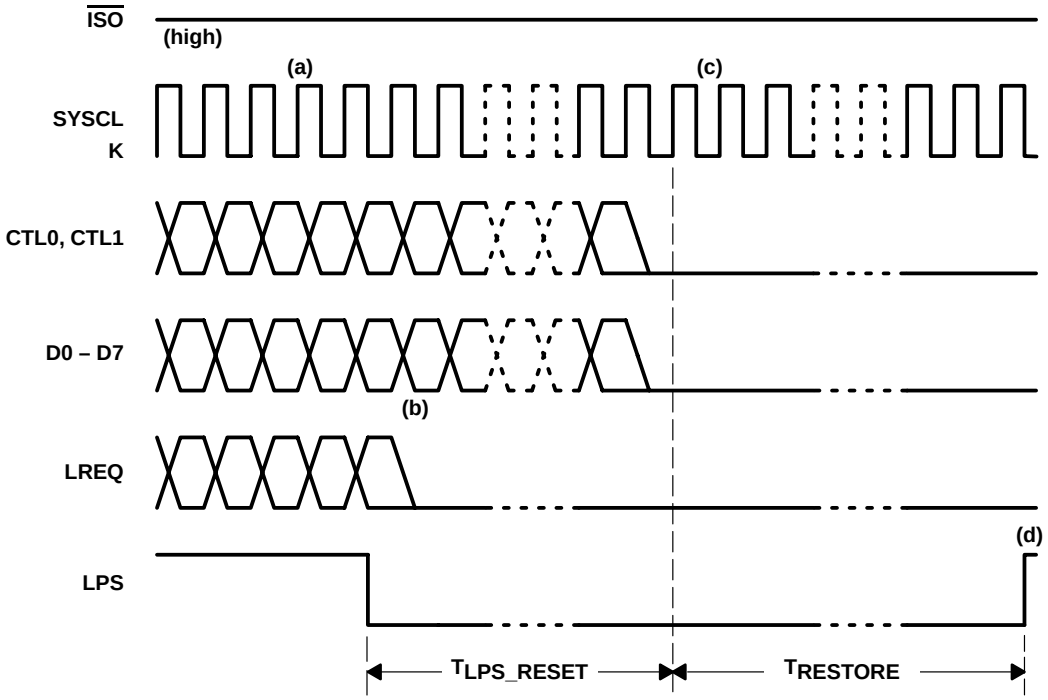


Figure 23. Interface Disable, $\overline{ISO}$ High

PRINCIPLES OF OPERATION

interface reset and disable (continued)

The sequence of events for resetting the PHY-LLC interface when it is in the nondifferentiated mode of operation ($\overline{ISO}$ pin is high) is as follows:

a. Normal operation. Interface is operating normally, with LPS asserted, SYSCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line. In the above diagram, the LPS signal is shown as a non-pulsed level signal. However, it is permissible to use a pulsed signal for LPS in a direct connection between the PHY and LLC; a pulsed signal is required when using an isolation barrier (whether of the TI bus holder type or Annex J type).

b. LPS deasserted. The LLC deasserts the LPS signal and, within 1.0 μs, terminates any request or interface bus activity, places its CTL and D outputs into a high-impedance state, and drives its LREQ output low.

c. Interface reset. After T_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and drives its CTL and D outputs low. The PHY-LLC interface is now in the reset state.

d. Interface restored. After the minimum $T_{RESTORE}$ time, the LLC may again assert LPS active. When LPS is asserted, the interface is initialized as described below.

If the LLC continues to keep the LPS signal deasserted, it requests that the interface be disabled. The PHY disables the interface when it observes that LPS has been deasserted for $T_{LPS\_DISABLE}$. When the interface is disabled, the PHY sets its CTL and D outputs as stated above for interface reset, but also stops SYSCLK activity. The interface is also placed into the disabled condition upon a hardware reset of the PHY. The timing for interface disable is shown in Figure 23 and Figure 24.

When the interface is disabled, the PHY enters a low-power state if none of its ports is active.

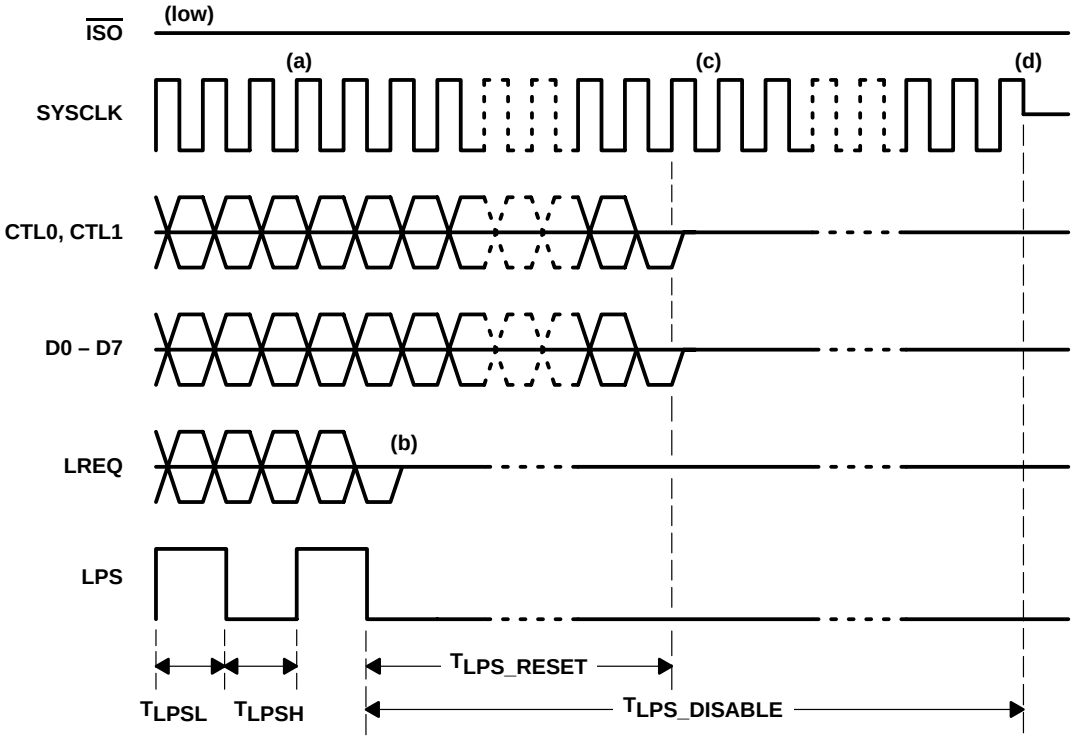


Figure 24. Interface Disable, $\overline{ISO}$ Low

PRINCIPLES OF OPERATION

interface reset and disable (continued)

The sequence of events for disabling the PHY-LLC interface when it is in the differentiated mode of operation ($\overline{ISO}$ pin is low) is as follows:

a. Normal operation. Interface is operating normally, with LPS active, SYSCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line.

b. LPS deasserted. The LLC deasserts the LPS signal and, within 1.0 μs, terminates any request or interface bus activity, and places its LREQ, CTL, and D outputs into a high-impedance state (the LLC should terminate any output signal activity such that signals end in a logic 0 state).

c. Interface reset. After T_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and places its CTL and D outputs into a high-impedance state (the PHY terminates any output signal activity such that signals end in a logic 0 state). The PHY-LLC interface is now in the reset state.

d. Interface disabled. If the LPS signal remain inactive for $T_{LPS\_DISABLE}$ time, the PHY terminates SYSCLK activity by placing the SYSCLK output into a high-impedance state. The PHY-LLC interface is now in the disabled state.

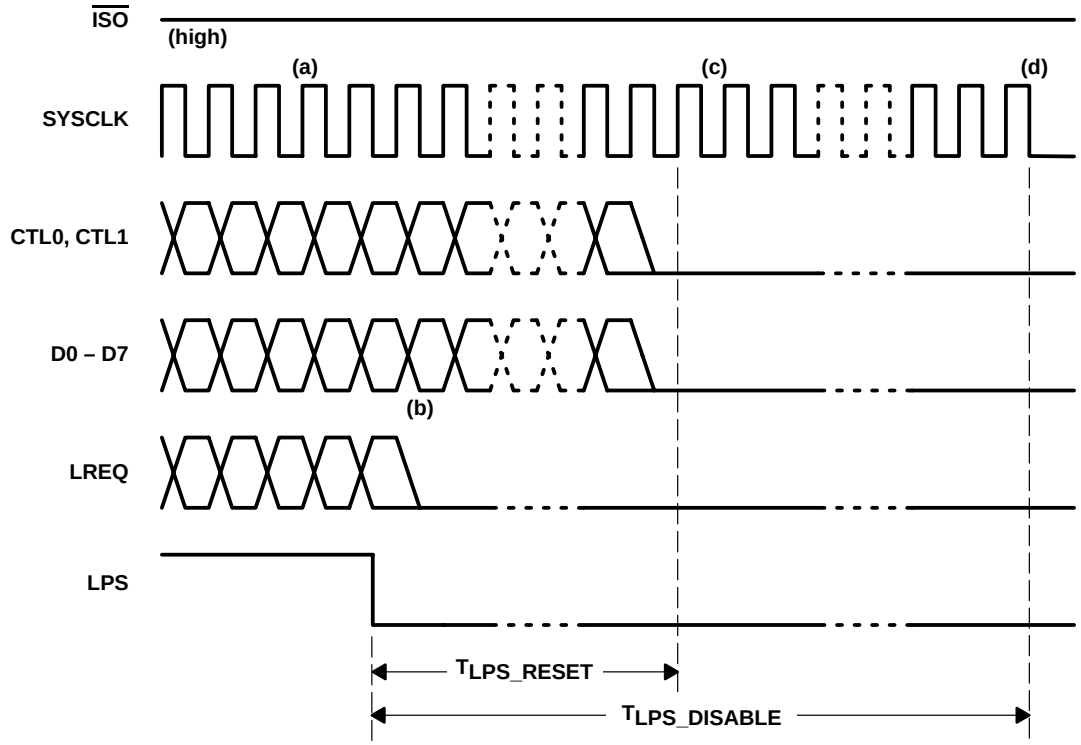


Figure 25. Interface Disable, $\overline{ISO}$ High

PRINCIPLES OF OPERATION

interface reset and disable (continued)

The sequence of events for disabling the PHY-LLC interface when it is in the nondifferentiated mode of operation ($\overline{ISO}$ pin is high) is as follows:

a. Normal operation. Interface is operating normally, with LPS active, SYSCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line.

b. LPS deasserted. The LLC deasserts the LPS signal and, within 1.0 μs, terminates any request or interface bus activity, places its CTL and D outputs into a high-impedance state, and drives its LREQ output low.

c. Interface reset. After T_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and drives its CTL and D outputs low. The PHY-LLC interface is now in the reset state.

d. Interface disabled. If the LPS signal remain inactive for $T_{LPS\_DISABLE}$ time, the PHY terminates SYSCLK activity by driving the SYSCLK output low. The PHY-LLC interface is now in the disabled state.

After the interface has been reset, or reset and then disabled, the interface is initialized and restored to normal operation when LPS is reasserted by the LLC. The timing for interface initialization is shown in Figure 26 and Figure 27.

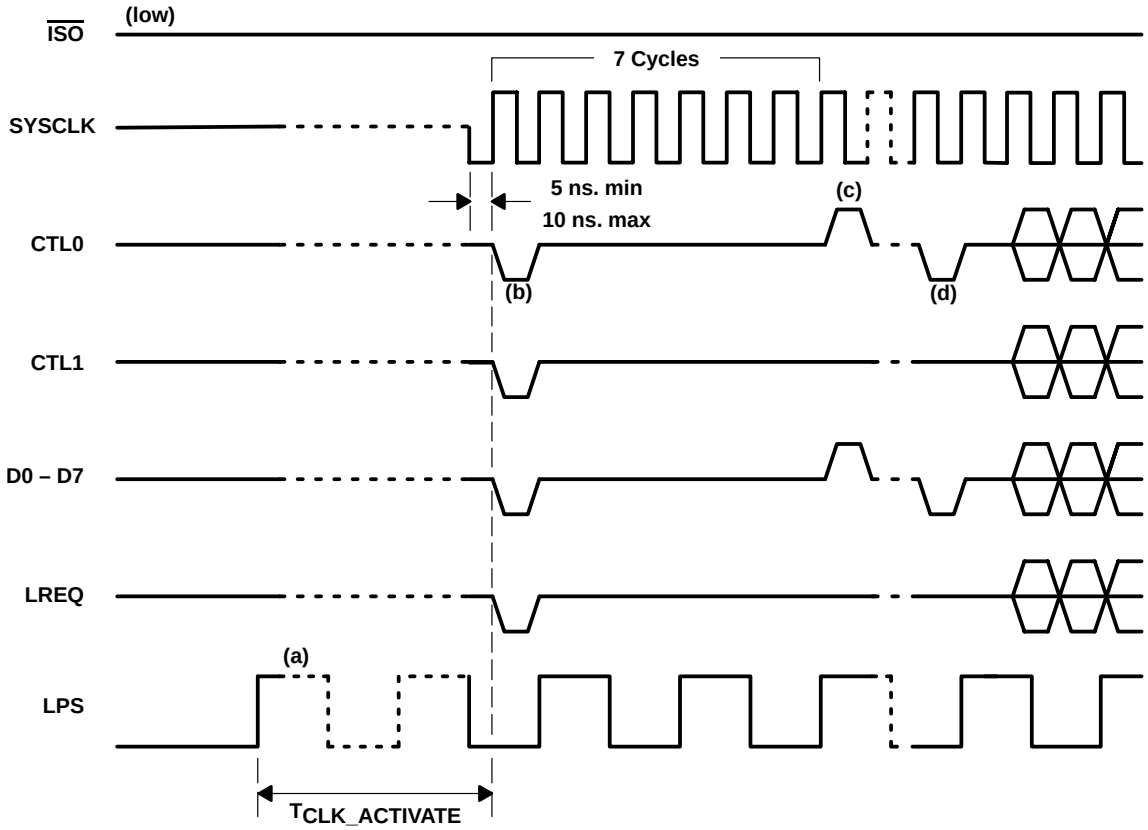


Figure 26. Interface Initialization, $\overline{ISO}$ Low

PRINCIPLES OF OPERATION

interface reset and disable (continued)

The sequence of events for initialization of the PHY-LLC interface when the interface is in the differentiated mode of operation ($\overline{ISO}$ pin is low) is as follows:

a. LPS reasserted. After the interface has been in the reset or disabled state for at least the minimum $T_{RESTORE}$ time, the LLC causes the interface to be initialized and restored to normal operation by reactivating the LPS signal. (In the above diagram, the interface is shown in the disabled state with SYSCLK high-impedance inactive. However, the interface initialization sequence described here is also executed if the interface is merely reset but not yet disabled.)

b. SYSCLK activated. If the interface is disabled, the PHY reactivates its SYSCLK output when it detects that LPS has been reasserted. If the PHY has entered a low-power state, it takes between 5.3 ms and 7.3 ms for SYSCLK to be restored; if the PHY is not in a low-power state, SYSCLK is restored within 60 ns. The PHY commences SYSCLK activity by driving the SYSCLK output low for half a cycle. Thereafter, the SYSCLK output is a 50% duty cycle square wave with a frequency of 49.152 MHz ±100 ppm (period of 20.345 ns). Upon the first full cycle of SYSCLK, the PHY drives the CTL and D pins low for one cycle. The LLC is also required to drive its CTL, D, and LREQ outputs low during one of the first six cycles of SYSCLK (this is shown as occurring in the first SYSCLK cycle in Figure 26).

c. Receive indicated. Upon the eighth SYSCLK cycle following reassertion of LPS, the PHY asserts the receive state on the CTL lines and the data-on indication (all ones) on the D lines for one or more cycles (because the interface is in the differentiated mode of operation, the CTL and D lines are in the high-impedance state after the first cycle).

d. Initialization complete. The PHY asserts the idle state on the CTL lines and logic 0 on the D lines. This indicates that the PHY-LLC interface initialization is complete and normal operation may commence. The PHY now accepts requests from the LLC via the LREQ line.

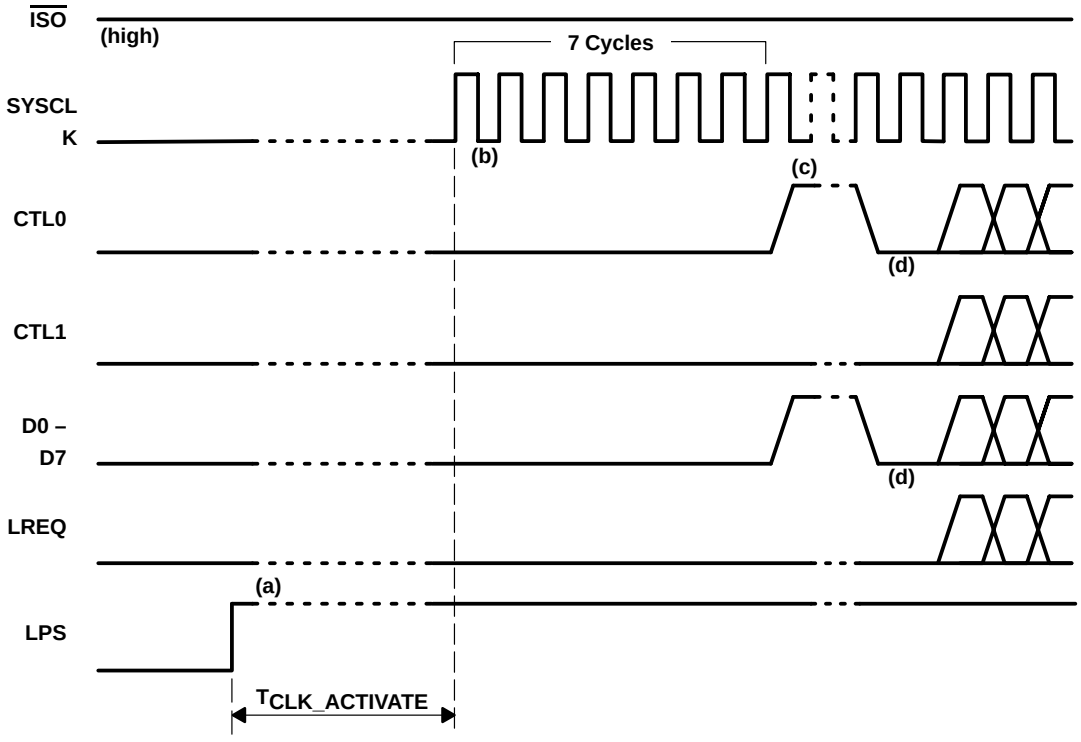
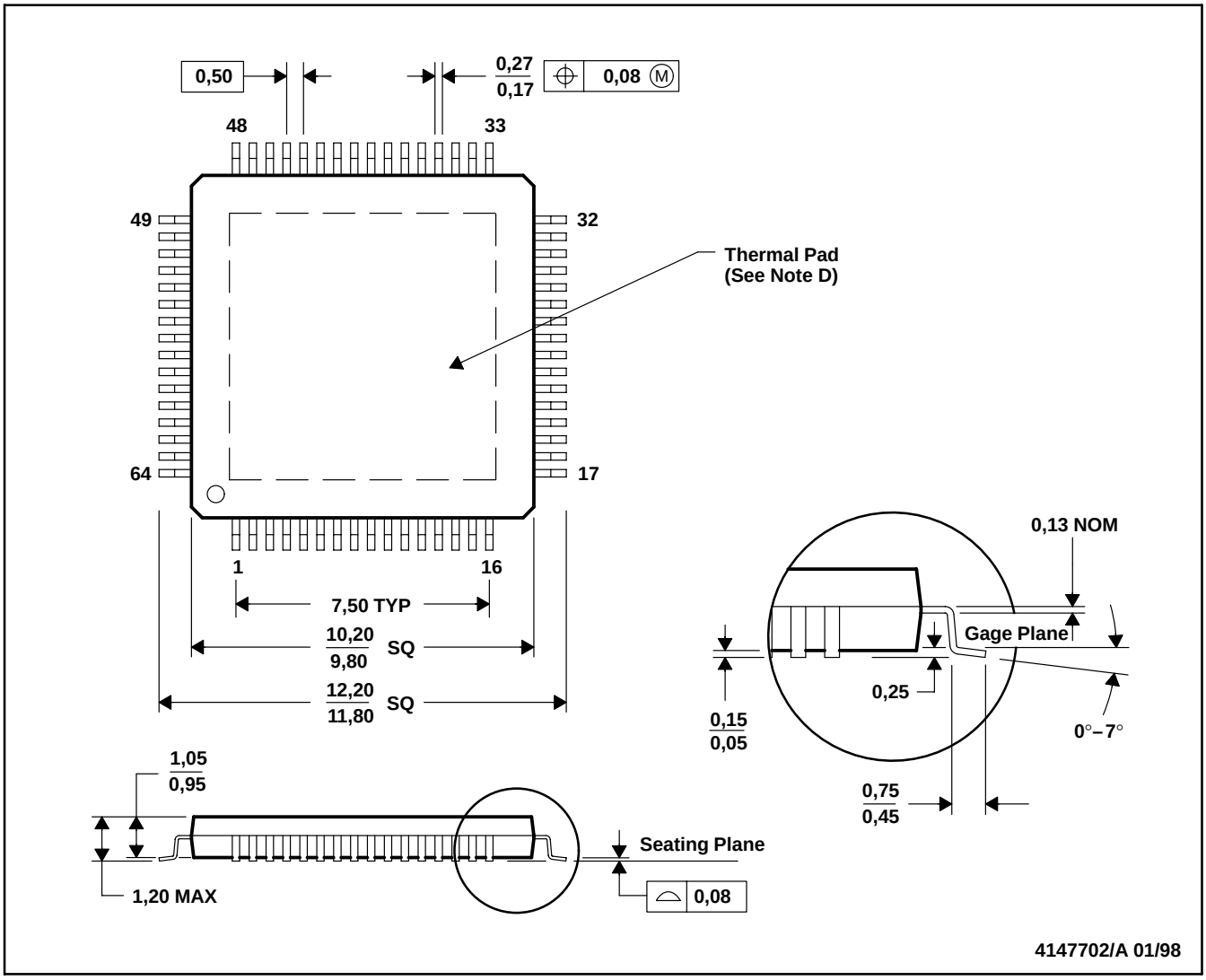


Figure 27. Interface Initialization, $\overline{ISO}$ High

MECHANICAL DATA

PAP (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TSB41LV01PAP	OBSOLETE	HTQFP	PAP	64		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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