

# MACH215-12/15/20

Lattice/Vantis

## High-Density EE CMOS Programmable Logic

### DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 32 Output Macrocells
- 32 Input Macrocells
- Product terms for:
  - Individual flip-flop clock
  - Individual asynchronous reset, preset
  - Individual output enable
- 12 ns  $t_{PD}$  Commercial  
14.5 ns  $t_{PD}$  Industrial
- 67 MHz  $f_{CNT}$
- 38 Inputs with pull-up resistors
- 32 Outputs
- 64 Flip-flops
- For asynchronous and synchronous applications
- 4 "PAL22RA8" blocks with buried macrocells
- Pin-compatible with MACH110, MACH111, MACH210, and MACH211

### GENERAL DESCRIPTION

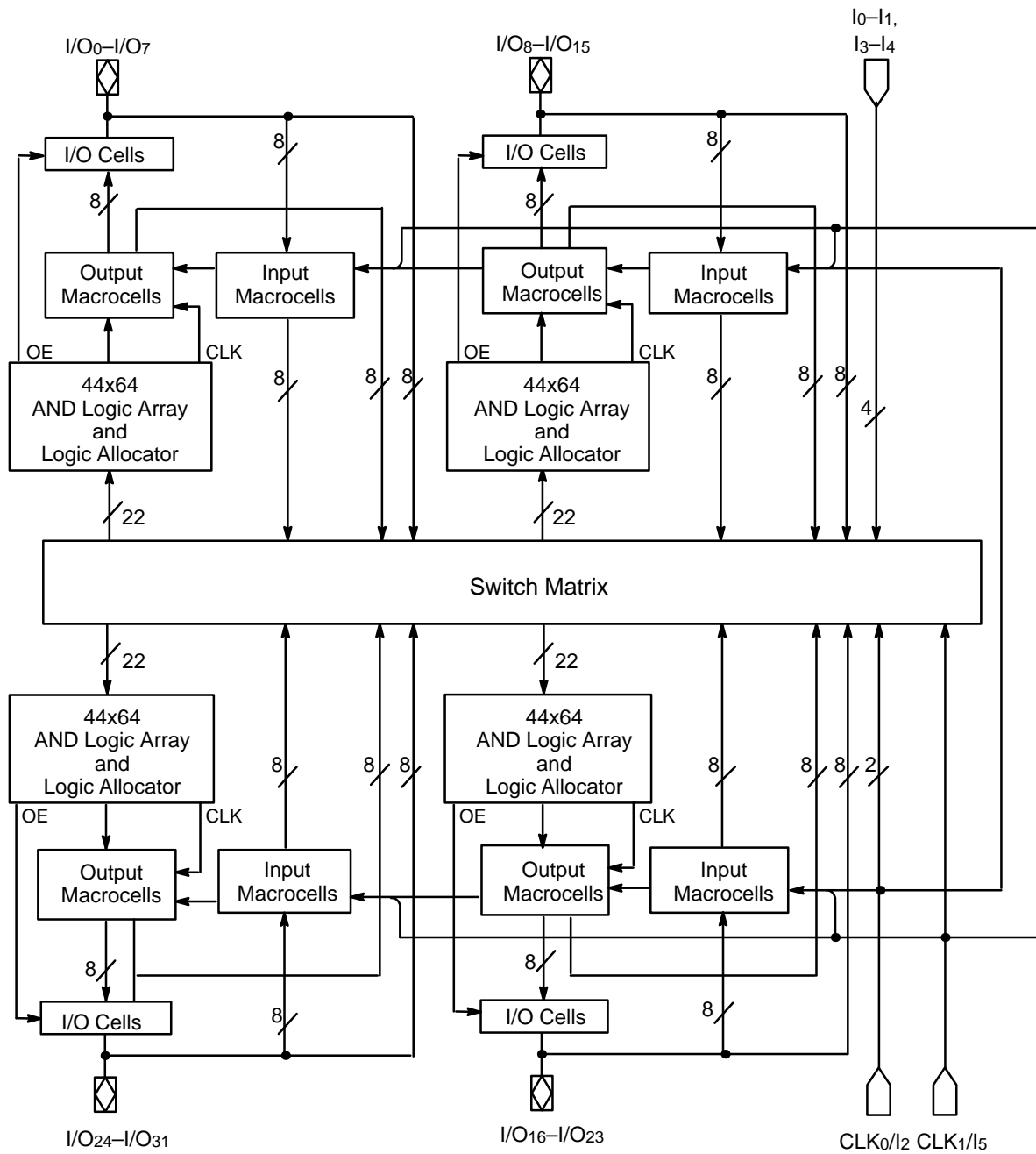
The MACH215 is a member of the high-performance EE CMOS MACH device family. This device has approximately three times the capability of the popular PAL20RA10 without loss of speed. This device is designed for use in asynchronous as well as synchronous applications.

The MACH215 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22RA8" structures complete with product-term arrays and programmable macrocells, individual register control product terms, and input registers. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH215 has two kinds of macrocell: output and input. The MACH215 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. Each macrocell has its own dedicated clock, asynchronous reset, and asynchronous preset control. The polarity of the clock signal is programmable. All output macrocells can be connected to an I/O cell.

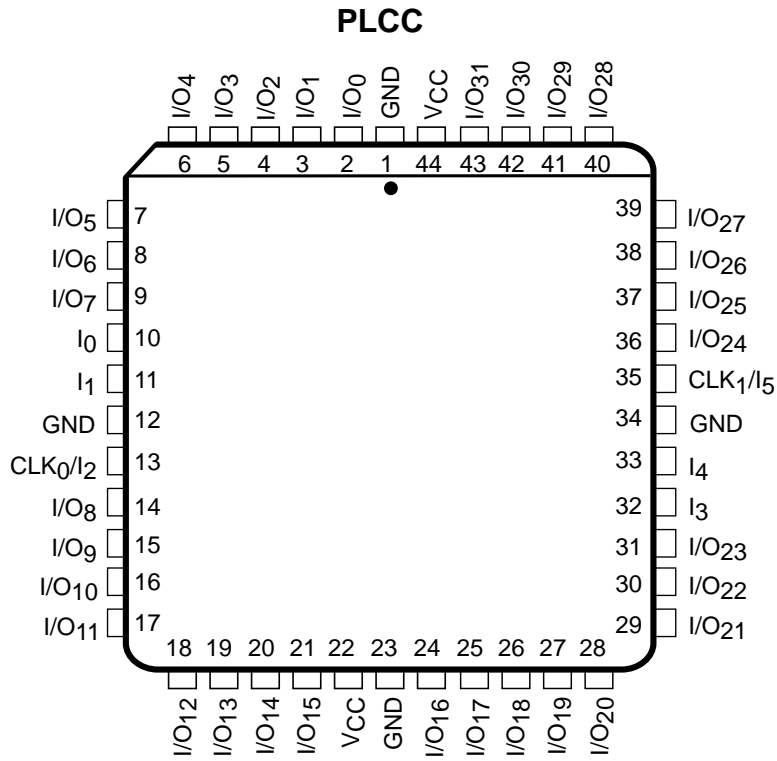
The MACH215 has dedicated input macrocells which provide input registers or latches for synchronizing input signals and reducing setup time requirements.

# BLOCK DIAGRAM



16751E-1

**CONNECTION DIAGRAM**  
**Top View**



16751E-2

**Note:**  
*Pin-compatible with MACH110, MACH111, MACH210, and MACH211.*

**PIN DESIGNATIONS**

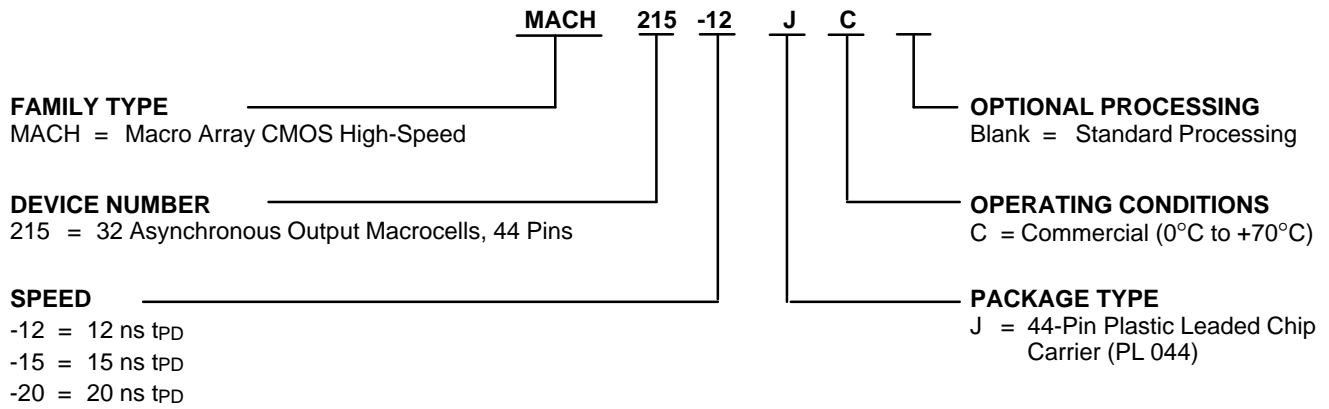
- CLK/I = Clock or Input
- GND = Ground
- I = Input
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage

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## ORDERING INFORMATION

### Commercial Products

Programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH215-12	JC
MACH215-15	
MACH215-20	

#### Valid Combinations

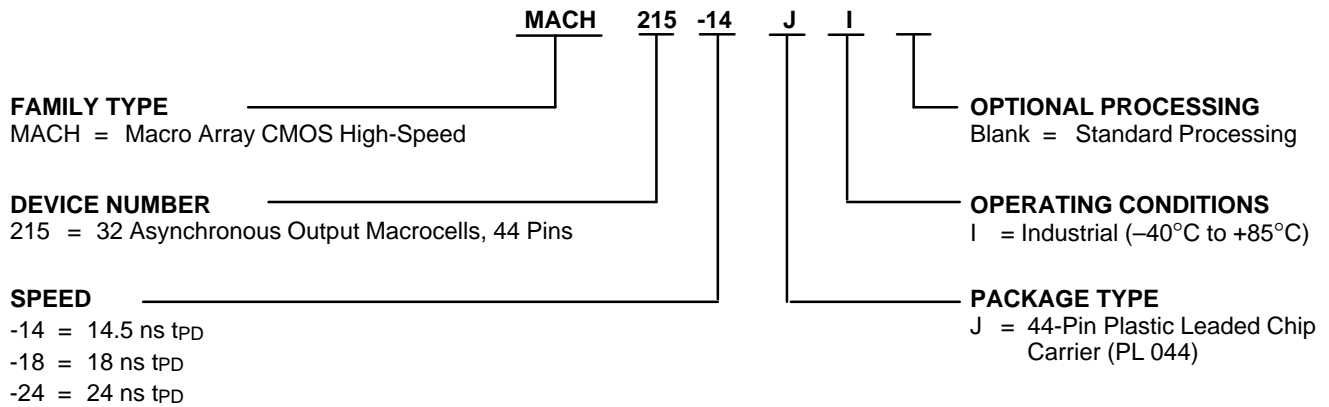
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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## ORDERING INFORMATION

### Industrial Products

Programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH215-14	JI
MACH215-18	
MACH215-24	

#### Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## FUNCTIONAL DESCRIPTION

The MACH215 consists of four asynchronous PAL blocks connected by a switch matrix. There are 32 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are also two additional global clock pins that can be used as dedicated inputs. This device provides two kinds of macrocell: output macrocells and input macrocells. This adds greater logic density without affecting the number of pins.

### The PAL Blocks

Each PAL block in the MACH215 (Figure 1) contains a 64-product-term array, a logic allocator, 8 output macrocells, 8 input macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22RA8" with 8 input macrocells. All flip-flops within the device can operate independently.

### The Switch Matrix

The MACH215 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

### The Product-term Array

The MACH215 product-term array consists of 32 product terms for logic use and 32 product terms for generating macrocell control signals.

### The Logic Allocator

The logic allocator in the MACH215 (Figure 2) takes the 32 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

**Table 1. Logic Allocation**

Output Macrocell	Available Clusters
M <sub>0</sub>	C <sub>0</sub> , C <sub>1</sub>
M <sub>1</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>
M <sub>2</sub>	C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub>
M <sub>3</sub>	C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub>
M <sub>4</sub>	C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub>
M <sub>5</sub>	C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub>
M <sub>6</sub>	C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>
M <sub>7</sub>	C <sub>6</sub> , C <sub>7</sub>

### The Macrocell

There are two types of macrocell in the MACH215: output macrocells and input macrocells. The output macrocell takes the logic of the device and provides it to I/O pins and/or provides feedback for additional logic generation. The input macrocell allows I/O pins to be configured as registered or latched inputs.

The output macrocell (Figure 3) can generate registered or combinatorial outputs. In addition, a transparent-low latched configuration is provided. If used, the register can be configured as a T-type or a D-type flip-flop. Register and latch functionality is defined in Table 2. Programmable polarity and the T-type flip-flop both give the software a way to minimize the number of product terms needed. These choices can be made automatically by the software when it fits the design into the device.

**Table 2. Register/Latch Operation**

Configuration	D/T	CLK/LE*	Q+
D-Register	X 0 1	0, 1, ↓ (↑) ↑ (↓) ↑ (↓)	Q 0 1
T-Register	X 0 1	0, 1, ↓ (↑) ↑ (↓) ↑ (↓)	Q Q Q
Latch	X 0 1	1 (0) 0 (1) 0 (1)	Q 0 1

\*Polarity of CLK/LE can be programmed.

The output macrocell sends its output back to the switch matrix, via internal feedback, and to the I/O cell. The feedback is always available regardless of the configuration of the I/O cell. This allows for buried combinatorial or registered functions, freeing up the I/O pins for use as inputs if not needed as outputs. The basic output macrocell configurations are shown in Figure 4.

The clock/latch-enable for each individual output macrocell can be driven by one of four signals. Two of the signals are provided by the global clock pin CLK<sub>0</sub>/LE<sub>0</sub>; either polarity may be chosen. The other two signals come from a product term provided for each output macrocell. Either polarity of the logic generated by the product term can be chosen. The global clock pin is also available as an input, although care must be taken when a signal acts as both clock and input to the same device.

Each individual output macrocell also has a product term for asynchronous reset and a product term for asynchronous preset. This means that any register or latch may be reset or preset without affecting any other register or latch in the device. The functionality of the flip-flops with respect to initialization is illustrated in Table 3.

**Table 3. Asynchronous Reset/Preset Operation**

AR	AP	CLK/LE	Q+
0	0	X	See Table 12
0	1	X	1
1	0	X	0
1	1	X	0

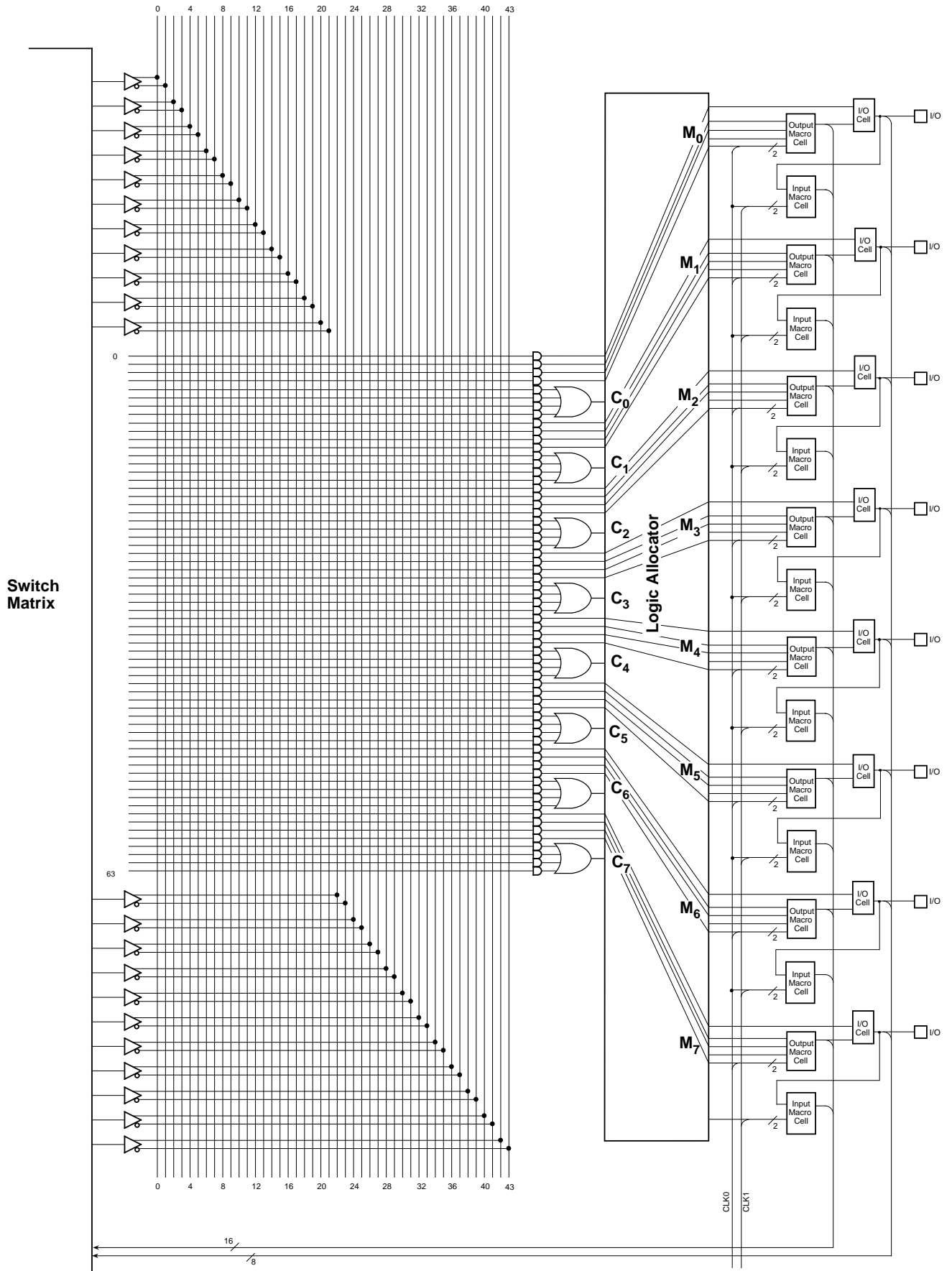
The input macrocell (Figure 5) consists of a flip-flop that can be used to provide registered or latched inputs. The flip-flop can be clocked by either polarity of one of the two global clock/latch-enable pins.

Reset or preset are not provided for these flip-flops. If combinatorial inputs are desired, this macrocell is not used, and the feedback from the I/O pin is used directly. Both the I/O pin feedback and the output of the input register or latch are always available to the switch matrix.

Possible input macrocell configurations are shown in Figure 6.

### The I/O Cell

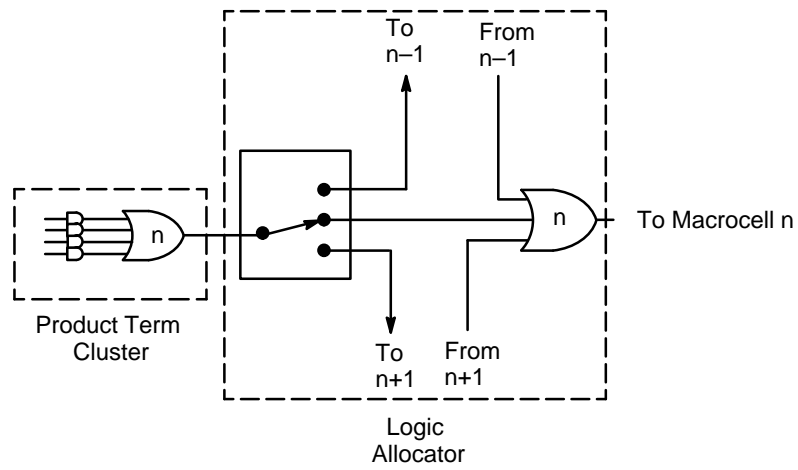
The I/O cell (Figure 7) provides a three-state output buffer. The three-state control is provided by an individual product term for each I/O cell. Depending on the logic programmed onto this product term, the I/O pin can be configured as an output, an input, or a bidirectional pin. The feedback from the I/O pin is always available to the switch matrix, regardless of the state of the output buffer or the output macrocell.



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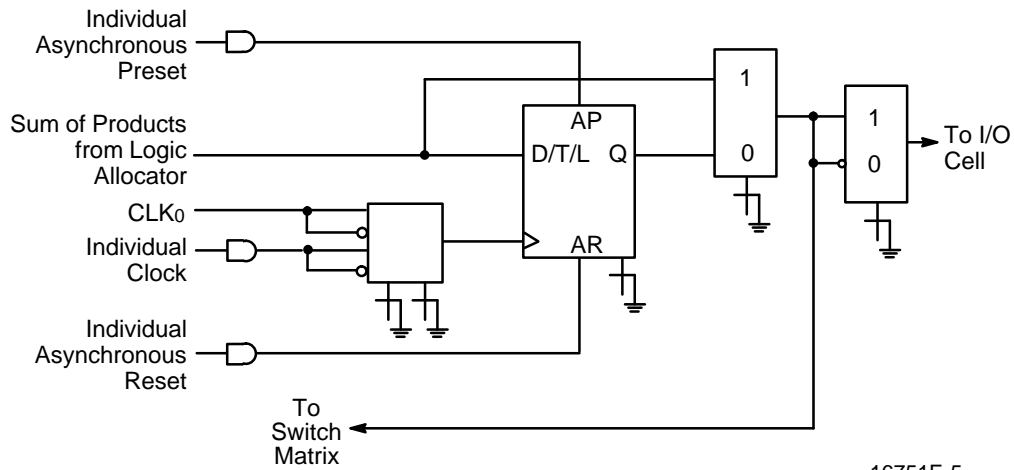
Figure 1. MACH215 PAL Block





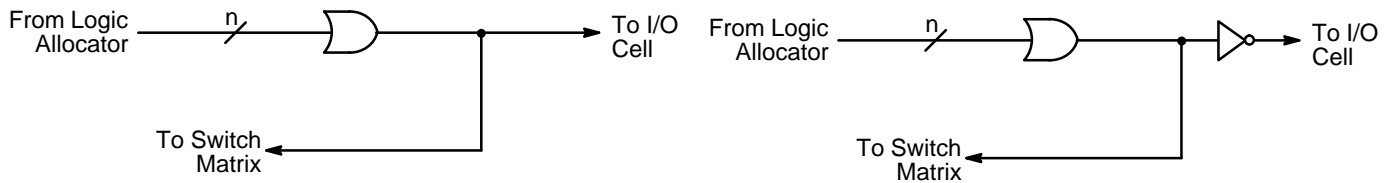
16751E-4

**Figure 2. Product Term Clusters and the Logic Allocator**



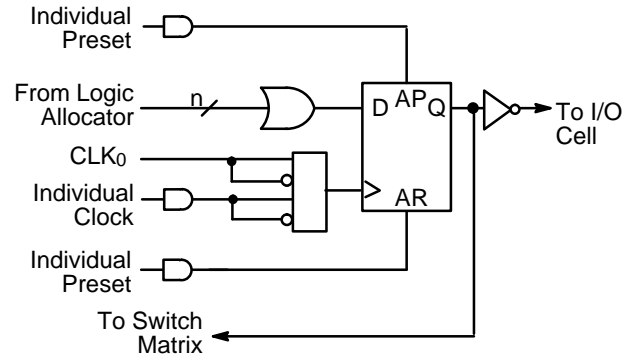
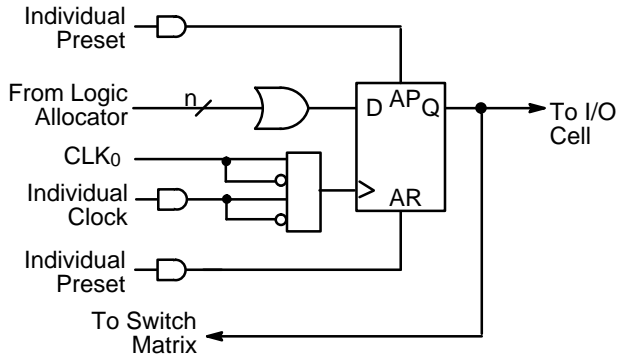
16751E-5

**Figure 3. Output Macrocell**



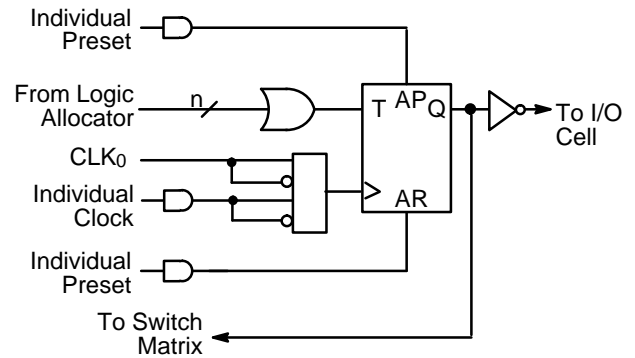
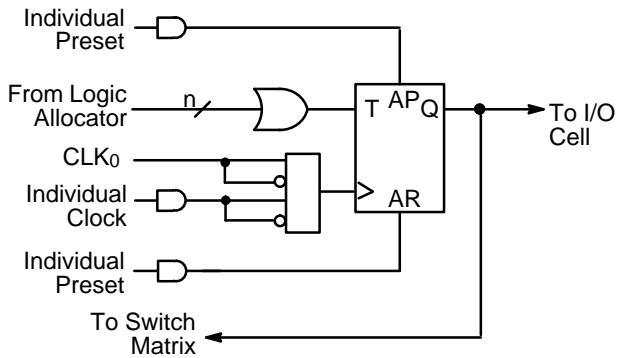
**a. Combinatorial, Active High**

**b. Combinatorial, Active Low**



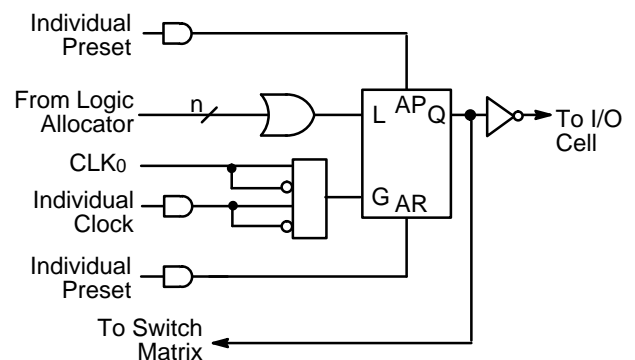
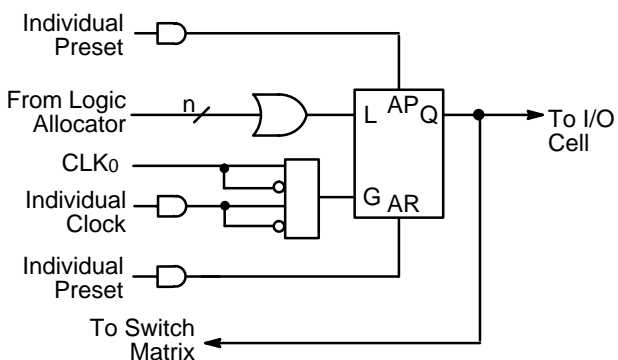
**c. D-type Register, Active High**

**d. D-type Register, Active Low**



**e. T-type Register, Active High**

**f. T-type Register, Active Low**

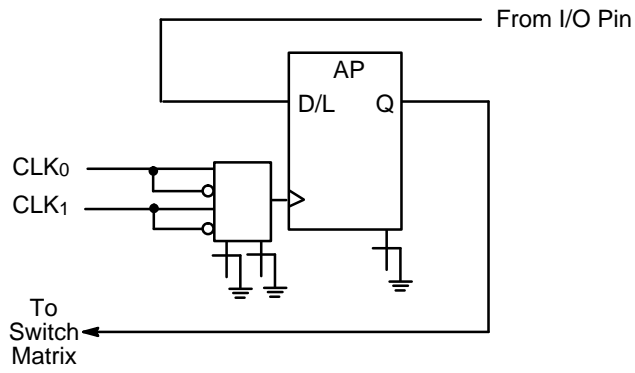


**g. Latch, Active High**

**h. Latch, Active Low**

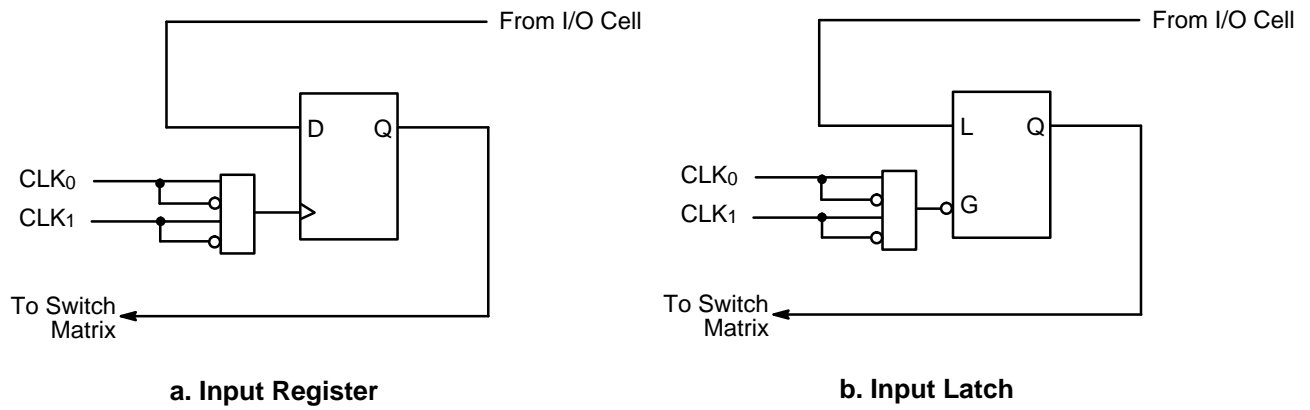
16751E-6

**Figure 4. Output Macrocell Configurations**



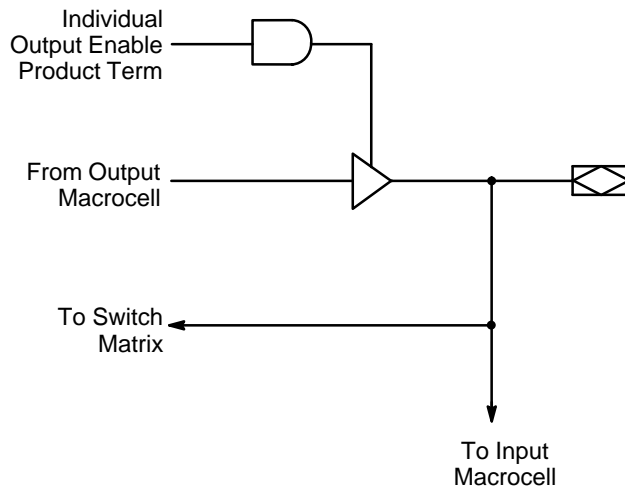
16751E-7

**Figure 5. Input Macrocell**



16751E-8

**Figure 6. Input Macrocell Configurations**



16751E-9

**Figure 7. I/O Cell**

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	−0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ )	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

## OPERATING RANGES

### Commercial (C) Devices

Temperature ( $T_A$ ) Operating in Free Air	0°C to +70°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 1)			0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
$I_{IH}$	Input HIGH Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)			10	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)			−100	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)			10	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)			−100	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)	−30		−160	mA
$I_{CC}$	Supply Current (Typical)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ , $f = 25$ MHz (Note 5)		95		mA

### Notes:

- Total  $I_{OL}$  for one PAL block should not exceed 128 mA.
- These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.  
 $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.
- Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

## CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C, f = 1 MHz	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V		8	pF

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		-12		-15		-20		Unit	
			Min	Max	Min	Max	Min	Max		
t <sub>PD</sub>	Input, I/O, or Feedback to Combinatorial Output (Note 3)		3	12	3	15	3	20	ns	
t <sub>SA</sub>	Setup Time from Input, I/O, or Feedback to Product Term Clock		D-type	5		6		8	ns	
			T-type	6		7		9	ns	
t <sub>HA</sub>	Register Data Hold Time Using Product Term Clock		5		6		8	ns		
t <sub>COA</sub>	Product Term Clock to Output (Note 3)		4	14	4	18	4	22	ns	
t <sub>WLA</sub>	Product Term, Clock Width		LOW	8		9		12	ns	
t <sub>WHA</sub>			HIGH	8		9		12	ns	
f <sub>MAXA</sub>	Maximum Frequency Using Product Term Clock (Note 1)	External Feedback	1/(t <sub>SA</sub> + t <sub>COA</sub> )	D-type	52.6		41.7		33.3	MHz
			T-type	50		40		32.2	MHz	
		Internal Feedback (f <sub>CNTA</sub> )	D-type	58.8		45.5		35.7	MHz	
			T-type	55.6		43.5		34.5	MHz	
No Feedback	1/(t <sub>WLA</sub> + t <sub>WHA</sub> )	62.5		55.6		41.7	MHz			
t <sub>SS</sub>	Setup Time from Input, I/O, or Feedback to Global Clock		D-type	7		10		13	ns	
			T-type	8		11		14	ns	
t <sub>HS</sub>	Register Data Hold Time Using Global Clock		0		0		0	ns		
t <sub>COS</sub>	Global Clock to Output (Note 3)		2	8	2	10	2	12	ns	
t <sub>WLS</sub>	Global Clock Width		LOW	6		6		8	ns	
t <sub>WHS</sub>			HIGH	6		6		8	ns	
f <sub>MAXS</sub>	Maximum Frequency Using Global Clock (Note 1)	External Feedback	1/(t <sub>SS</sub> + t <sub>COS</sub> )	D-type	66.7		50		40	MHz
			T-type	62.5		47.6		38.5	MHz	
		Internal Feedback (f <sub>CNTS</sub> )	D-type	83.3		66.6		50	MHz	
			T-type	76.9		62.5		47.6	MHz	
No Feedback	1/(t <sub>WLS</sub> + t <sub>WHS</sub> )	83.3		83.3		62.5	MHz			
t <sub>SLA</sub>	Setup Time from Input, I/O, or Feedback to Product Term Gate		5		6		8	ns		
t <sub>HLA</sub>	Latch Data Hold Time Using Product Term Clock		5		6		8	ns		
t <sub>GOA</sub>	Product Term Gate to Output (Note 3)			16		19		22	ns	
t <sub>GWA</sub>	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		8		9		12	ns		
t <sub>SLS</sub>	Setup Time from Input, I/O, or Feedback to Global Gate		7		10		13	ns		
t <sub>HLS</sub>	Latch Data Hold Time Using Global Gate		0		0		0	ns		
t <sub>GOS</sub>	Gate to Output (Note 3)			10		11		12	ns	
t <sub>GWS</sub>	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		6		6		8	ns		

**SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)  
(continued)**

Parameter Symbol	Parameter Description	-12		-15		-20		Unit	
		Min	Max	Min	Max	Min	Max		
t <sub>PDL</sub>	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch		14		17		22	ns	
t <sub>SIR</sub>	Input Register Setup Time	2		2		2		ns	
t <sub>HIR</sub>	Input Register Hold Time	2		2.5		3		ns	
t <sub>ICO</sub>	Input Register Clock to Combinatorial Output		15		18		23	ns	
t <sub>ICS</sub>	Input Register Clock to Output Register Setup	D-type	12		15		20	ns	
		T-type	13		16		21	ns	
t <sub>WICL</sub>	Input Register Clock Width	LOW	6		6		8	ns	
t <sub>WICH</sub>		HIGH	6		6		8	ns	
f <sub>MAXIR</sub>	Maximum Input Register Frequency	1/(t <sub>WICL</sub> + t <sub>WICH</sub> )		83.3		83.3		62.5	MHz
t <sub>SIL</sub>	Input Latch Setup Time	2		2		2		ns	
t <sub>HIL</sub>	Input Latch Hold Time	2		2.5		3		ns	
t <sub>IGO</sub>	Input Latch Gate to Combinatorial Output		17		20		25	ns	
t <sub>IGOL</sub>	Input Latch Gate to Output Through Transparent Output Latch		19		22		27	ns	
t <sub>SLLA</sub>	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate	7		8		10		ns	
t <sub>IGSA</sub>	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate	7		8		10		ns	
t <sub>SLLS</sub>	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate	9		12		15		ns	
t <sub>IGSS</sub>	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate	13		16		21		ns	
t <sub>WIGL</sub>	Input Latch Gate Width LOW	6		6		8		ns	
t <sub>PDLL</sub>	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16		19		24	ns	
t <sub>AR</sub>	Asynchronous Reset to Registered or Latched Output		16		20		25	ns	
t <sub>ARW</sub>	Asynchronous Reset Width (Note 1)	12		15		20		ns	
t <sub>ARR</sub>	Asynchronous Reset Recovery Time (Note 1)	8		10		15		ns	
t <sub>AP</sub>	Asynchronous Preset to Registered or Latched Output		16		20		25	ns	
t <sub>APW</sub>	Asynchronous Preset Width (Note 1)	12		15		20		ns	
t <sub>APR</sub>	Asynchronous Preset Recovery Time (Note 1)	8		10		15		ns	
t <sub>EA</sub>	Input, I/O, or Feedback to Output Enable (Note 3)	2	12	2	15	2	20	ns	
t <sub>ER</sub>	Input, I/O, or Feedback to Output Disable (Note 3)	2	12	2	15	2	20	ns	

**Notes:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
2. See Switching Test Circuit for test conditions. Switching waveforms illustrate true clocks only. Switching waveforms can be used to illustrate both synchronous and asynchronous clock timing. For example, t<sub>SS</sub> is the t<sub>S</sub> parameter for synchronous clocks and t<sub>SA</sub> is the t<sub>S</sub> parameter for asynchronous clocks.
3. Parameters measured with 16 outputs switching.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	−0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

## INDUSTRIAL OPERATING RANGES

Ambient Temperature ( $T_A$ ) Operating in Free Air	−40°C to +85°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 1)			0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)			10	$\mu\text{A}$
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)			−100	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)			10	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)			−100	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)	−30		−160	mA
$I_{CC}$	Supply Current (Typical)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ , $f = 25$ MHz (Note 5)		95		mA

### Notes:

- Total  $I_{OL}$  for one PAL block should not exceed 128 mA.
- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.
- Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

## CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C,	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V	f = 1 MHz	8	pF

## SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-14		-18		-24		Unit	
				Min	Max	Min	Max	Min	Max		
t <sub>PD</sub>	Input, I/O, or Feedback to Combinatorial Output (Note 3)				14.5		18		24	ns	
t <sub>SA</sub>	Setup Time from Input, I/O, or Feedback to Product Term Clock		D-type	6		7.5		10		ns	
			T-type	7.5		8.5		11		ns	
t <sub>HA</sub>	Register Data Hold Time Using Product Term Clock			6		7.5		10		ns	
t <sub>COA</sub>	Product Term Clock to Output (Note 3)				17		22		26.5	ns	
t <sub>WLA</sub>	Product Term, Clock Width			LOW	10		11		15	ns	
t <sub>WHA</sub>				HIGH	10		11		15		ns
f <sub>MAXS</sub>	Maximum Frequency Using Product Term Clock (Note 1)	External Feedback	1/(t <sub>SA</sub> + t <sub>COA</sub> )		D-type	42		33		26.5	MHz
					T-type	40		32		25.5	MHz
	Internal Feedback (f <sub>CNTA</sub> )			D-type	47		36		28.5	MHz	
				T-type	44		34.5		27.5	MHz	
	No Feedback	1/(t <sub>WLA</sub> + t <sub>WHA</sub> )			50		44.5		33		MHz
t <sub>SS</sub>	Setup Time from Input, I/O, or Feedback to Global Clock		D-type	8.5		12		16		ns	
			T-type	10		13.5		17		ns	
t <sub>HS</sub>	Register Data Hold Time Using Global Clock			0		0		0		ns	
t <sub>COS</sub>	Global Clock to Output (Note 3)				10		12		14.5	ns	
t <sub>WLS</sub>	Global Clock Width			LOW	7.5		7.5		10	ns	
t <sub>WHS</sub>				HIGH	7.5		7.5		10		ns
f <sub>MAXS</sub>	Maximum Frequency Using Global Clock (Note 1)	External Feedback	1/(t <sub>SS</sub> + t <sub>COS</sub> )		D-type	53		40		32	MHz
					T-type	50		38		30.5	MHz
	Internal Feedback (f <sub>CNTS</sub> )			D-type	66.5		53		40		MHz
				T-type	61.5		50		38		MHz
	No Feedback	1/(t <sub>WLS</sub> + t <sub>WHS</sub> )			66.5		66.5		50		MHz
t <sub>SLA</sub>	Setup Time from Input, I/O, or Feedback to Product Term Gate			6		7.5		10		ns	
t <sub>HLA</sub>	Latch Data Hold Time Using Product Term Clock			6		7.5		10		ns	
t <sub>GOA</sub>	Product Term Gate to Output (Note 3)				19.5		23		26.5	ns	
t <sub>GWA</sub>	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			10		11		14.5		ns	
t <sub>SLS</sub>	Setup Time from Input, I/O, or Feedback to Global Gate			8.5		12		16		ns	
t <sub>HLS</sub>	Latch Data Hold Time Using Global Gate			0		0		0		ns	
t <sub>GOS</sub>	Gate to Output (Note 3)				12		13.5		14.5	ns	
t <sub>GWS</sub>	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			7.5		7.5		10		ns	



**SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)  
(continued)**

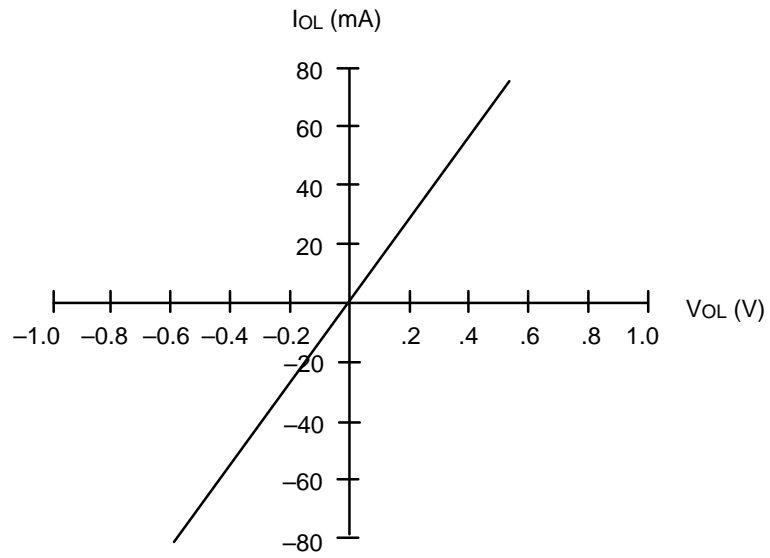
Parameter Symbol	Parameter Description	-14		-18		-24		Unit
		Min	Max	Min	Max	Min	Max	
t <sub>PDL</sub>	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch		17		20.5		26.5	ns
t <sub>SIR</sub>	Input Register Setup Time	2.4		2.4		2.4		ns
t <sub>HIR</sub>	Input Register Hold Time	3		3.5		4		ns
t <sub>ICO</sub>	Input Register Clock to Combinatorial Output		18		22		28	ns
t <sub>ICS</sub>	Input Register Clock to Output Register Setup	D-type	14.5		18		24	ns
		T-type	16		19.5		25.5	ns
t <sub>WICL</sub>	Input Register Clock Width	LOW	7.5		7.5		10	ns
t <sub>WICH</sub>		HIGH	7.5		7.5		10	ns
f <sub>MAXIR</sub>	Maximum Input Register Frequency	1/(t <sub>WICL</sub> + t <sub>WICH</sub> )		66.5		66.5		MHz
t <sub>SIL</sub>	Input Latch Setup Time	2.5		2.5		2.5		ns
t <sub>HIL</sub>	Input Latch Hold Time	3		3.5		4		ns
t <sub>IGO</sub>	Input Latch Gate to Combinatorial Output		20.5		24		30	ns
t <sub>IGOL</sub>	Input Latch Gate to Output Through Transparent Output Latch		23		26.5		32.5	ns
t <sub>SLLA</sub>	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate	8.5		10		12		ns
t <sub>IGSA</sub>	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate	8.5		10		12		ns
t <sub>SLLS</sub>	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate	11		14.5		18		ns
t <sub>IGSS</sub>	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate	16		19.5		25.5		ns
t <sub>WIGL</sub>	Input Latch Gate Width LOW	7.5		7.5		10		ns
t <sub>PDLL</sub>	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		19.5		23		29	ns
t <sub>AR</sub>	Asynchronous Reset to Registered or Latched Output		19.5		24		30	ns
t <sub>ARW</sub>	Asynchronous Reset Width (Note 1)	14.5		18		24		ns
t <sub>ARR</sub>	Asynchronous Reset Recovery Time (Note 1)	10		12		18		ns
t <sub>AP</sub>	Asynchronous Preset to Registered or Latched Output		19.5		24		30	ns
t <sub>APW</sub>	Asynchronous Preset Width (Note 1)	14.5		18		24		ns
t <sub>APR</sub>	Asynchronous Preset Recovery Time (Note 1)	10		12		18		ns
t <sub>EA</sub>	Input, I/O, or Feedback to Output Enable (Note 3)		14.5		18		24	ns
t <sub>ER</sub>	Input, I/O, or Feedback to Output Disable (Note 3)		14.5		18		24	ns

**Notes:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
2. See Switching Test Circuit for test conditions. Switching waveforms illustrate true clocks only. Switching waveforms can be used to illustrate both synchronous and asynchronous clock timing. For example, t<sub>SS</sub> is the t<sub>S</sub> parameter for synchronous clocks and t<sub>SA</sub> is the t<sub>S</sub> parameter for asynchronous clocks.
3. Parameters measured with 16 outputs switching.

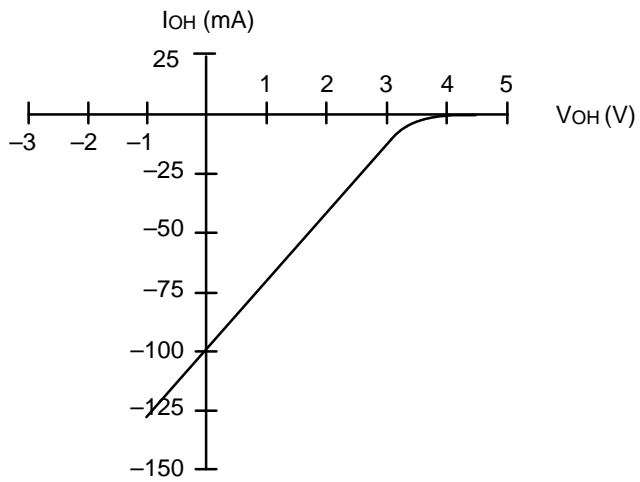
# TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

$V_{CC} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$



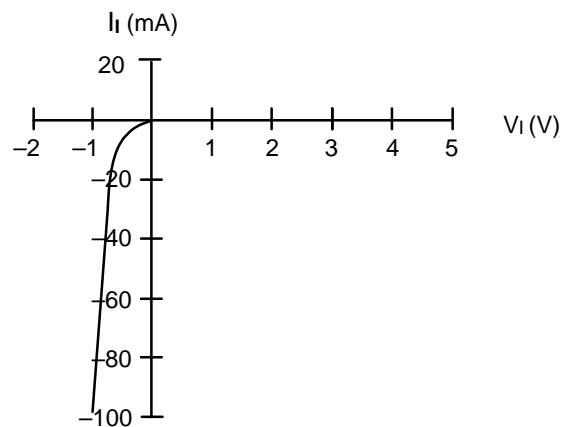
**Output, LOW**

16751E-10



**Output, HIGH**

16751E-11



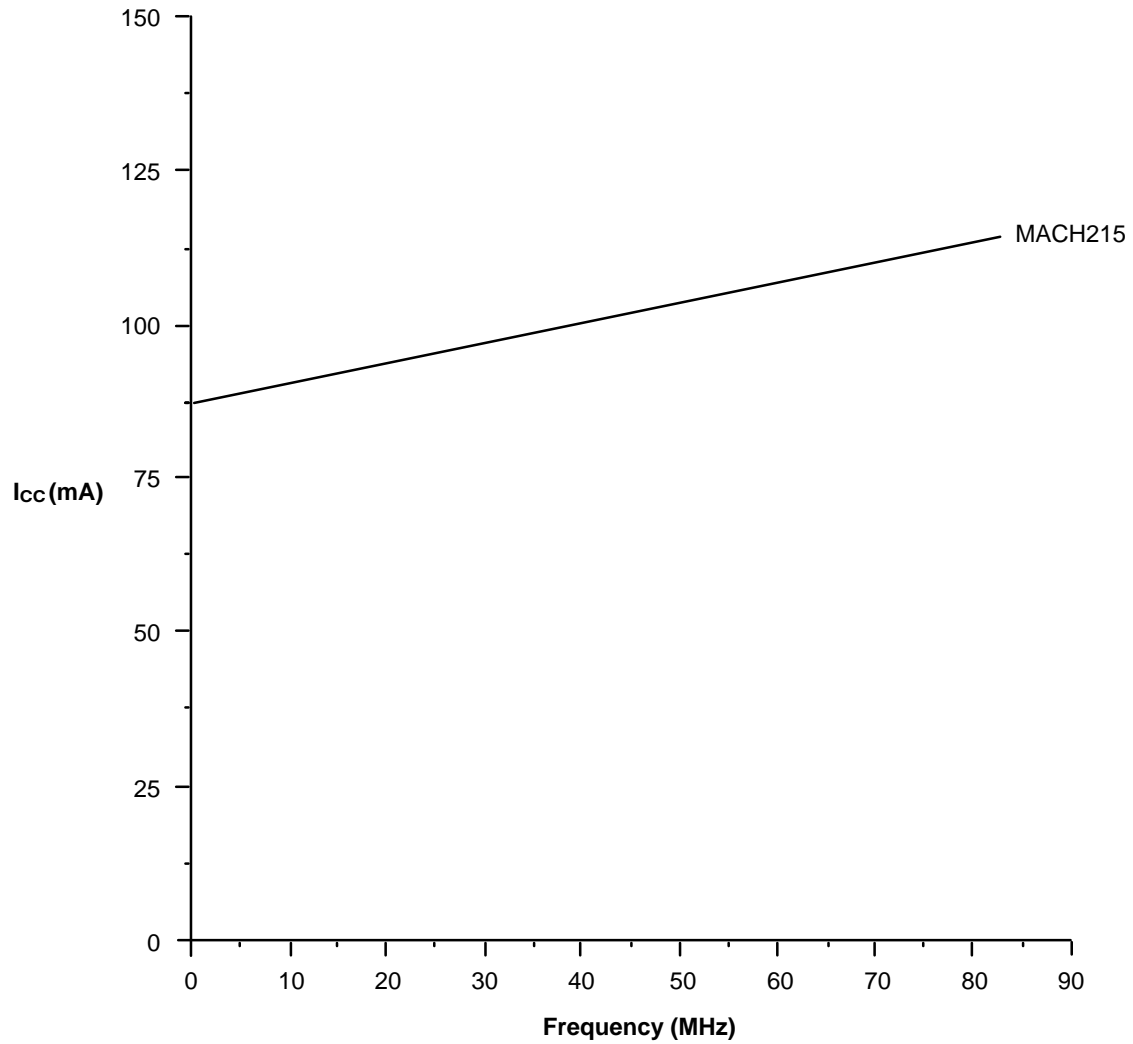
**Input**

16751E-12

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## TYPICAL $I_{CC}$ CHARACTERISTICS

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$



16751E-13

*The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

*Maximum frequency shown uses internal feedback and a D-type register.*

## TYPICAL THERMAL CHARACTERISTICS

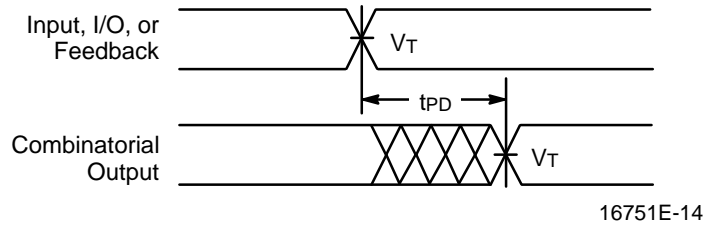
Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description	Typ	Units	
		PLCC		
$\theta_{jc}$	Thermal impedance, junction to case	15	°C/W	
$\theta_{ja}$	Thermal impedance, junction to ambient	40	°C/W	
$\theta_{jma}$	Thermal impedance, junction to ambient with air flow	200 lfp air	36	°C/W
		400 lfp air	33	°C/W
		600 lfp air	31	°C/W
		800 lfp air	29	°C/W

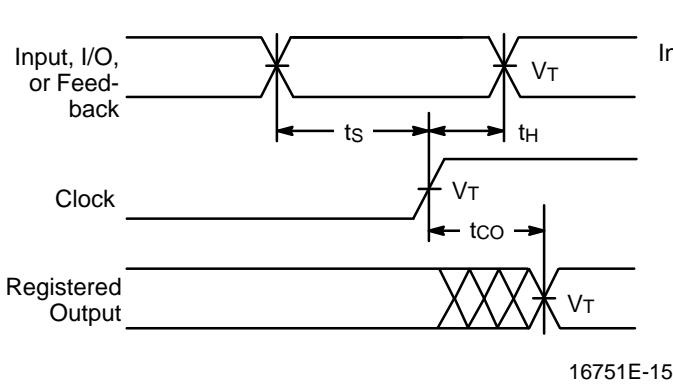
### **Plastic $\theta_{jc}$ Considerations**

*The data listed for plastic  $\theta_{jc}$  are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the  $\theta_{jc}$  measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore,  $\theta_{jc}$  tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.*

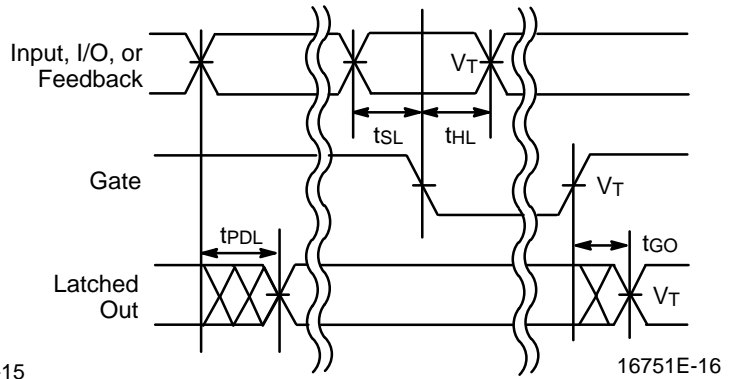
# SWITCHING WAVEFORMS



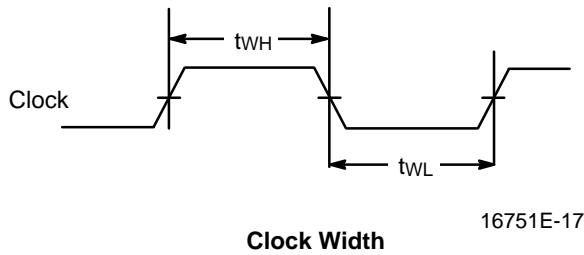
**Combinatorial Output**



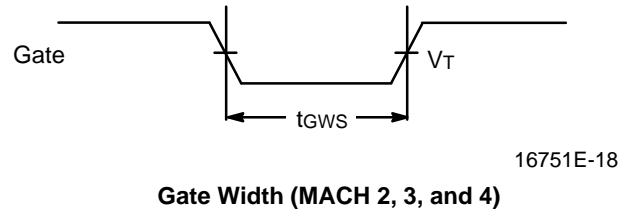
**Registered Output**



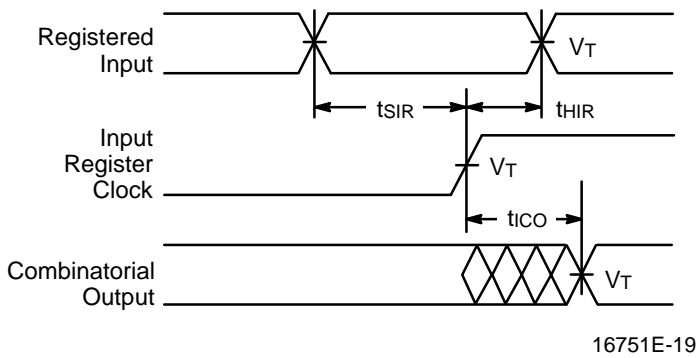
**Latched Output (MACH 2, 3, and 4)**



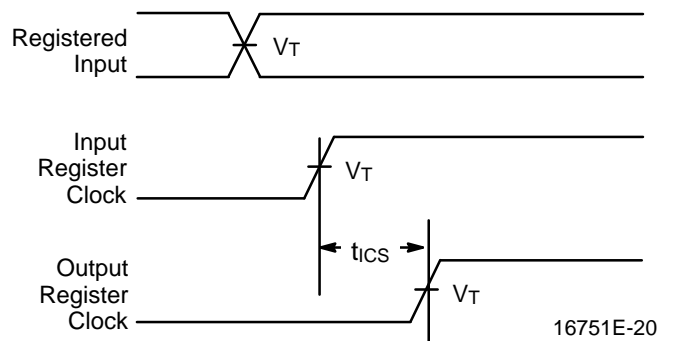
**Clock Width**



**Gate Width (MACH 2, 3, and 4)**



**Registered Input (MACH 2 and 4)**

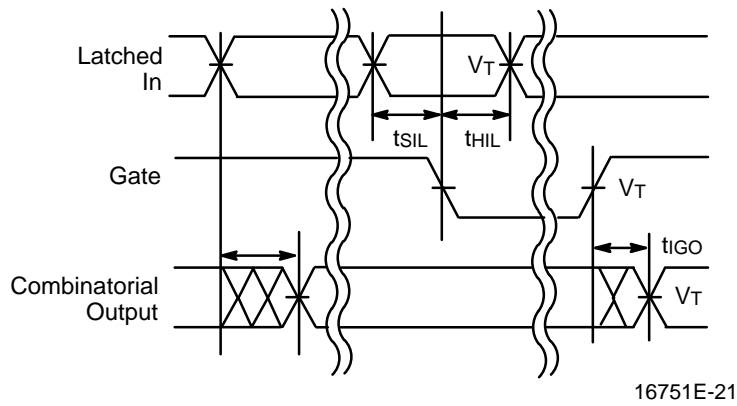


**Input Register to Output Register Setup (MACH 2 and 4)**

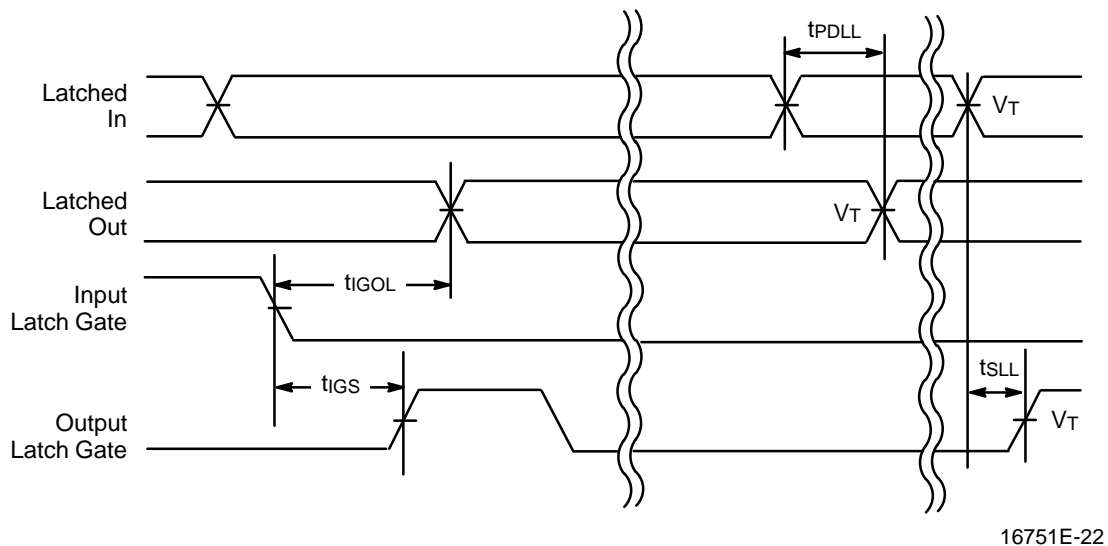
**Notes:**

1.  $V_T = 1.5 V$ .
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2 ns–4 ns typical.

## SWITCHING WAVEFORMS



Latched Input (MACH 2 and 4)

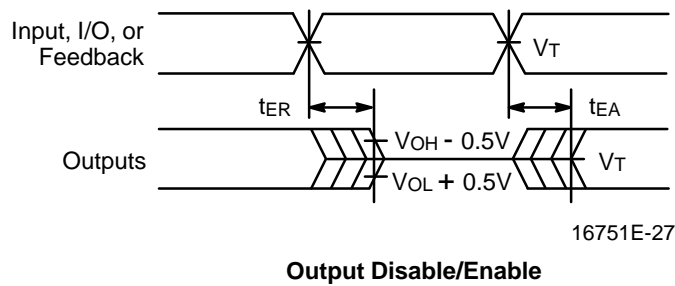
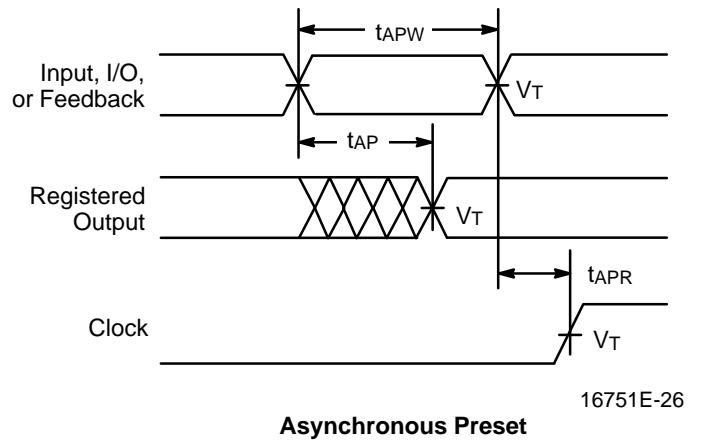
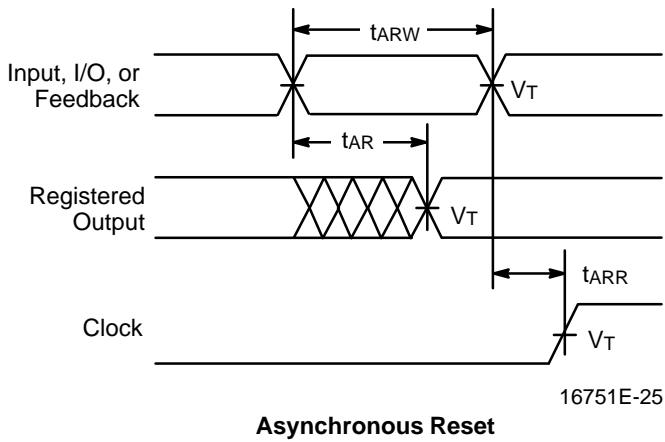
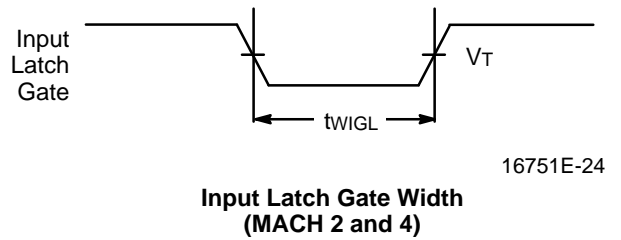
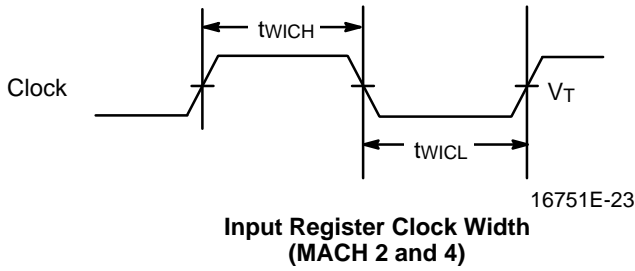


Latched Input and Output  
(MACH 2, 3, and 4)

**Notes:**

1.  $V_T = 1.5$  V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2 ns–4 ns typical.




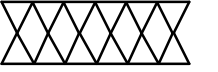
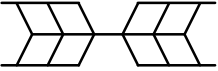
# SWITCHING WAVEFORMS



**Notes:**

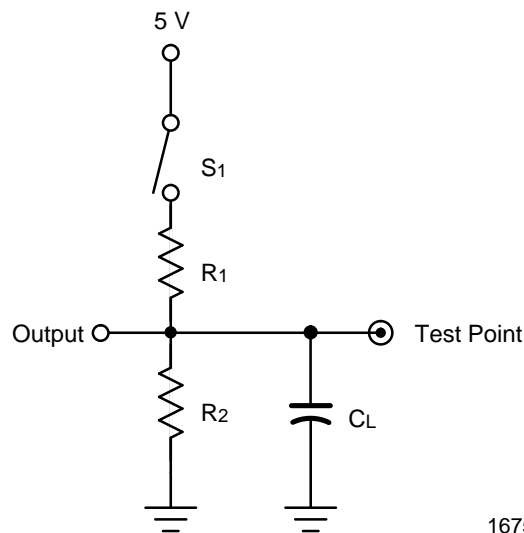
1.  $V_T = 1.5 V$ .
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2 ns–4 ns typical.

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

## SWITCHING TEST CIRCUIT



16751E-28

Specification	S <sub>1</sub>	C <sub>L</sub>	Commercial		Measured Output Value
			R <sub>1</sub>	R <sub>2</sub>	
t <sub>PD</sub> , t <sub>CO</sub>	Closed	35 pF	300 Ω	390 Ω	1.5 V
t <sub>EA</sub>	Z → H: Open Z → L: Closed				1.5 V
t <sub>ER</sub>	H → Z: Open L → Z: Closed	5 pF			H → Z: V <sub>OH</sub> - 0.5 V L → Z: V <sub>OL</sub> + 0.5 V

\*Switching several outputs simultaneously should be avoided for accurate measurement.



## f<sub>MAX</sub> PARAMETERS

The parameter  $f_{MAX}$  is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs,  $f_{MAX}$  is specified for three types of synchronous designs.

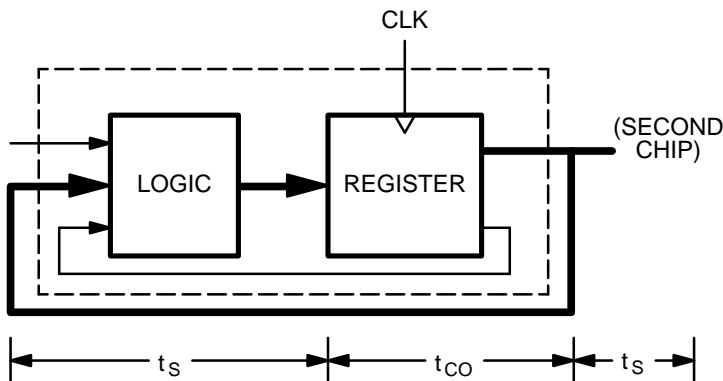
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ( $t_s + t_{CO}$ ). The reciprocal,  $f_{MAX}$ , is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This  $f_{MAX}$  is designated “ $f_{MAX}$  external.”

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This  $f_{MAX}$  is designated “ $f_{MAX}$  internal”. A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called “ $f_{CNT}$ .”

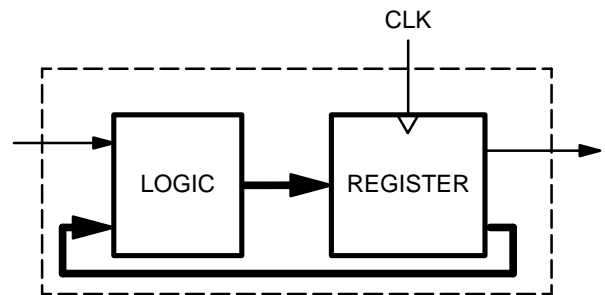
The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ( $t_s + t_H$ ). However, a lower limit for the period of each  $f_{MAX}$  type is the minimum clock period ( $t_{WH} + t_{WL}$ ). Usually, this minimum clock period determines the period for the third  $f_{MAX}$ , designated “ $f_{MAX}$  no feedback.”

For devices with input registers, one additional  $f_{MAX}$  parameter is specified:  $f_{MAXIR}$ . Because this involves no feedback, it is calculated the same way as  $f_{MAX}$  no feedback. The minimum period will be limited either by the sum of the setup and hold times ( $t_{SIR} + t_{HIR}$ ) or the sum of the clock widths ( $t_{WICL} + t_{WICH}$ ). The clock widths are normally the limiting parameters, so that  $f_{MAXIR}$  is specified as  $1/(t_{WICL} + t_{WICH})$ . Note that if both input and output registers are used in the same path, the overall frequency will be limited by  $t_{CS}$ .

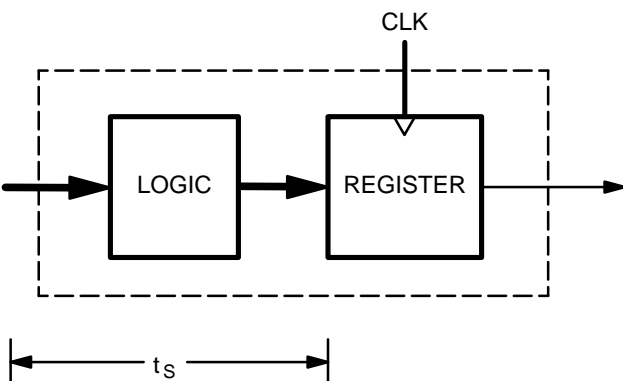
All frequencies except  $f_{MAX}$  internal are calculated from other measured AC parameters.  $f_{MAX}$  internal is measured directly.



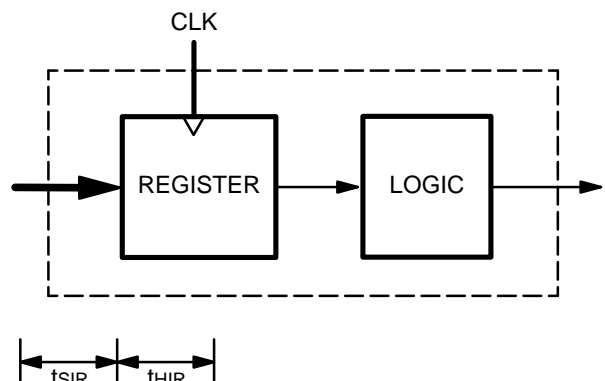
$f_{MAX}$  External;  $1/(t_s + t_{CO})$



$f_{MAX}$  Internal ( $f_{CNT}$ )



$f_{MAX}$  No Feedback;  $1/(t_s + t_H)$  or  $1/(t_{WH} + t_{WL})$



$f_{MAXIR}$  ;  $1/(t_{SIR} + t_{HIR})$  or  $1/(t_{WICL} + t_{WICH})$

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## ENDURANCE CHARACTERISTICS

The MACH families are manufactured using our advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in

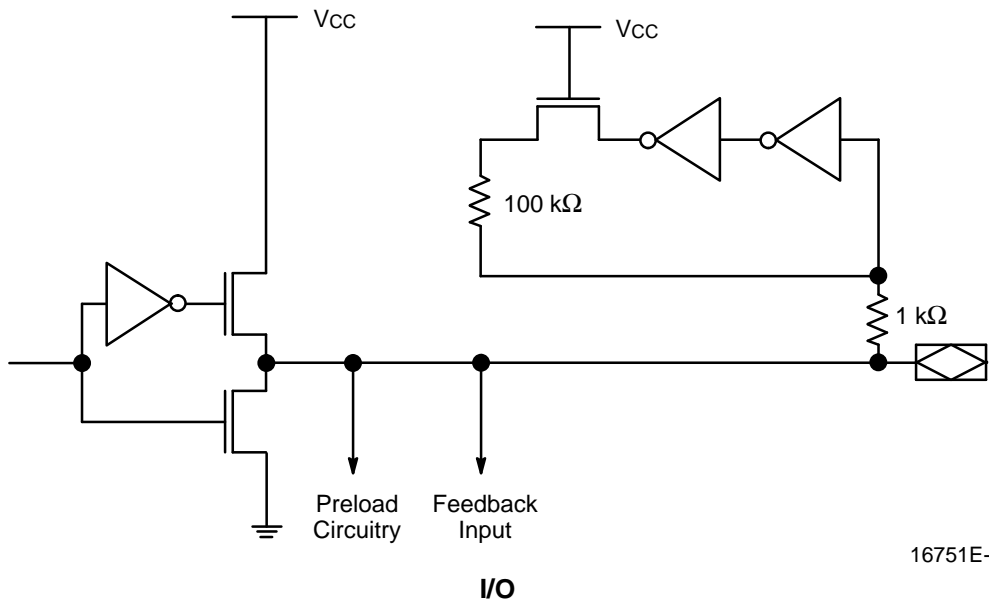
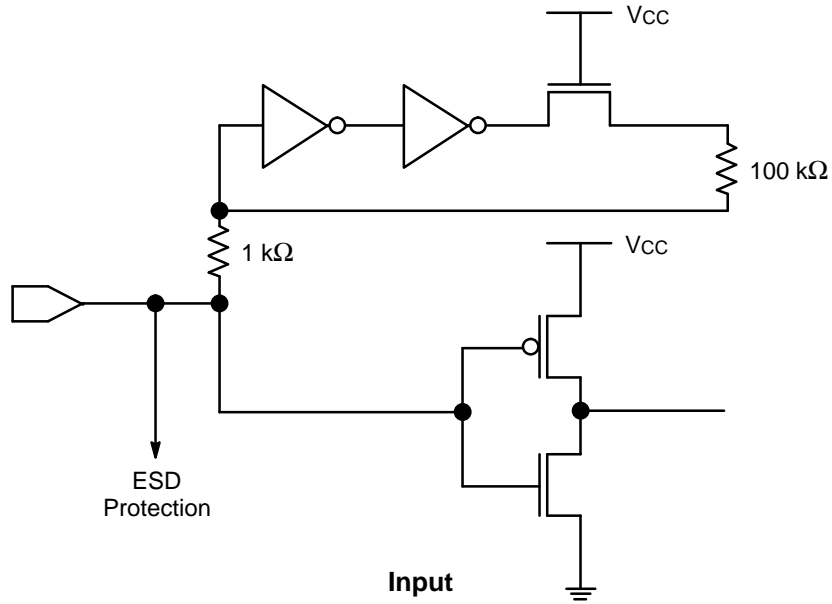
bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

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### Endurance Characteristics

Parameter Symbol	Parameter Description	Min	Units	Test Conditions
t <sub>DR</sub>	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

# INPUT/OUTPUT EQUIVALENT SCHEMATICS



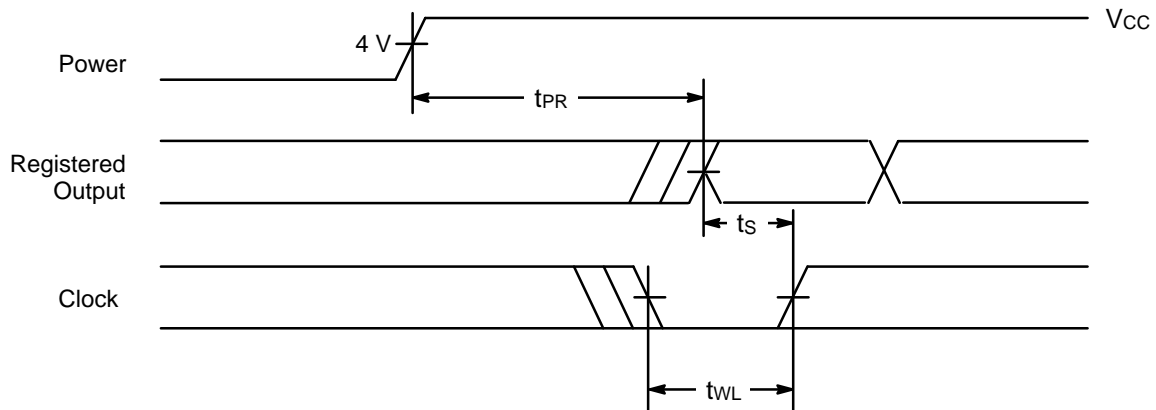
## POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the

wide range of ways  $V_{CC}$  can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The  $V_{CC}$  rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
$t_{PR}$	Power-Up Reset Time	10	$\mu s$
$t_s$	Input or Feedback Setup Time	See Switching Characteristics	
$t_{WL}$	Clock Width LOW	See Switching Characteristics	



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Power-Up Reset Waveform

## USING PRELOAD AND OBSERVABILITY

In order to be testable, a circuit must be both controllable and observable. To achieve this, the MACH devices incorporate register preload and observability.

In preload mode, each flip-flop in the MACH device can be loaded from the I/O pins, in order to perform functional testing of complex state machines. Register preload makes it possible to run a series of tests from a known starting state, or to load illegal states and test for proper recovery. This ability to control the MACH device's internal state can shorten test sequences, since it is easier to reach the state of interest.

The observability function makes it possible to see the internal state of the buried registers during test by overriding each register's output enable and activating the output buffer. The values stored in output and buried registers can then be observed on the I/O pins. Without this feature, a thorough functional test would be impossible for any designs with buried registers.

While the implementation of the testability features is fairly straightforward, care must be taken in certain instances to insure valid testing.

One case involves asynchronous reset and preset. If the MACH registers drive asynchronous reset or preset lines and are preloaded in such a way that reset or preset are asserted, the reset or preset may remove the preloaded data. This is illustrated in Figure 8. Care should be taken when planning functional tests, so that states that will cause unexpected resets and presets are not preloaded.

Another case to be aware of arises in testing combinatorial logic. When an output is configured as combinatorial, the observability feature forces the output into registered mode. When this happens, all product terms are forced to zero, which eliminates all combinatorial data. For a straight combinatorial output, the correct value will be restored after the preload or observe function, and there will be no problem. If the function implements a combinatorial latch, however, it relies on feedback to hold the correct value, as shown in Figure 9. As this value may change during the preload or observe operation, you cannot count on the data being correct after the operation. To insure valid testing in these cases, outputs that are combinatorial latches should not be tested immediately following a preload or observe sequence, but should first be restored to a known state.

All MACH 2 devices support both preload and observability.

Contact individual programming vendors in order to verify programmer support.

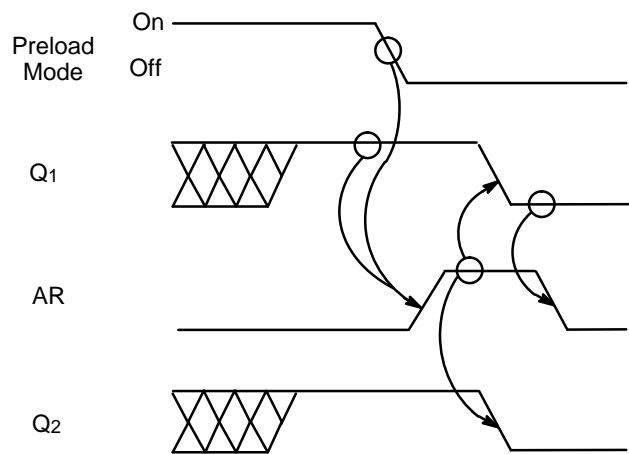
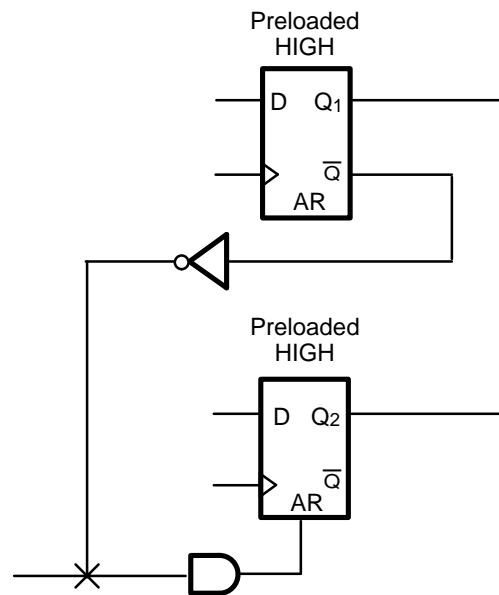


Figure 8. Preload/Reset Conflict

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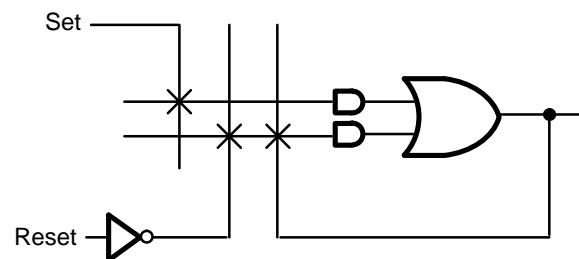


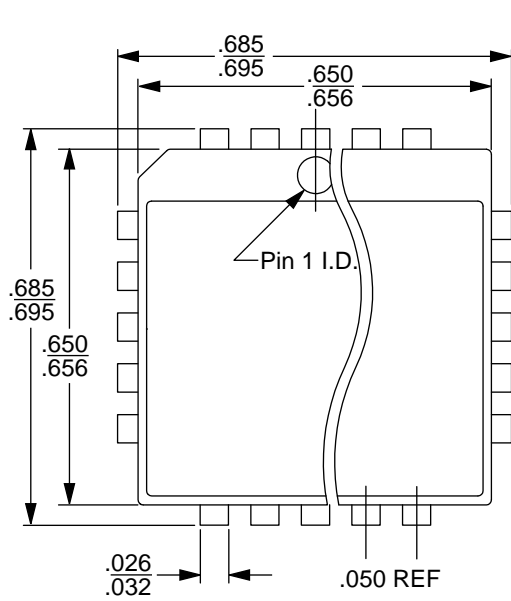
Figure 9. Combinatorial Latch

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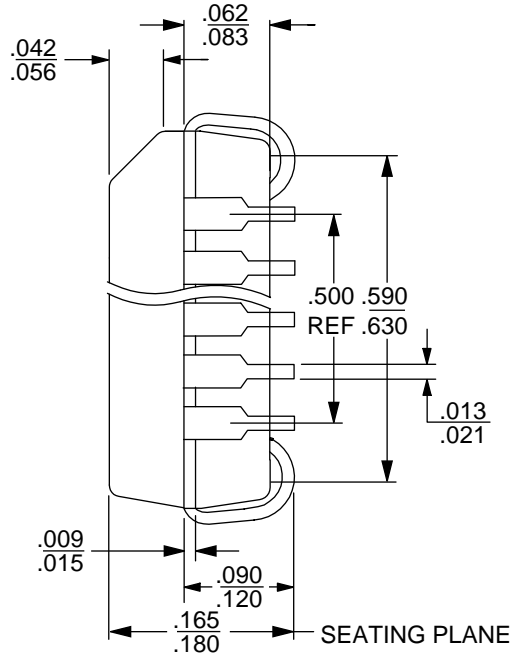
**PHYSICAL DIMENSIONS\***

**PL 044**

**44-Pin Plastic Leaded Chip Carrier (measured in inches)**



TOP VIEW



SIDE VIEW

16-038-SQ  
 PL 044  
 DA78  
 6-28-94 ae

\*For reference only. BSC is an ANSI standard for Basic Space Centering.