ADS78/8505EVM User's Guide

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1 Introduction

The ADS7805 and ADS8505 are complete 16-bit analog-to-digital (A/D) using state-of-the-art CMOS structures. They contain a complete 16-bit, capacitor-based, successive approximation register (SAR) A/D with sample-and-hold, reference, internal conversion clock, and a parallel data interface with 3-state output drivers.

The evaluation module (EVM) is available with either the ADS7805 or ADS8505 installed. The EVM can also accommodate the 12-bit ADS7804 simply removing and replacing the installed device. Samples of the ADS7804 can be obtained through the sample program at Texas Instruments. See the ADS7804 Product Folder for details.

1.1 Features

- Full-Featured Evaluation Board for the ADS7804, ADS7805 or ADS8505, parallel Analog to Digital Converters
- Industry Standard ±10 V Analog Input Range
- Built in reference
- Parallel Interface with 3-state output drivers
- Compatible with the 5-6K Interface Board for use with a variety of DSP Starter Kits as well as the HPA449 from SoftBaugh, Inc. (www.softbaugh.com).
- Field Programmable Gate Array (FPGA) users can evaluate the ADS78/8505EVM by obtaining the Texas Instruments Analog Adapter Kit from Avnet Design Services (www.em.avnet.com).

2 Analog Interface

For maximum flexibility, the ADS78/8505EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient ten-pin dual row header/socket combination at J1. This header/socket provides access to the analog input pins of the ADC. Please consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 1 shows the pin out of the analog input connector, J1.

Table 1. Pinout of the Analog Input Connector, J1

Pin Number	Signal	Description
J1.2 thru J1.16 (even)	Analog Input	To accommodate EVM Stacking using the SN74AHC138 address decoder, J1 feeds jumper W1. Up to four converters can used at the same time.
J1.20	REF(+)J	External reference source input, accessible through W4.
J1.15	REFOUT	Optional connection via W4. Provides external AFE circuitry with REFOUT bias voltage.
J1.1- J1.19 (odd)	AGND	Analog ground connections. Note J1.15 is used for REFOUT connections to external AFE circuitry.

The analog front-end (AFE) circuitry found on the EVM consists of a simple RC filter. When used in combination with the 5-6K Interface Board, the circuits found on both DAP Signal Conditioning Boards (see SLAU105) provide the level shifting and amplifier configurations to realize single ended or bi-polar mode operation of the analog-to-digital converter installed on the EVM.

2.1 Optional Amplifier Input

Jumper W6 provides access to an optional amplifier/buffer circuit on the front end of the data converter. Component U8 can be installed at the user's option with any standard 8 pin SOIC single amplifier component. The amplifier circuit is connected to the ±VA terminals for split supply operation. If single supply amplifiers are used, the –VA (J3 pin 2) can be tied to analog ground (J3 pin 6). The footprint for common 4mm trim pots (see component R7) is provided as an offset adjustment for precision amplifiers such as the OPA228. When used in conjunction with the 5-6K Interface Board, please be aware that the –VA supply is common to all power connectors (JP1 through JP6). Shorting the –VA supply to ground on the ADS78/8505EVM is possible only if it is not used elsewhere on the interface board.

3 Digital Interface

The active low $\overline{CS}$ pin is connected to W8. This pin can be controlled through the SN74AHC138 address decoder at U5. For standalone operation, a 10K resistor to ground on the $\overline{CS}$ pin is provided. Completely removing the shunt at W8 ensures this pin is held low.

The converted data output from the ADC is applied to U3, an SN74ALVCH16245. This 16-bit wide buffer can be configured for 3.3 or 5.0V systems by providing the device with the appropriate IO voltage via W3 (see EVM silkscreen and schematic for details). The SN74ALVCH16245 features 5V tolerant inputs, making it an ideal level shifting buffer for 3V processors. The entire 16 bit data output is presented to J4 pins 1-31 (odd). J4 is a header/socket combination which acts as a pass through connector for easy data monitoring and/or board stacking when multiple devices share the data bus.

The $\overline{BUSY}$ signal is fed through a single gate buffer, an SN74AHC1G125, which is also supplied by the IO voltage selected at W3. The $\overline{BUSY}$ signal can be used as an interrupt source to the host processor, indicating the converted data is ready to be accessed through the parallel data buffer. The remaining digital control lines are discussed in the following section.

3.1 Digital Control via J5, U4 and U6

J5 provides the parallel data bus control signals used on the various interface boards mentioned at the beginning of this document. Two single "OR" gates (U4 and U6 - SN74AHC1G32) are provided to allow several methods of accessing the converted analog signal.

U4 in conjunction with three pin jumper W5 (shunt pins 1-2) allows the user to write a conversion command to the R/C pin of the data converter. When a valid chip select signal is applied to the ADC's $\overline{CS}$ pin, the host processors write strobe ($\overline{WR}$/(R/W)) can be used to initiate a conversion cycle. This function can be bypassed by placing a shunt jumper on J5 pins 3-4. For stand alone operation, the $\overline{CS}$ pin can be held low by removing the shunt at W8 and applying the R/C strobe to J5, pin 17. The shunt on W5 needs to be moved to cover pins 2-3 in this case. The signal on J5 pin 17 connects to one of the timer outputs of the host DSP when this EVM is used with the 5-6K Interface Board. DSK users could set a periodic function in the DSP to initiate the conversion cycle if desired.

U6 in conjunction with U3 (an SN74ALVCH16245) provides a means to isolate the ADC from the external data bus. When a valid chip select is applied to the ADC, the host processors read strobe ($\overline{RD}$) enables the outputs of the data buffer. This function can be bypassed by placing a shunt jumper on J5 pins 5-6.

Table 2. Pinnout of the Digital Control Connector, J5

Pin	Signal / Function
1	DC_CSx - EVM Address Decoder Enable. Can be tied low by placing a shunt on J5 pins 1-2.
3	/WR(R/W) - Host processor active low write strobe
5	/RD - Host processor active low read strobe
7	EVM_A0 - used in conjunction with EVM_A1 and EVM_A2 to determine the ADC address on the data bus.
9	EVM_A1 - used in conjunction with EVM_A0 and EVM_A2 to determine the ADC address on the data bus.
11	EVM_A2 - used in conjunction with EVM_A0 and EVM_A1 to determine the ADC address on the data bus.
13	EVM_A3 - connects to the G1 enable of the address decoder U5. This pin must be high for address decoding operations.
15	EVM_A4 - can be used to control BYTE mode data access
17	TOUT - When W5 is shunted pins 2-3, the signal applied to this pin can be used to initiate a conversion if the ADC has been properly chip selected.
19	/INTB - the buffered BUSY signal output of the ADC. Can provide the host processor with an interrupt source.
2-20 (even)	Digital Ground

3.2 Additional Digital Control and Monitoring

Jumper W2 is provided along with a 10 kΩ resistor (R5) allowing the data converter installed at position U1 to operate in BYTE mode. BYTE access requires two read accesses to the ADC in order to get the full 16-bit data output, once with BYTE high and again with BYTE low. When BYTE is low (default, W2 installed) the data is presented with the LS Byte on pins 22-15 and the MS Byte on pins 13-6. When BYTE is high, the LS Byte and MS Byte swap. An eight bit processor can be configured to take LS or MS data first using either side of the chip, simplifying board layout.

The digital control lines and parallel data bus can be monitored directly from J5 and J4. Each of these connectors provides a complementary digital ground pin and can easily accomodata logic analysers or oscilloscopes. Test points 1 through 4 provide access to analog and digital ground as well as the applied power supply voltages. Test point 5 can be used to monitor the reference voltage.

4 Power Supplies

The ADS78/8505EVM board requires +5V DC for both the analog and digital sections of the ADC. Power to the ADC is sourced from J3 pin 3 and pin 10 (+5VA and +5VD - see table below). The digital I/O voltage can be set for +3.3V or +5.0V depending on the needs of the host processor driving the ADC.

Note:
VDIG must be less than or equal to VANA.

Table 3 shows the pin out of J3:

Table 3. Pinout of the Power Supply Connector, J3

Signal	Pin Number		Signal
+VA	1	2	-VA
+5VA	3	4	Unused
DGND	5	6	AGND
Unused	7	8	Unused
+3.3VD	9	10	+5VD

The EVM is configured with two small LC filters that take the voltage applied to J3 pin 3 and splits it into +5VA and +5VD nodes. For stand alone operation, power sources can be applied via various test points located on the EVM (VANA to TP2 and VDIG to TP4) provided that inductor L2 is removed. Refer to the schematic at the end of this document for details.

The optional amplifier located at position U8 (user supplied) can be powered through J3 pins 1 and 2. See the earlier discussion about the power supply restrictions in section 1.2 of this manual.

Note:
While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.

4.1 Reference Voltage control via W4

The ADS78/8505 is normally configured to use its internal reference. Jumper W4 provides various options to allow the EVM user to send the reference voltage off board to external amplifier circuits (W4 pins 7-8, default state). An external reference source applied to J1 pin 20 can be sent to the ADC by moving the shunt at W4 to pins 1-2. An on board trim pot is provided at R8, and can be used with a shunt jumper placed on W6 pins 3-4. Finally, an on-board fixed 2.5V reference from U2 (REF3125) can be applied to the ADC by moving the shunt at W4 to cover pins 5-6.

5 EVM Operation

The maximum analog input swing is +/-10Vpp. Offset trim can be accomplished on board via R3. Single amplifier U8 in an industry standard SOIC 8 package can be installed to do on board signal conditioning if desired. Please refer to Section 12 of Op Amps for Everyone (Doc. No. SLOD006) for information on various circuit applications.

Once power is applied to the EVM, the analog input source can be connected directly to J1 (top or bottom side) or through optional amplifier and signal conditioning modules using the 5-6K Interface Board or HPA449. Jumper W1 allows the EVM user to choose which analog signal applied to J1 is directed to the input of the ADC, providing the ability to stack up to four ADS78/8505EVM's using the address decoder found at U5.

The digital control signals can be applied directly to J5 (top or bottom side). The ADS78/8505EVM can also be connected directly to the 5-6K Interface Board for use with a variety of C5000 and C6000 series DSP Starter Kits (DSK). The analog and digital input connectors are designed to allow pattern generators and/or logic analyzers to be connected to the EVM using standard ribbon type cables on 0.1" centers.

No specific evaluation software is provided with this EVM, however, code examples are available that show how to use this EVM with a variety of digital signal processors from Texas Instruments Incorporated. Check the product folders or send e-mail to dataconvapps@list.ti.com for a listing of available code examples. The EVM Gerber files are available on request.

Table 4 shows the factory default jumper locations for the ADS78/8505EVM.

Table 4. Factory Default Jumper Locations

Jumper	Function	Default Condition
W1	Controls application of the applied analog signal to VIN	1–2
W2	Controls the state of BYTE	Closed
W3	Controls application of the VIO (3.3 (default) or 5V)	1–2
W4	Controls the application of the reference voltage	7–8
W5	Controls the source of the conversion start signal applied to the ADC's R/C pin	1–2
W6	Controls the application of optional signal conditioning circuitry	1–2
W7	Controls the application of the voltage at the CAP pin or offest trim through R3 to 33.2 kΩ resistor R4.	1–2
W8	Determines which decoded address the ADC will respond to.	1–2

6 EVM Bill of Materials and Schematic

Table 5 contains a complete Bill of Materials for the ADS78/8505EVM. The schematic diagram is also provided for reference.

Table 5. Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C1 C3 C5 C8 C9 C10 C15 C19 C18 C27	0.1uF Ceramic, 0805, X7R, 25V	TDK	C2012X7R1E104K
C2 C12 C20 C21	0.01uF Ceramic, 0805, X7R, 50V	TDK	C2012X7R1H103K
C4 C6 C25	10uF Tantalum, A case, 10V	Panasonic	ECS-T1AY106R
C7 C16	2.2uF Ceramic, 0805, X5R, 10V	TDK	C2012X5R1A225K
C11 C13 C22	10uF Ceramic, 0805, X5R, 10V	Murata	GRM21BR61A106KE19L
C14	0.47uF Ceramic, 0805, X7R, 16V	TDK	C2012X7R1C474K
C17	2.2nF Ceramic, 0805, X7R, 50V	TDK	C2012X7R1H223K
C26 C28	100 pF Ceramic, C0G, 50V	TDK	C2012C0G1H101K
J1 J2 J5 (top side)	10 pin, dual row, SMTheader (20 pos.)	Samtec	TSM-110-01-T-DV-P
J1 J2 J5 (bottom side)	10 pin, dual row, SMT socket (20 pos.)	Samtec	SSW-110-22-F-D-VS-K
J3 (top side)	5 pin, dual row, SMT header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
J3 (bottom side)	5 pin, dual row, SMT socket (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
J4 (top side)	16 Pin, Dual Row, SMT Header (32 Pos.)	Samtec	TSM-116-01-T-DV-P
J4 (bottom side)	16 Pin, Dual Row, SMT socket (32 Pos.)	Samtec	SSW-116-22-F-D-VS-K
L1 L2	15 µH inductor, SMT, 1608 series	Inductors, Inc.	CTDS1608C-153
R1 R5	10 kΩ, 0805, 5%	Yageo America	9C08052A1002JLHFT
R2	33 Ω, 0805, 5%	Yageo America	9C08052A33R0JLHFT
R3 R6	50 kΩ, SMT Trim Pot, 4 mm	Bourns	3214W-1-503E
R4	33.2 kΩ, 0805, 1%	Yageo America	9C08052A3322FKHFT
R8	576 kΩ, 0805, 1%	Yageo America	9C08052A5763FKHFT
R9	0 Ω, 0805, 5%	Yageo America	9C08052A0R00JLHFT
R10, R11	200 Ω, 0805, 1%	Yageo America	9C08052A1002JLHFT
TP2 TP4 TP5	Red test point loop	Keystone	5000
TP1 TP3	Black test point loop	Keystone	5001
U1	ADS7805 or ADS8505	TI	ADS7805U or ADS8505U
U2	REF3125	TI	REF3125AIDBZT
U3	SN74ALVCH15245	TI	SN74ALVCH15245DL
U4 U6	SN74AHC1G32	TI	SN74AHC1G32DBVT
U5	SN74AHC138	TI	SN74AHC138D
U7	OPA353	TI	OPA353NA
U8	Not Installed	TI	Single Op Amp - SOIC
W1	8 pin , dual row, 2 mm header (16 pos)	Samtec	TMM-108-02-L-D
W2	2 pin , 0.1" header	Samtec	TSW-102-07-L-S
W3 W5 W6 W7	3 pin , 0.1" header	Samtec	TSW-103-07-L-S
W4	4 Pin, dual row header (8 pos)	Samtec	TSW-104-07-L-D
W8	3 pin, dual row, TH header (6 pos.)	Samtec	TSW-103-07-L-D

Revision History		
REV	ECN Number	Approved
A	Initial Release	TH

J1 EVM_IN_0 EVM_IN_1 EVM_IN_2 EVM_IN_3 EVM_IN_4 EVM_IN_5 EVM_IN_6 EVM_IN_7

W1 EVM_IN_0 EVM_IN_1 EVM_IN_2 EVM_IN_3 EVM_IN_4 EVM_IN_5 EVM_IN_6 EVM_IN_7

R7 *

+VA C21 10nF

U8 *

-VA C20 10nF

R11 200 ohm

C28 100pF

W6

ADC_ANALOG_IN R10 200 ohm

R4 33.2K

C17 2.2nF

5Va C11 10uF R3 50K W7 C7 2.2uF

U1 ADS8505

Vin CAP REF Vana AGND1 AGND2 DGND Vdig R/C /CS BYTE /BUSY

D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15

24 ADC_R/C 25 /CS 23 EVM_A4 26 /INT

W4 EXT_REFIN ADJ_REFIN EVM_REFIN REFOUT

TP5

C16 2.2uF

R8 10K

C13 10uF R6 50K

C1 0.1uF C2 0.01uF

C12 0.01uF C3 0.1uF

U2 REF3125 VIN OUT GND

C14 0.47uF C22 10uF

C18 0.1uF

U7 OPA353N

R2 33

+5VA +VA C23 C24 -VA 5Va L1 +5VA L2 5Vd TP4

C6 R9 0 Ohm C4 C19 0.1uF C15 0.1uF

TP2 TP3 J3 DGND AGND TP1

VIO +3.3VD W3 +5.0VD C25

VIO C8 0.1uF C10 0.1uF C9 0.1uF C5 0.1uF

C27 0.1uF U9 SN74AHC1G125 /INT /INTB

5VD U6 SN74AHC1G32 /RD_ADC /CS /RD

U3 SN74ALVCH16245 /RD_ADC /OE1 /OE2 DIR1 DIR2 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 1B1 1B2 1B3 1B4 1B5 1B6 1B7 1B8 2B1 2B2 2B3 2B4 2B5 2B6 2B7 2B8 1A1 1A2 1A3 1A4 1A5 1A6 1A7 1A8 2A1 2A2 2A3 2A4 2A5 2A6 2A7 2A8 DGND

J4

ADC_R/C

5VD U4 SN74AHC1G32 /CS /WR(R/W) C26 100pF W5 TOUT

U5 SN74AHC138 Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 VCC GND A B C G1 G2A G2B EVM_A0 EVM_A1 EVM_A2 EVM_A3 DC_CSx

W8 /CS A B C R1 10K

5Vd R5 10K EVM_A4 W2

J5 DC_CSx /WR(R/W) /RD EVM_A0 EVM_A1 EVM_A2 EVM_A3 EVM_A4 TOUT /INTB

TEXAS INSTRUMENTS

12500 TI Blvd. Dallas, Texas 75243

Title: ADS7805/8505 Evaluation Module Schematic

Drawn By: Tom Hendrick			
Engineer: Tom Hendrick	SIZE: B	DATE: 22-Nov-2004	REV: A
FILE: EDGE #6465116			SHEET: 1 OF: 1

7 Related Documentation from Texas Instruments

Table 6. EVM Compatible Device Data Sheets, Users Guides and Additional Resources

Data Sheet	**Literature Number**
ADS7804	SBAS019
ADS7805	SBAS020
ADS8505	SLAS180
Users Guides	**Literatuare Number**
5-6K Interface Board	SLAU104
DAP Signal Conditioning Boards	SLAU105
Additional Resources	**Literature Number**
Op Amps for Everyone	SLOD006
Controlling the ADS7805 With TMS320 Series DSPs	SLAA229

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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