**Please note that Cypress is an Infineon Technologies Company.**

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

# CY14U256LA

# 256-Kbit (32 K × 8) nvSRAM

## Features

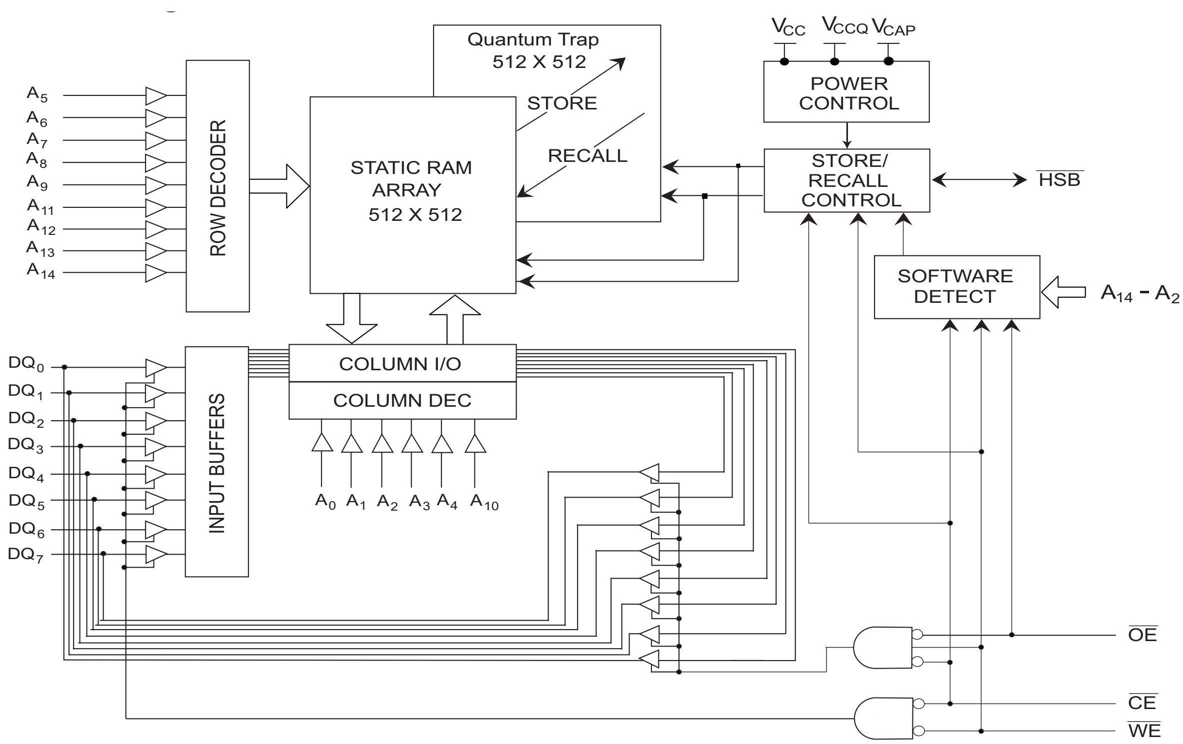
- 35 ns access time
- Internally organized as 32 K × 8
- Hands off automatic STORE on power down with only a small capacitor
- STORE to QuantumTrap nonvolatile elements initiated by software, device pin, or AutoStore on power down
- RECALL to SRAM initiated by software or power up
- Infinite read, write, and recall cycles
- 1 million STORE cycles to QuantumTrap
- 20 year data retention
- Core $V_{CC}$ = 2.7 V to 3.6 V; I/O $V_{CCQ}$ = 1.65 V to 1.95 V
- Industrial temperature
- 48-ball fine-pitch ball grid array (FBGA) package
- Pb-free and restriction of hazardous substances (RoHS) compliance

## Functional Description

The Cypress CY14U256LA is a fast static RAM, with a nonvolatile element in each memory cell. The memory is organized as 32 K bytes of 8 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

For a complete list of related documentation, click here.

## Logic Block Diagram



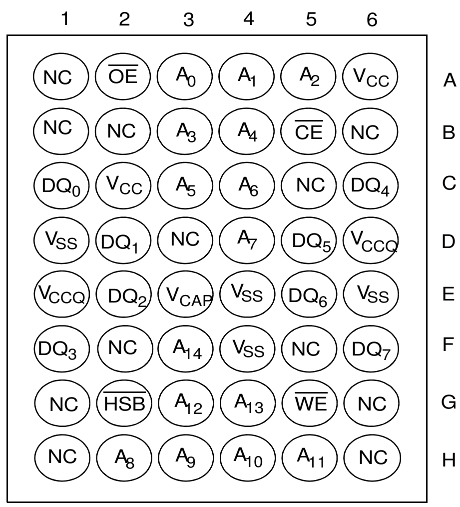
## Contents

## Pinout

**Figure 1. 48-ball FBGA (6 × 10 × 1.2 mm) pinout**

**(× 8)**

**Top View**
**(not to scale)**




## Pin Definitions

| Pin Name | I/O Type | Description |
|---|---|---|
| $A_0$–$A_{14}$ | Input | Address inputs. Used to select one of the 32,768 bytes of the nvSRAM. |
| $DQ_0$–$DQ_7$ | Input/Output | Bidirectional data I/O lines. Used as input or output lines depending on operation. |
| $\overline{WE}$ | Input | Write enable input, active LOW. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location. |
| $\overline{CE}$ | Input | Chip enable input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip. |
| $\overline{OE}$ | Input | Output enable, active LOW. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. I/O pins are tri-stated on deasserting $\overline{OE}$ HIGH. |
| $V_{SS}$ | Ground | Ground for the device. Must be connected to the ground of the system. |
| $V_{CC}$ | Power supply | Power supply inputs to the core of the device. |
| $V_{CCQ}$ | Power supply | Power supply inputs for the inputs and outputs of the device. |
| $\overline{HSB}$ | Input/Output | Hardware STORE busy ($\overline{HSB}$). When LOW, this output indicates that a Hardware STORE is in progress. When pulled LOW, external to the chip, it initiates a nonvolatile STORE operation. After each hardware and software STORE operation $\overline{HSB}$ is driven HIGH for a short time ($t_{HHHD}$) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional). |
| $V_{CAP}$ | Power supply | AutoStore capacitor. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements. |
| NC | No connect | No connect. This pin is not connected to the die. |

## Device Operation

The CY14U256LA nvSRAM is made up of two functional components paired in the same physical cell. They are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14U256LA supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. Refer to the Truth Table for SRAM Operations on page 17 for a complete description of read and write modes.

### SRAM Read

The CY14U256LA performs a read cycle when $\overline{CE}$ and $\overline{OE}$ are LOW and $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins $A_{0-14}$ determines which of the 32,768 data bytes each are accessed. When the read is initiated by an address transition, the outputs are valid after a delay of $t_{AA}$ (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at $t_{ACE}$ or at $t_{DOE}$, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the $t_{AA}$ access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

### SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins $DQ_{0-7}$ are written into the memory if the data is valid $t_{SD}$ before the end of a $\overline{WE}$-controlled write or before the end of a $\overline{CE}$-controlled write. Keep $\overline{OE}$ HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers $t_{HZWE}$ after $\overline{WE}$ goes LOW.

### AutoStore Operation

The CY14U256LA stores data to the nvSRAM using one of the following three storage operations: Hardware STORE activated by $\overline{HSB}$; Software STORE activated by an address sequence; AutoStore on device power down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14U256LA.

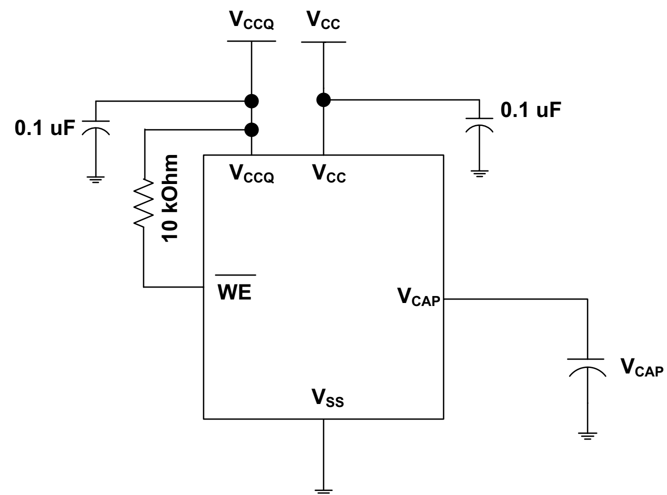
During a normal operation, the device draws current from $V_{CC}$ to charge a capacitor connected to the $V_{CAP}$ pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the $V_{CC}$ pin drops below $V_{SWITCH}$ the part automatically disconnects the $V_{CAP}$ pin from $V_{CC}$. A STORE operation is initiated with power provided by the $V_{CAP}$ capacitor.

**Note** If a capacitor is not connected to $V_{CAP}$ pin, AutoStore must be disabled using the soft sequence specified in Preventing AutoStore on page 6. If AutoStore is enabled without a capacitor on $V_{CAP}$ pin, the device attempts an AutoStore operation without sufficient charge to complete the Store. This corrupts the data stored in nvSRAM.

Figure 2 shows the proper connection of the storage capacitor ($V_{CAP}$) for automatic STORE operation. Refer to DC Electrical Characteristics on page 7 for the size of $V_{CAP}$. The voltage on the $V_{CAP}$ pin is driven to $V_{CC}$ by a regulator on the chip. Place a pull-up on $\overline{WE}$ to hold it inactive during power up. This pull-up is only effective if the $\overline{WE}$ signal is tristate during power up. Many MPUs tristate their controls on power-up. This must be verified when using the pull-up. When the nvSRAM comes out of power-on-RECALL, the MPU must be active or the $\overline{WE}$ held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The $\overline{HSB}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.

**Figure 2. AutoStore Mode**




### Hardware STORE Operation

The CY14U256LA provides the $\overline{HSB}$ pin to control and acknowledge the STORE operations. Use the $\overline{HSB}$ pin to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the CY14U256LA conditionally initiates a STORE operation after $t_{DELAY}$. An actual STORE cycle only begins if a write to the SRAM has taken place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver (internal 100 kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

**Note** After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time ($t_{HHHD}$) with standard output high current and then remains HIGH by internal 100 kΩ pull-up resistor.

SRAM write operations that are in progress when $\overline{HSB}$ is driven LOW by any means are given time ($t_{DELAY}$) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after $\overline{HSB}$ goes LOW are inhibited until $\overline{HSB}$ returns HIGH. In case the write latch is not set, $\overline{HSB}$ is not driven LOW by the CY14U256LA. But any SRAM read and write cycles are inhibited until $\overline{HSB}$ is returned HIGH by MPU or other external source.

During any STORE operation, regardless of how it is initiated, the CY14U256LA continues to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for $t_{LZHSB}$ time after $\overline{HSB}$ pin returns HIGH. Leave the $\overline{HSB}$ unconnected if it is not used.

### Hardware RECALL (Power-Up)

During power up or after any low-power condition ($V_{CC}$< $V_{SWITCH}$), an internal RECALL request is latched. When $V_{CC}$ again exceeds the sense voltage of $V_{SWITCH}$, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, $\overline{HSB}$ is driven LOW by the $\overline{HSB}$ driver.

### Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14U256LA Software STORE cycle is initiated by executing sequential $\overline{CE}$ or $\overline{OE}$ controlled read cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read Address 0x0E38 Valid READ
2. Read Address 0x31C7 Valid READ
3. Read Address 0x03E0 Valid READ
4. Read Address 0x3C1F Valid READ
5. Read Address 0x303F Valid READ
6. Read Address 0x0FC0 Initiate STORE Cycle

The software sequence may be clocked with $\overline{CE}$ controlled reads or $\overline{OE}$ controlled reads, with $\overline{WE}$ kept HIGH for all the six READ sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. $\overline{HSB}$ is driven LOW. After the $t_{STORE}$ cycle time is fulfilled, the SRAM is activated again for the read and write operation.

### Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A Software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read Address 0x0E38 Valid READ
2. Read Address 0x31C7 Valid READ
3. Read Address 0x03E0 Valid READ
4. Read Address 0x3C1F Valid READ
5. Read Address 0x303F Valid READ
6. Read Address 0x0C63 Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared. Next, the nonvolatile information is transferred into the SRAM cells. After the $t_{RECALL}$ cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

**Table 1. Mode Selection**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $A_{14}$–$A_0$ [1] | Mode | I/O | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | Not selected | Output High Z | Standby |
| L | H | L | X | Read SRAM | Output data | Active |
| L | L | X | X | Write SRAM | Input data | Active |
| L | H | L | 0x0E38<br>0x31C7<br>0x03E0<br>0x3C1F<br>0x303F<br>0x0B45 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>AutoStore Disable | Output data<br>Output data<br>Output data<br>Output data<br>Output data<br>Output data | Active [2] |

**Notes**
1. While there are 15 address lines on the CY14U256LA, only the 13 address lines ($A_{14}$–$A_2$) are used to control software modes. Rest of the address lines are don't care.
2. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile cycle.

**Table 1. Mode Selection** (continued)

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $A_{14}$–$A_0$[1] | Mode | I/O | Power |
|---|---|---|---|---|---|---|
| L | H | L | 0x0E38<br>0x31C7<br>0x03E0<br>0x3C1F<br>0x303F<br>0x0B46 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>AutoStore Enable | Output data<br>Output data<br>Output data<br>Output data<br>Output data<br>Output data | Active[3] |
| L | H | L | 0x0E38<br>0x31C7<br>0x03E0<br>0x3C1F<br>0x303F<br>0x0FC0 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile STORE | Output data<br>Output data<br>Output data<br>Output data<br>Output data<br>Output High Z | Active $I_{CC2}$[3] |
| L | H | L | 0x0E38<br>0x31C7<br>0x03E0<br>0x3C1F<br>0x303F<br>0x0C63 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile RECALL | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | Active[3] |

## Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x0E38 Valid READ
2. Read address 0x31C7 Valid READ
3. Read address 0x03E0 Valid READ
4. Read address 0x3C1F Valid READ
5. Read address 0x303F Valid READ
6. Read address 0x0B45 AutoStore Disable

The AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the Software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x0E38 Valid READ
2. Read address 0x31C7 Valid READ
3. Read address 0x03E0 Valid READ
4. Read address 0x3C1F Valid READ
5. Read address 0x303F Valid READ
6. Read address 0x0B46 AutoStore Enable

If the AutoStore function is disabled or reenabled, a manual STORE operation (Hardware or Software) must be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled and written 0x00 in all cells.

## Data Protection

The CY14U256LA protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low-voltage condition is detected when $V_{CC} \leq V_{SWITCH}$. If the CY14U256LA is in a write mode (both $\overline{CE}$ and $\overline{WE}$ are LOW) at power up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after $t_{LZHSB}$ ($\overline{HSB}$ to output active). When $V_{CCQ} < V_{IODIS}$, I/Os are disabled (no STORE takes place). This protects against inadvertent writes during brown out conditions on $V_{CCQ}$ supply.

**Note**
3. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile cycle.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ................................ –65 °C to +150 °C

Maximum accumulated storage time:

At 150 °C ambient temperature ..................... 1000 h

At 85 °C ambient temperature .................... 20 Years

Maximum junction temperature ................................ 150 °C

Supply voltage on $V_{CC}$ relative to $V_{SS}$ ...........–0.5 V to 4.1 V

Supply voltage on $V_{CCQ}$ relative to $V_{SS}$ ......–0.5 V to 2.45 V

Voltage applied to outputs in High Z State .................................–0.5 V to $V_{CCQ}$ + 0.5 V

Input voltage ....................................–0.5 V to $V_{CCQ}$ + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential ...............–2.0 V to $V_{CCQ}$ + 2.0 V

Package power dissipation capability ($T_A$ = 25 °C) ................................................ 1.0 W

Surface mount Pb soldering temperature (3 seconds) ........................................ +260 °C

DC output current (1 output at a time, 1s duration) ................................. 15 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ........................ > 2001 V

Latch up current .................................................... > 140 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ | $V_{CCQ}$ |
|---|---|---|---|
| Industrial | –40 °C to +85 °C | 2.7 V to 3.6 V | 1.65 V to 1.95 V |

## DC Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | Min | Typ [4] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | 2.7 | 3.0 | 3.6 | V |
| $V_{CCQ}$ | | | 1.65 | 1.8 | 1.95 | V |
| $I_{CC1}$ | Average $V_{CC}$ current | $t_{RC}$ = 35 ns<br>Values obtained without output loads ($I_{OUT}$ = 0 mA) | – | – | 60 | mA |
| $I_{CCQ1}$ | Average $V_{CCQ}$ current | | – | – | 20 | mA |
| $I_{CC2}$ | Average $V_{CC}$ current during STORE | All inputs don't care, $V_{CC}$ = Max<br>Average current for duration $t_{STORE}$ | – | – | 10 | mA |
| $I_{CC3}$ | Average $V_{CC}$ current at $t_{RC}$ = 200 ns, $V_{CC(Typ)}$, 25 °C | All inputs cycling at CMOS levels. Values obtained without output loads ($I_{OUT}$ = 0 mA) | – | 35 | – | mA |
| $I_{CCQ3}$ | Average $V_{CCQ}$ current at $t_{RC}$ = 200 ns, $V_{CCQ(Typ)}$, 25 °C | | – | 5 | – | mA |
| $I_{CC4}$ | Average $V_{CAP}$ current during AutoStore cycle | All inputs don't care. Average current for duration $t_{STORE}$ | – | – | 8 | mA |
| $I_{SB}$ | $V_{CC}$ standby current | $\overline{CE} \geq (V_{CCQ} - 0.2$ V).<br>$V_{IN} \leq 0.2$ V or $\geq (V_{CCQ} - 0.2$ V).<br>Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz | – | – | 8 | mA |
| $I_{IX}$[5] | Input leakage current (except $\overline{HSB}$) | $V_{CCQ}$ = Max, $V_{SS} \leq V_{IN} \leq V_{CCQ}$ | –1 | – | +1 | µA |
| | Input leakage current (for $\overline{HSB}$) | $V_{CCQ}$ = Max, $V_{SS} \leq V_{IN} \leq V_{CCQ}$ | –100 | – | +1 | µA |

**Notes**

4. Typical values are at 25 °C, $V_{CC} = V_{CC(Typ)}$ and $V_{CCQ} = V_{CCQ(Typ)}$. Not 100% tested.
5. The $\overline{HSB}$ pin has $I_{OUT}$ = –4 µA for $V_{OH}$ of 1.07 V when both active HIGH and LOW drivers are disabled. When they are enabled standard $V_{OH}$ and $V_{OL}$ are valid. This parameter is characterized but not tested.

## DC Electrical Characteristics (continued)

Over the Operating Range

| Parameter | Description | Test Conditions | Min | Typ [4] | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OZ}$ | Off-state output leakage current | $V_{CCQ}$ = Max, $V_{SS} \le V_{OUT} \le V_{CCQ}$, $\overline{CE}$ or $\overline{OE} \ge V_{IH}$ or $\overline{WE} \le V_{IL}$ | –1 | – | +1 | μA |
| $V_{IH}$ | Input HIGH voltage | – | 0.7 × $V_{CCQ}$ | – | $V_{CCQ}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | – | – 0.3 | – | 0.3 × $V_{CCQ}$ | V |
| $V_{OH}$ | Output HIGH voltage | $I_{OUT}$ = –1 mA | $V_{CCQ}$ – 0.45 | – | – | V |
| $V_{OL}$ | Output LOW voltage | $I_{OUT}$ = 2 mA | – | – | 0.45 | V |
| $V_{CAP}$ [6] | Storage capacitor | Between $V_{CAP}$ pin and $V_{SS}$ | 120 | 150 | 180 | μF |
| $V_{VCAP}$ [7, 8] | Maximum voltage driven on $V_{CAP}$ pin by the device | $V_{CC}$ = Max | – | – | $V_{CC}$ | V |

## Data Retention and Endurance

| Parameter | Description | Min | Unit |
|---|---|---|---|
| $DATA_R$ | Data retention | 20 | Years |
| $NV_C$ | Nonvolatile STORE operations | 1,000 | K |

## Capacitance

| Parameter [8] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance (except $\overline{HSB}$) | $T_A$ = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(Typ)}$, $V_{CCQ} = V_{CCQ(Typ)}$ | 7 | pF |
| | Input capacitance (for $\overline{HSB}$) | | 8 | pF |
| $C_{OUT}$ | Output capacitance (except $\overline{HSB}$) | | 7 | pF |
| | Output capacitance (for $\overline{HSB}$) | | 8 | pF |

## Thermal Resistance

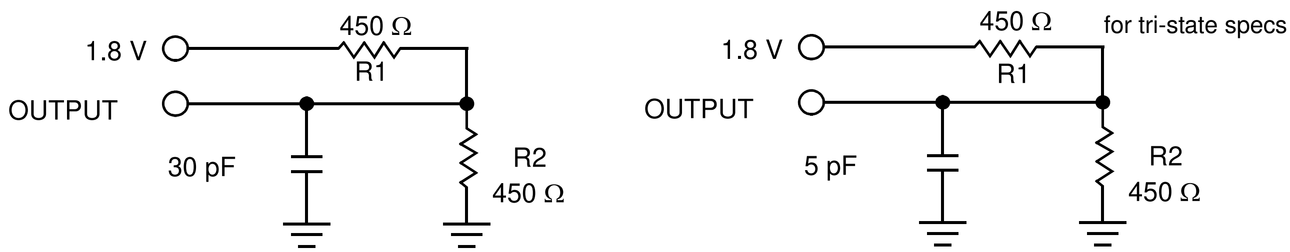
| Parameter [8] | Description | Test Conditions | 48-ball FBGA | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 48.19 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 6.5 | °C/W |

**Notes**

6. Min $V_{CAP}$ value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max $V_{CAP}$ value guarantees that the capacitor on $V_{CAP}$ is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. Refer application note AN43593 for more details on $V_{CAP}$ options.
7. Maximum voltage on $V_{CAP}$ pin ($V_{VCAP}$) is provided for guidance when choosing the $V_{CAP}$ capacitor. The voltage rating of the $V_{CAP}$ capacitor across the operating temperature range should be higher than the $V_{VCAP}$ voltage.
8. These parameters are guaranteed by design and are not tested.

## AC Test Loads

**Figure 3. AC Test Loads**




## AC Test Conditions

Input pulse levels ................................................0 V to 1.8 V

Input rise and fall times (10% to 90%) .................... $\leq$ 1.8 ns

Input and output timing reference levels ....................... 0.9 V

## AC Switching Characteristics

Over the Operating Range

| Parameters [9] | | Description | 35 ns | | Unit |
|---|---|---|---|---|---|
| Cypress Parameters | Alt Parameters | | Min | Max | |
| **SRAM Read Cycle** | | | | | |
| $t_{ACE}$ | $t_{ACS}$ | Chip enable access time | – | 35 | ns |
| $t_{RC}$[10] | $t_{RC}$ | Read cycle time | 35 | – | ns |
| $t_{AA}$[11] | $t_{AA}$ | Address access time | – | 35 | ns |
| $t_{DOE}$ | $t_{OE}$ | Output enable to data valid | – | 15 | ns |
| $t_{OHA}$[11] | $t_{OH}$ | Output hold after address change | 3 | – | ns |
| $t_{LZCE}$[12, 13] | $t_{LZ}$ | Chip enable to output active | 3 | – | ns |
| $t_{HZCE}$[12, 13] | $t_{HZ}$ | Chip disable to output inactive | – | 13 | ns |
| $t_{LZOE}$[12, 13] | $t_{OLZ}$ | Output enable to output active | 0 | – | ns |
| $t_{HZOE}$[12, 13] | $t_{OHZ}$ | Output disable to output inactive | – | 13 | ns |
| $t_{PU}$[12] | $t_{PA}$ | Chip enable to power active | 0 | – | ns |
| $t_{PD}$[12] | $t_{PS}$ | Chip disable to power standby | – | 35 | ns |
| **SRAM Write Cycle** | | | | | |
| $t_{WC}$ | $t_{WC}$ | Write cycle time | 35 | – | ns |
| $t_{PWE}$ | $t_{WP}$ | Write pulse width | 25 | – | ns |
| $t_{SCE}$ | $t_{CW}$ | Chip enable to end of write | 25 | – | ns |
| $t_{SD}$ | $t_{DW}$ | Data setup to end of write | 12 | – | ns |
| $t_{HD}$ | $t_{DH}$ | Data hold after end of write | 0 | – | ns |
| $t_{AW}$ | $t_{AW}$ | Address setup to end of write | 25 | – | ns |
| $t_{SA}$ | $t_{AS}$ | Address setup to start of write | 0 | – | ns |
| $t_{HA}$ | $t_{WR}$ | Address hold after end of write | 0 | – | ns |
| $t_{HZWE}$[12, 13, 14] | $t_{WZ}$ | Write enable to output disable | – | 13 | ns |
| $t_{LZWE}$[12, 13] | $t_{OW}$ | Output active after end of write | 3 | – | ns |

**Notes**

9. Test conditions assume signal transition time of 1.8 ns or less, timing reference levels of $V_{CCQ}/2$, input pulse levels of 0 to $V_{CC\,Q(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ and load capacitance shown in Figure 3 on page 9.
10. $\overline{WE}$ must be HIGH during SRAM read cycles.
11. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ LOW.
12. These parameters are guaranteed by design and are not tested.
13. Measured ±200 mV from steady state output voltage.
14. If $\overline{WE}$ is low when $\overline{CE}$ goes low, the outputs remain in the high-impedance state.

## Switching Waveforms

**Figure 4. SRAM Read Cycle #1 (Address Controlled)** [15, 16, 17]

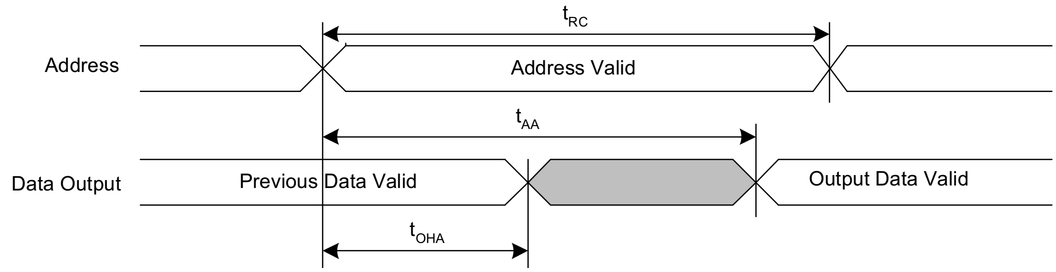
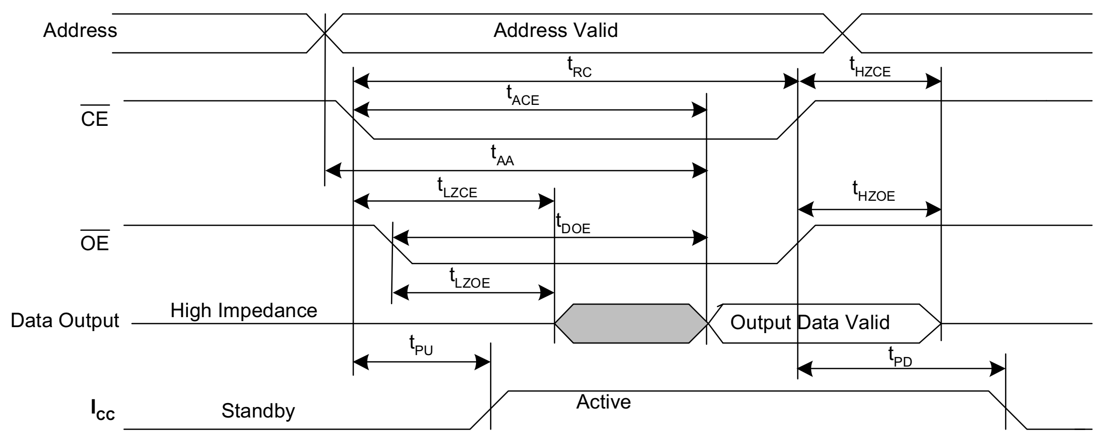



**Figure 5. SRAM Read Cycle #2 ($\overline{CE}$ and $\overline{OE}$ Controlled)** [15, 17]




**Notes**
15. $\overline{WE}$ must be HIGH during SRAM read cycles.
16. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ LOW.
17. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.

## Switching Waveforms (continued)

**Figure 6. SRAM Write Cycle #1 (WE Controlled) [18, 19, 20]**

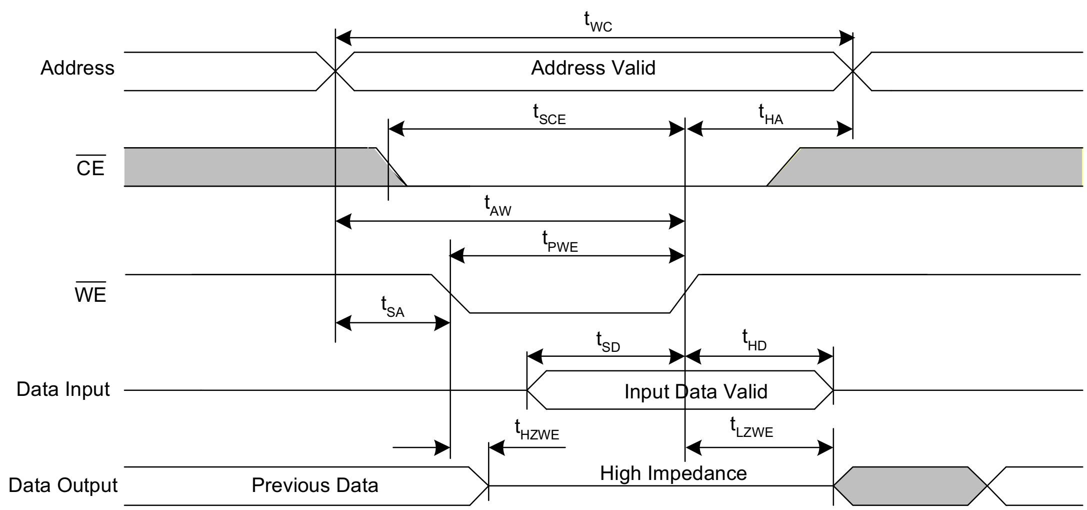
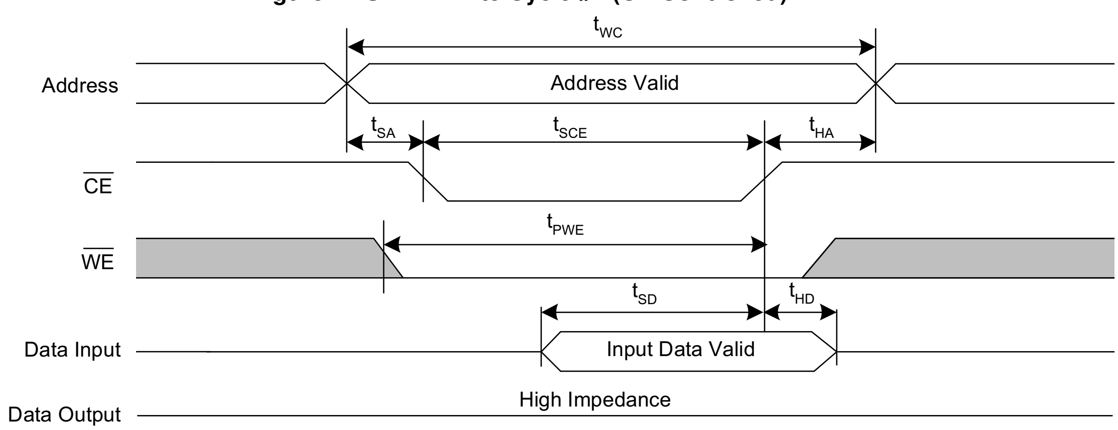



**Figure 7. SRAM Write Cycle #2 (CE Controlled) [18, 19, 20]**




**Notes**
18. HSB must remain HIGH during READ and WRITE cycles.
19. If WE is low when CE goes low, the outputs remain in the high impedance state.
20. CE or WE must be ≥ $V_{IH}$ during address transitions.

## AutoStore/Power-up RECALL

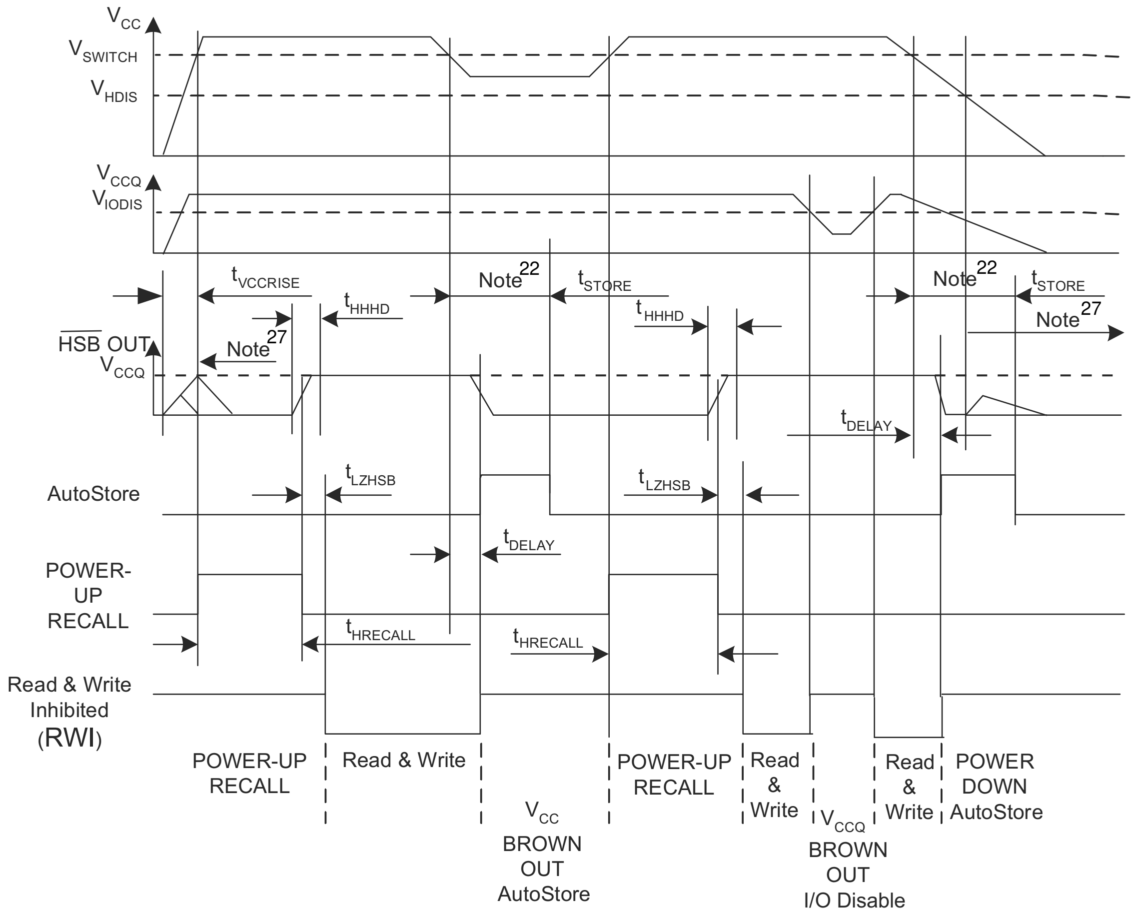
Over the Operating Range

| Parameter | Description | CY14U256LA | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{HRECALL}$ [21] | Power-up RECALL duration | – | 20 | ms |
| $t_{STORE}$ [22] | STORE cycle duration | – | 8 | ms |
| $t_{DELAY}$ [23] | Time allowed to complete SRAM write cycle | – | 25 | ns |
| $V_{SWITCH}$ | Low voltage trigger level for $V_{CC}$ | – | 2.65 | V |
| $V_{IODIS}$[24] | I/O disable voltage on $V_{CCQ}$ | – | 1.50 | V |
| $t_{VCCRISE}$[25] | $V_{CC}$ rise time | 150 | – | µs |
| $V_{HDIS}$[25] | $\overline{HSB}$ output disable voltage on $V_{CC}$ | – | 1.9 | V |
| $t_{LZHSB}$[25] | $\overline{HSB}$ to output active time | – | 5 | µs |
| $t_{HHHD}$[25] | $\overline{HSB}$ high active time | – | 500 | ns |

**Notes**
21. $t_{HRECALL}$ starts from the time $V_{CC}$ rises above $V_{SWITCH}$.
22. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
23. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time $t_{DELAY}$.
24. $\overline{HSB}$ is not defined below $V_{IODIS}$ voltage.
25. These parameters are guaranteed by design and are not tested.

## Switching Waveforms

**Figure 8. AutoStore or Power-up RECALL [26]**




**Notes**

26. Read and write cycles are ignored during STORE, RECALL, and while $V_{CC}$ is below $V_{SWITCH}$.
27. During power-up and power-down, HSB glitches when HSB pin is pulled up through an external resistor.

## Software Controlled STORE/RECALL Cycle

Over the Operating Range

| Parameter [28, 29] | Description | 35 ns | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{RC}$ | STORE/RECALL initiation cycle time | 35 | – | ns |
| $t_{SA}$ | Address setup time | 0 | – | ns |
| $t_{CW}$ | Clock pulse width | 20 | – | ns |
| $t_{HA}$ | Address hold time | 0 | – | ns |
| $t_{RECALL}$ | RECALL duration | – | 200 | µs |

## Switching Waveforms

**Figure 9. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE/RECALL Cycle [29]**

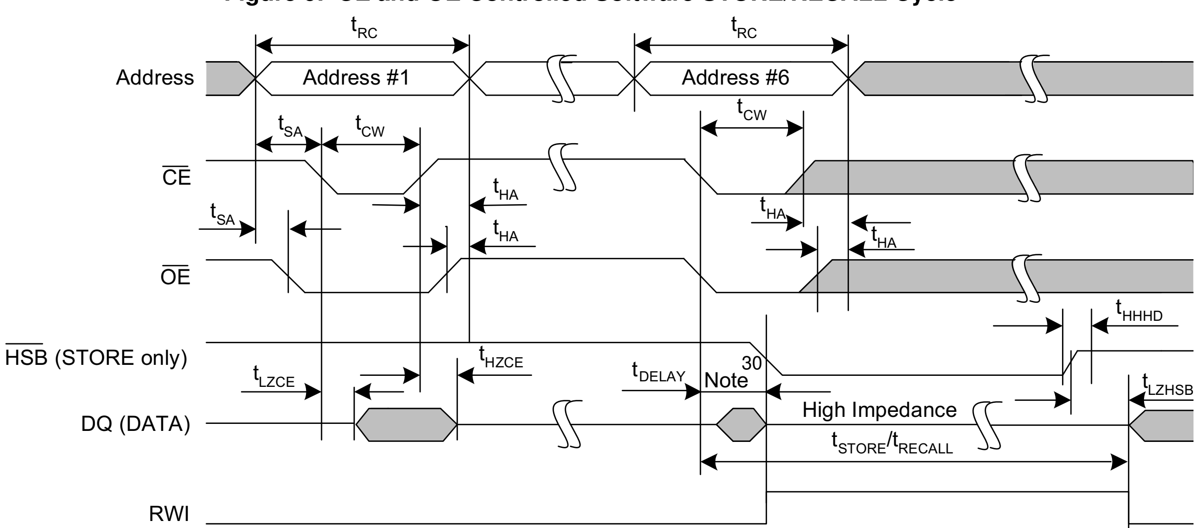
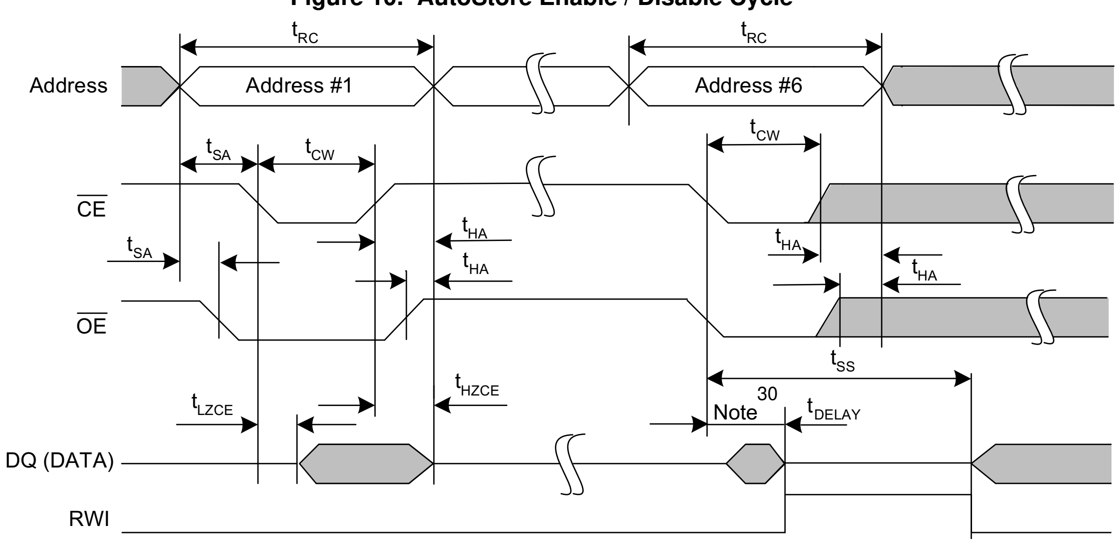



**Figure 10. AutoStore Enable / Disable Cycle [29]**




**Notes**

28. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
29. The six consecutive addresses must be read in the order listed in Table 1 on page 5. $\overline{WE}$ must be HIGH during all six consecutive cycles.
30. DQ output data at the sixth read may be invalid since the output is disabled at $t_{DELAY}$ time.

## Hardware STORE Cycle

Over the Operating Range

| Parameters | Description | CY14U256LA | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{DHSB}$ | $\overline{HSB}$ to output active time when write latch not set | – | 25 | ns |
| $t_{PHSB}$ | Hardware STORE pulse width | 15 | – | ns |
| $t_{SS}$ [31, 32] | Soft sequence processing time | – | 100 | µs |

## Switching Waveforms

**Figure 11. Hardware STORE Cycle [33]**

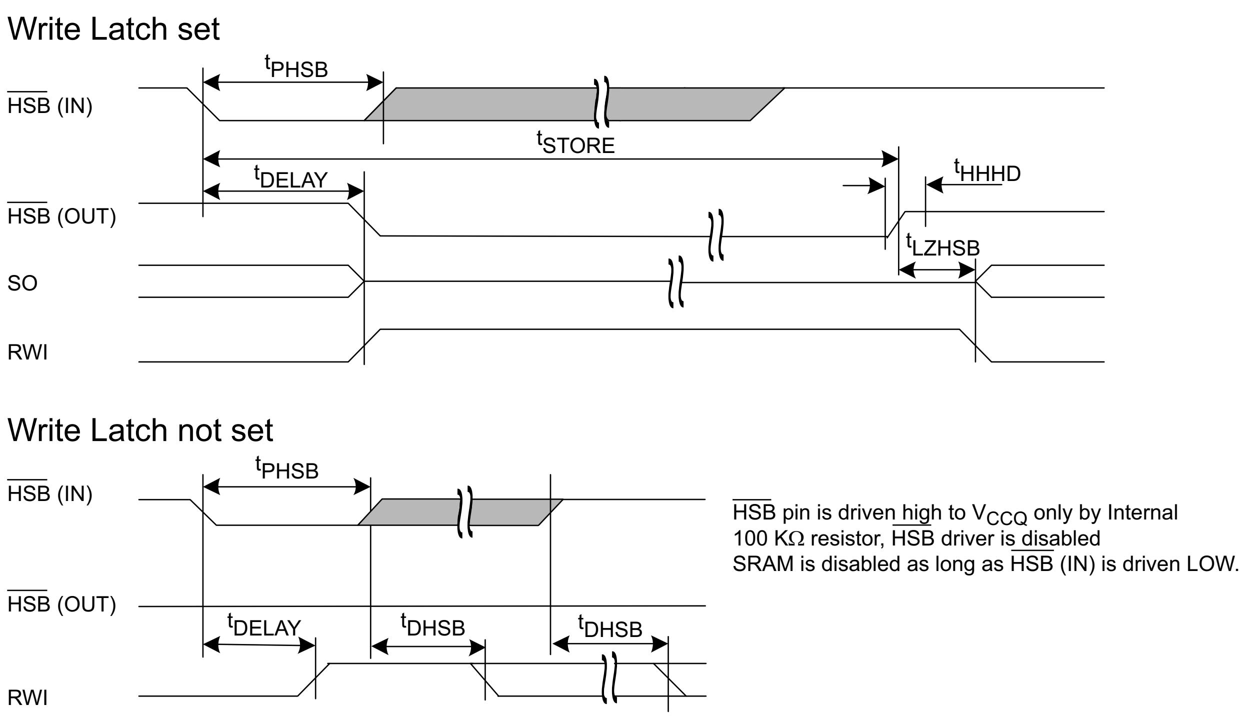
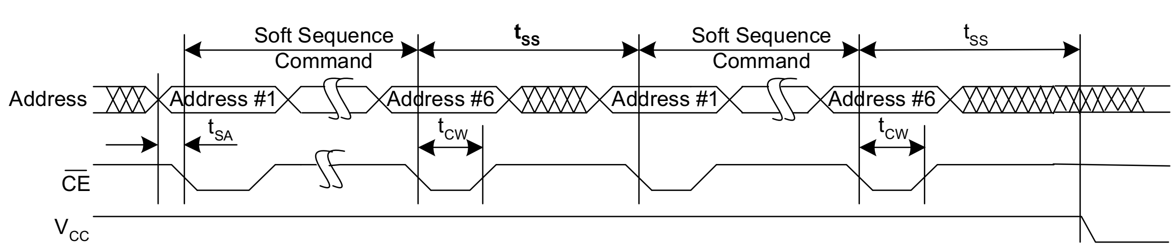



**Figure 12. Soft Sequence Processing [31, 32]**




**Notes**

31. This is the amount of time it takes to take action on a soft sequence command. $V_{CC}$ and $V_{CCQ}$ power must remain HIGH to effectively register command.
32. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
33. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.

## Truth Table for SRAM Operations

$\overline{HSB}$ must remain HIGH for SRAM operations.

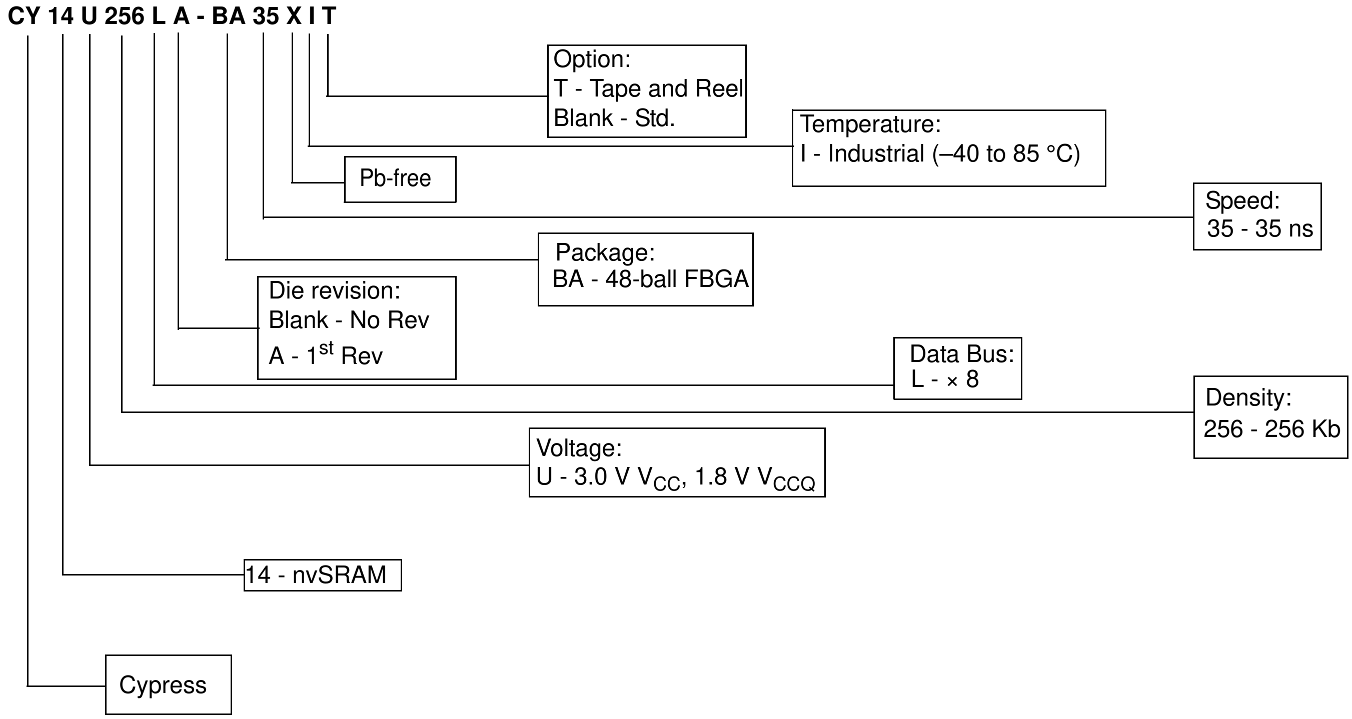
| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|
| H | X | X | High Z | Deselect / Power-down | Standby |
| L | H | L | Data out ($DQ_0$–$DQ_7$) | Read | Active |
| L | H | H | High Z | Output disabled | Active |
| L | L | X | Data in ($DQ_0$–$DQ_7$) | Write | Active |

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 35 | CY14U256LA-BA35XIT | 51-85128 | 48-ball FBGA | Industrial |
| | CY14U256LA-BA35XI | | | |

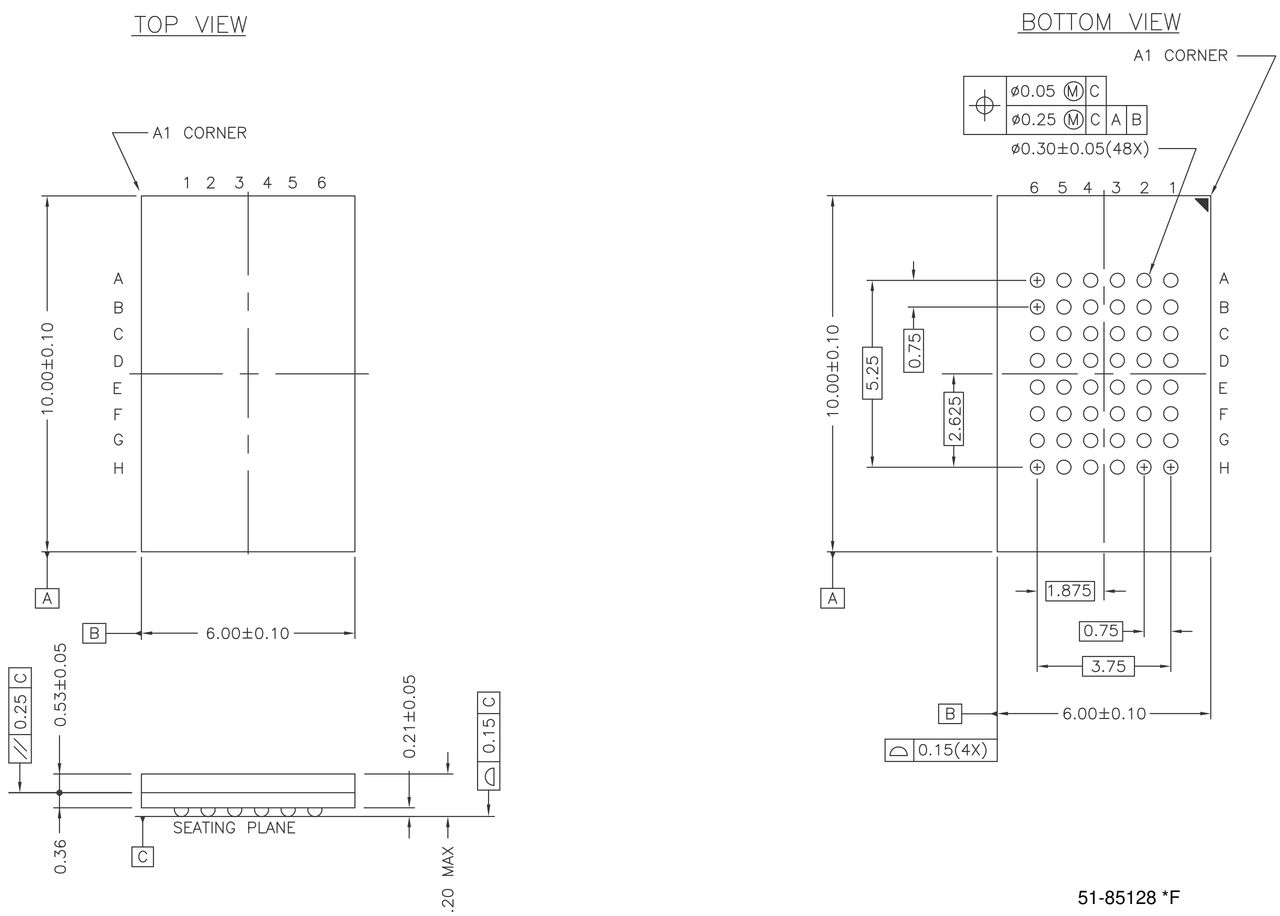
All parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

### Ordering Code Definitions



## Package Diagrams

**Figure 13. 48-ball FBGA (6 × 10 × 1.2 mm) BA48B Package Outline, 51-85128**




51-85128 *F

## Acronyms

| Acronym | Description |
|---|---|
| $\overline{CE}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| EIA | Electronic Industries Alliance |
| FBGA | Fine-Pitch Ball Grid Array |
| $\overline{HSB}$ | Hardware Store Busy |
| I/O | Input/Output |
| nvSRAM | Nonvolatile Static Random Access Memory |
| $\overline{OE}$ | Output Enable |
| SRAM | Static Random Access Memory |
| RoHS | Restriction of Hazardous Substances |
| RWI | Read and Write Inhibited |
| $\overline{WE}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| kΩ | kilohm |
| MHz | megahertz |
| µA | microampere |
| µF | microfarad |
| µs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY14U256LA, 256-Kbit (32 K × 8) nvSRAM<br>Document Number: 001-86200 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 3918324 | GVCH | 03/01/2013 | New data sheet. |
| *A | 4024815 | GVCH | 06/10/2013 | Changed status from “Summary” to “Final”.<br>Updated Maximum Ratings:<br>Removed “Ambient temperature with power applied” and added “Maximum junction temperature”. |
| *B | 4568158 | GVCH | 11/13/2014 | Added related documentation hyperlink in page 1. |

# Sales, Solutions, and Legal Information

## Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

### Products

| | |
|---|---|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc |
| | cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

### PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5