DSLVDS1047-1048EVM User's Guide

The DSLVDS1047-1048EVM is an evaluation module designed for performance and functional evaluation of the Texas Instruments DSLVDS1047 3-V LVDS Quad CMOS Differential Line Driver and DSLVDS1048 3-V LVDS CMOS Differential Line Receiver. With this kit, users can quickly evaluate the output waveform characteristics and signal integrity supported by the DSLVDS1047 and DSLVDS1048. Header pins allow access to the DSLVDS1047 and DSLVDS1048 inputs and outputs and also facilitate connection to lab equipment or user systems for performance evaluation.

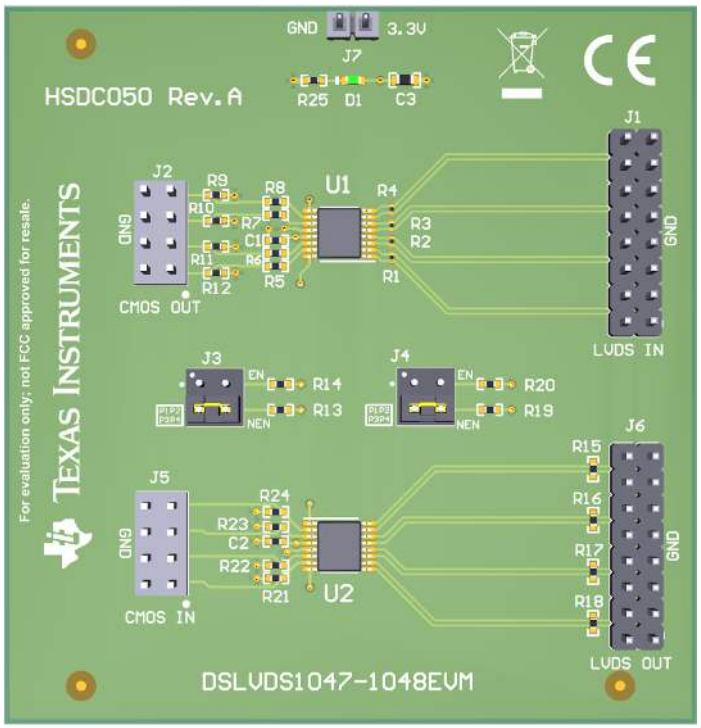

Figure 1. DSLVDS1047-1048EVM

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1 Features

DSLVDS1047:

- Converts Single-Ended LVCMOS to Differential LVDS
- >400 Mbps (200 MHz) Switching Rates
- Single Supply Operation: VDD = 3.3 V ± 5%
- Low Power (13 mW at 3.3 V Static)
- Interoperable With Existing 5-V LVDS Receivers
- Flow-Through Pinout Simplifies PCB Layout

DSLVDS1048:

- Converts Differential LVDS to Single-Ended LVCMOS
- >400 Mbps (200 MHz) Switching Rates
- Single Supply Operation: VDD = 3.3 V ± 5%
- Accepts Small ±35 mV Differential Signaling
- Supports Input Failsafe – Open, Short, and Terminated
- Low Power Design (40 mW at 3.3 V Static)
- Flow-Through Pinout Simplifies PCB Layout

2 Applications

- Multifunction Printers
- Board-to-Board Communication
- Test and Measurement
- Printers
- Data Center Interconnect
- Lab Instrumentation
- Ultrasound Scanners

3 Ordering Information

EVM ID	Device ID	Device Package
DSLVDS1047-1048EVM	DSLVDS1047, DSLVDS1048	SOIC

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4 Setup

The DSLVDS1047 is a LVDS Quad CMOS Differential Line Driver, and the DSLVDS1048 is a LVDS Quad CMOS Differential Line Receiver. When operating the DSLVDS1047-1048EVM, jumper setting definitions can be referenced in Table 1, while signal input and output connection descriptions can be found in Figure 2 and Figure 3. When using the DSLVDS1047 and DSLVDS1048 together, the typical configuration is to connect the DSLVDS1047 outputs (J6) such that they drive the inputs of the DSLVDS1048 (J1).

Table 1. Description of Jumper Settings

Component	Name	Comments
J7	VDD/GND	3.3 V VDD power supply
J3	ENABLE1	Leave Pins 1 and 2 open, and tie Pins 3 and 4 to enable DSLVDS1048.
J4	ENABLE2	Leave Pins 1 and 2 open, and tie Pins 3 and 4 to enable DSLVDS1047.

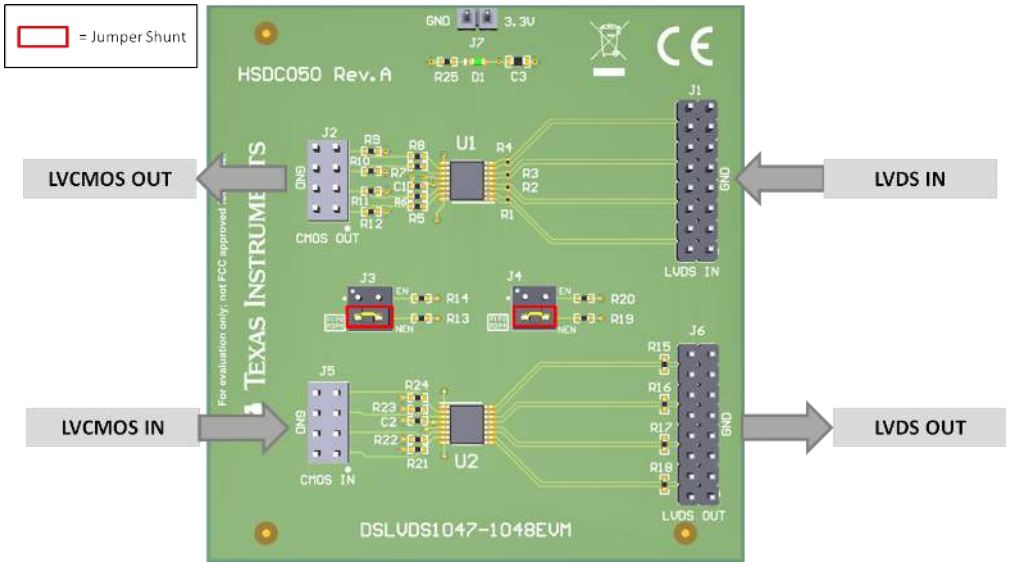

Figure 2. DSLVDS1047-1048EVM Input and Output Diagram

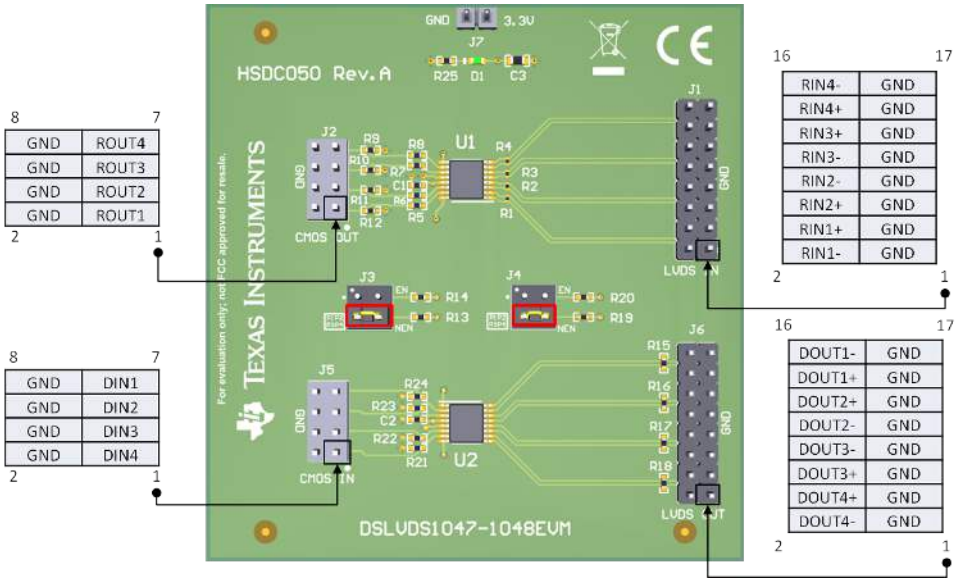

Figure 3. DSLVDS1047-1048EVM Input and Output Header Connections

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4.1 Hardware Description and Setup

For hardware setup and connections, reference the diagrams in Figure 3 and Figure 4.

1. Connect a 3.3 V DC power supply (30 mA max) to the header J7 on EVM.

2. Install a shunt jumper on J3 Pins 3-4 to tie DSLVDS1048 NEN to GND and install a shunt jumper on J4 Pins 3-4 to tie DSLVDS1047 NEN to GND for appropriate operation, as shown in Figure 4.

3. Apply a high-speed 3.3 V LVCMOS signal to the DSLVDS1047 inputs on header J5.

4. The DSLVDS1047 LVDS output signals can be measured deferentially on an oscilloscope by applying a Tektronix P6247 probe or equivalent differential probe at header J6 to measure the differential signal across the 100 Ω termination resistors R15-R18. The expected output waveform is a ±350 mV LVDS signal.

5. Apply a high-speed ±350 mV (700 mV_{pp} differential) LVDS signal to the DSLVDS1048 inputs on header J1. If desired, the LVDS inputs can be provided by connecting the LVDS outputs on header J4 to the desired LVDS input pins on header J1. If this is done, remove resistors R15-R18 to avoid double-termination.

6. The DSLVDS1048 LVCMOS output signals can be measured on an oscilloscope by applying a Tektronix P6247 probe or equivalent differential probe at header J2.

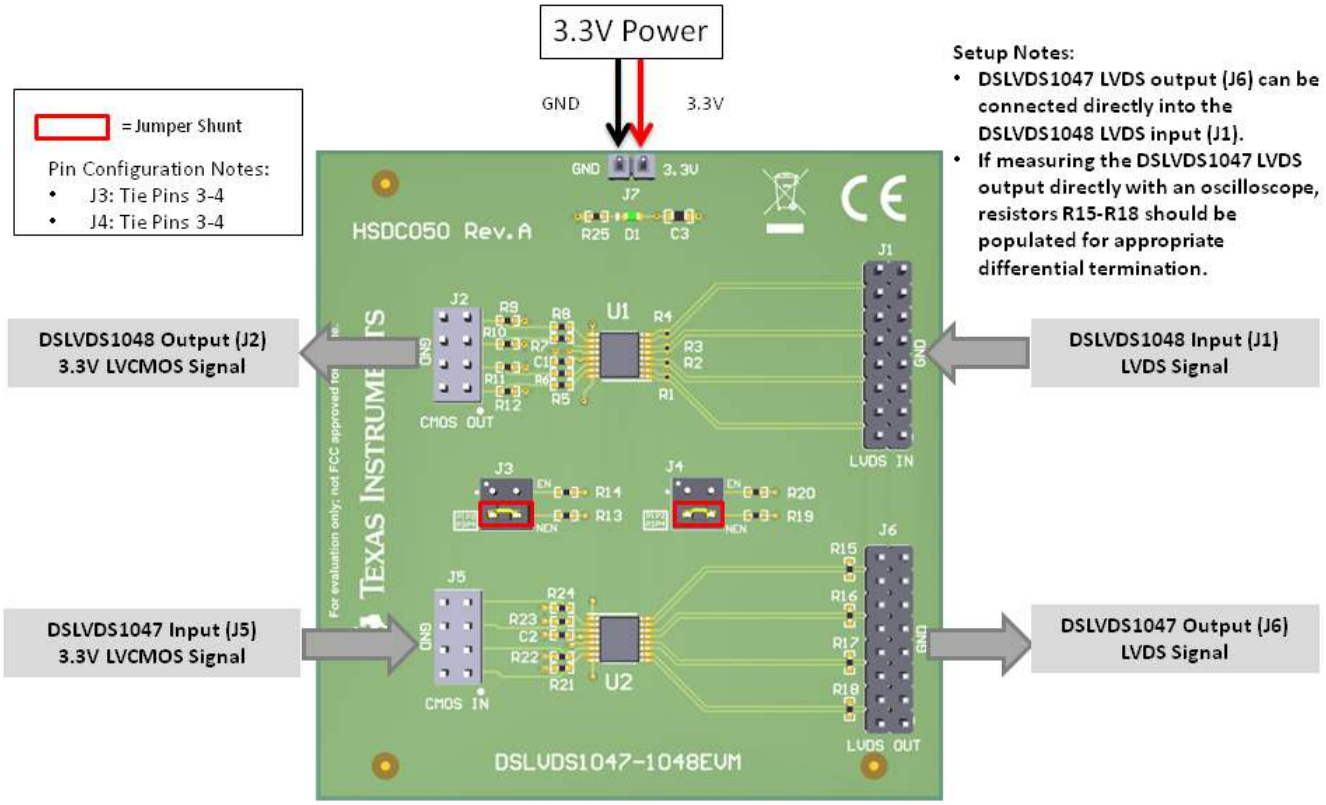

Figure 4. DSLVDS1047-1048EVM Setup Configuration

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In order to measure LVDS signals properly, a 100 Ω termination resistor must be present across each differential pair at the point of measurement. However, if multiple 100 Ω termination resistors are placed across a differential pair between the transmitter and receiver, the signal becomes double terminated. Double termination should be avoided, since this reduces the output amplitude and noise margin.

By factory default, the DSLVDS1047-1048EVM comes with stuffed termination resistors R1-R4 on the DSLVDS1048 inputs and stuffed termination resistors R15-R18 on the DSLVDS1047 outputs.

Remove R15-R18...

- if the DSLVDS1047 output interfaces with a DSLVDS1048 input by connecting J6 to J1.
- if the DSLVDS1047 output interfaces with an external load that has an appropriate 100 Ω differential termination.

Populate R15-R18 with 100 Ω termination resistors (or leave R15-R18 populated)...

- if the DSLVDS1047 output is measured by a high-impedance differential probe.
- if the DSLVDS1047 output interfaces with an external load that does **not** have an appropriate 100 Ω differential termination.

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4.2 DSLVDS1047-1048EVM Performance Plots

The following plots show typical waveforms measured on the DSLVDS1047-1048EVM inputs and outputs using the hardware setup in Figure 4. For these measurements, the following parameters were used:

- Operating Frequency: 200 MHz (400 Mbps)
- DSLVDS1047 Input: 3.3 V LVCMOS sine wave to DIN1
- DSLVDS1047 Output: Measured with 100 Ω termination resistor R15 populated across DOUT1±
- DSLVDS1048 Input: LVDS signal to RIN1± from DSLVDS1047 output DOUT1±. 100 Ω termination resistor R15 removed
- DSLVDS1048 Output: Measured at ROUT1

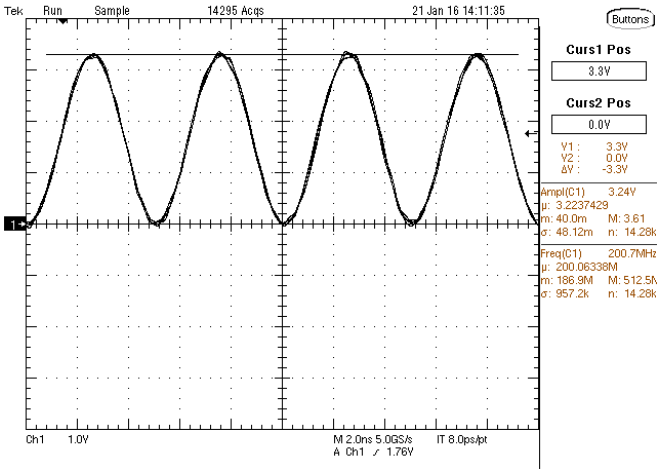

Figure 5. DSLVDS1047 3.3 V LVCMOS Input

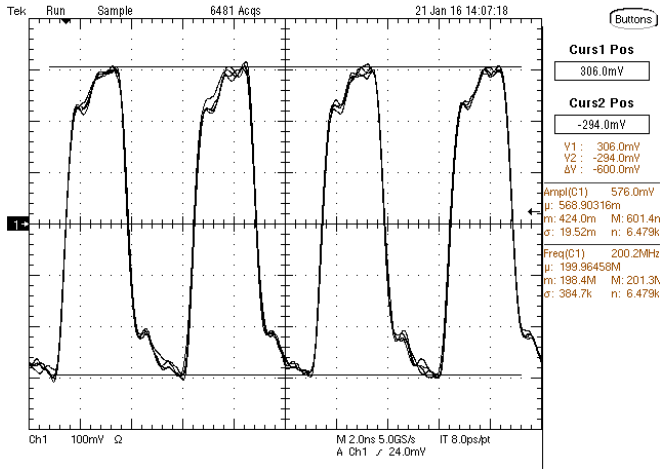

Figure 6. DSLVDS1047 Differential LVDS Output

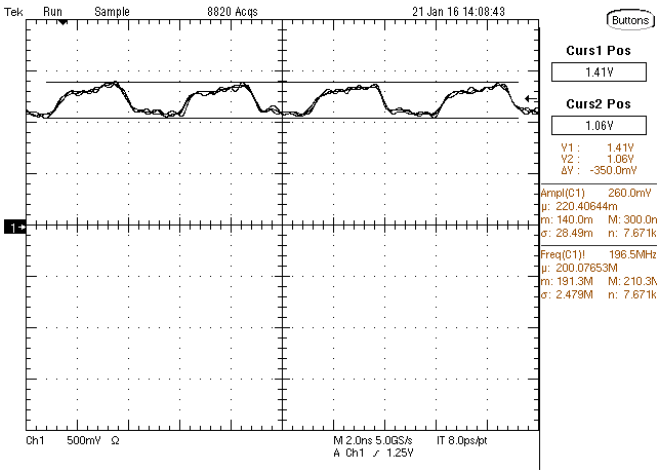

Figure 7. DSLVDS1047 Single-Ended LVDS Output

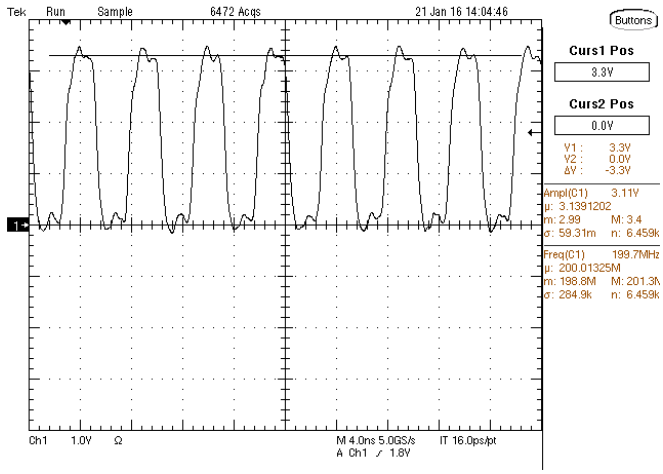

Figure 8. DSLVDS1048 LVCMOS Output

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5 Bill of Materials

Part Number	Description	Designator	Quantity
LMK105BJ104KV-F	CAP, CERM, 0.1 uF, 10 V,+/- 10%, X5R, 0402	C1, C2	2
CL10A106MQ8NNNC	CAP, CERM, 10 uF, 6.3 V, +/- 20%, X5R, 0603	C3	1
SML-LX0603GW-TR	LED, Green, SMD	D1	1
PEC08DAAN	Header, 2.54 mm, 8x2, Tin, Vertical, TH	J1, J6	2
PEC04DAAN	Header, 100 mil, 4x2, Tin, TH	J2, J5	2
PEC02DAAN	Header, 100 mil, 2x2, Tin, TH	J3, J4	2
TSW-102-07-T-S	Header, 2.54 mm, 2x1, Tin, TH	J7	1
RC0201JR-07100RL	RES, 100, 5%, 0.05 W, 0201	R1, R2, R3, R4	4
ERJ-2GE0R00X	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	R5, R6, R7, R8	4
CRCW040210K0FKED	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	R9, R10, R11, R12, R13, R14, R19, R20, R21, R22, R23, R24	12
ERJ-2RKF1000X	RES, 100, 1%, 0.1 W, 0402	R15, R16, R17, R18	4
CRCW0402301RFKED	RES, 301, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	R25	1
SNT-100-BK-G	Shunt, 100mil, Gold plated, Black	SH-J3, SH-J4	2
DSLVDS1048PWR	3-V LVDS Quad CMOS Differential Line Receiver, PW0016A (TSSOP-16)	U1	1
DSLVDS1047PWR	3-V LVDS Quad CMOS Differential Line Driver, PW0016A (TSSOP-16)	U2	1

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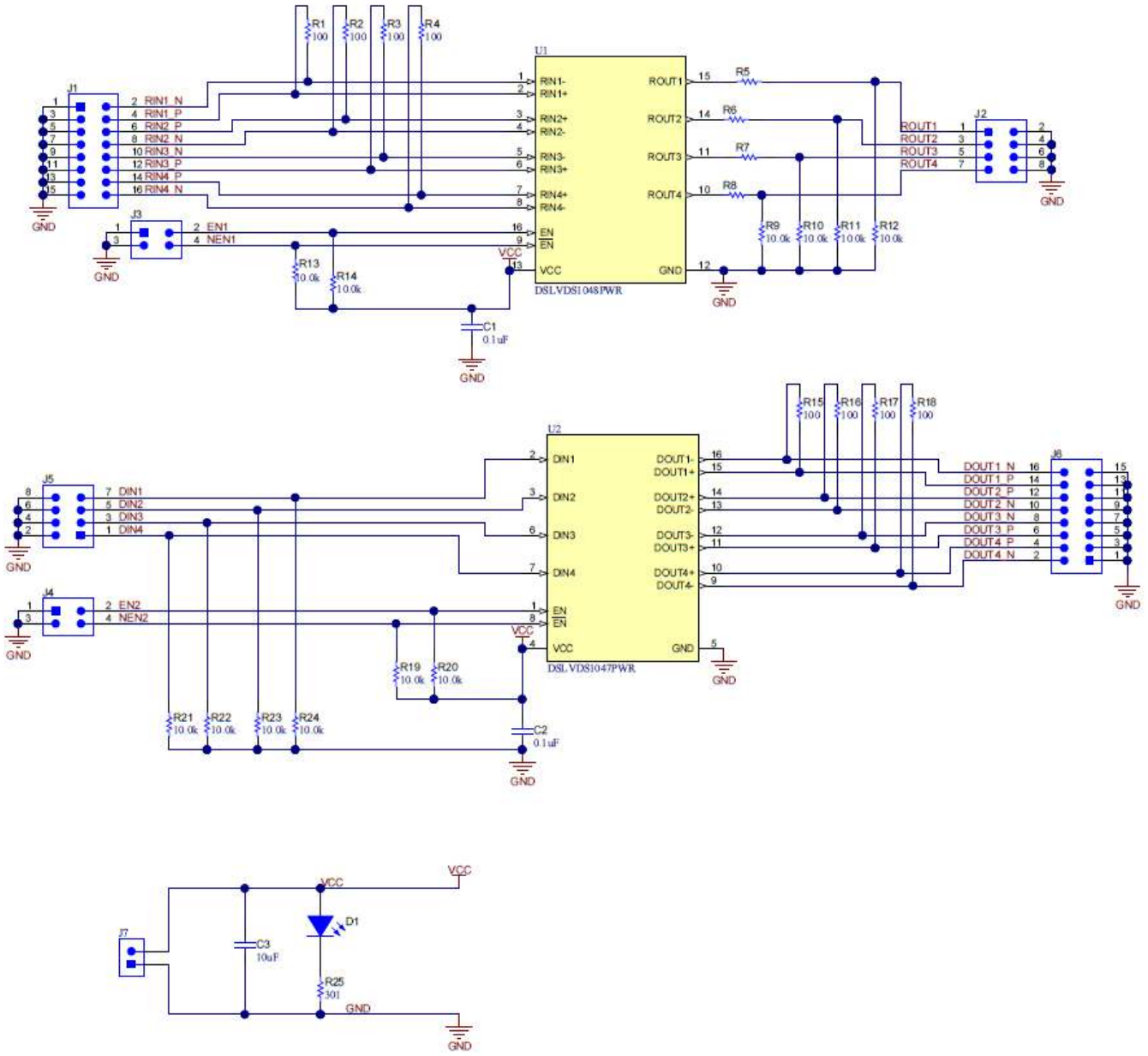
6 Schematic



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7 EVM Layout

Figure 9 and Figure 10 show the DSLVDS1047-1048EVM layout. The DSLVDS1047 and DSLVDS1048 inputs and outputs can be accessed via header pins.

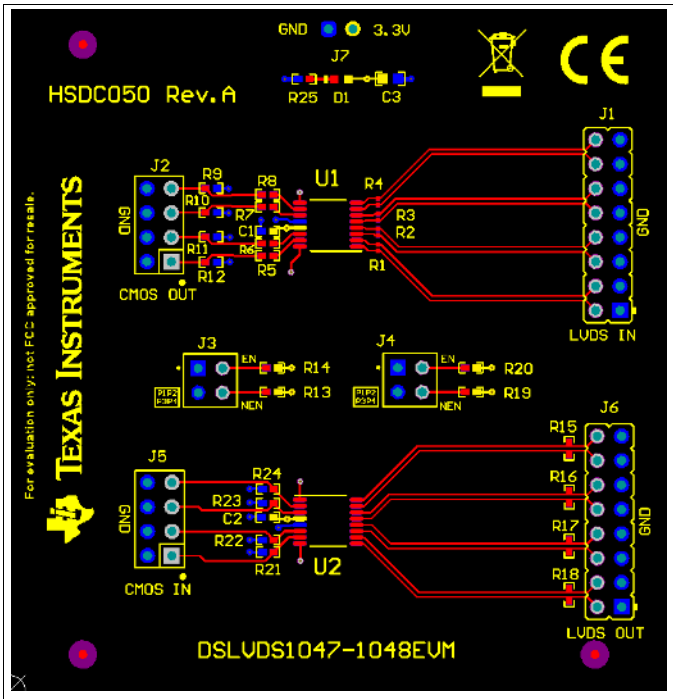

Figure 9. DSLVDS1047-1048EVM Top Layer

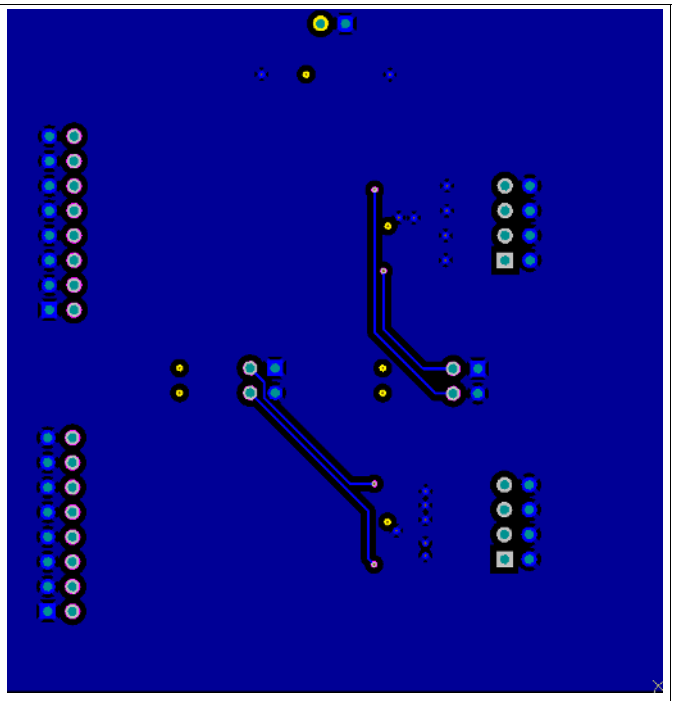

Figure 10. DSLVDS1047-1048EVM Bottom Layer

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