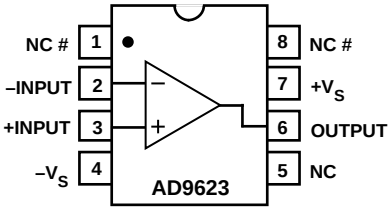
Wideband Voltage Feedback Amplifier

AD9623*

FEATURES
270 MHz Small Signal Bandwidth
190 MHz Large Signal BW (4 V p-p)
High Slew Rate: 2100 V/μs
Low Distortion: –64 dB @ 20 MHz
Fast Settling: 15 ns to 0.01%
2.6 nV/√Hz Spectral Noise Density
±3 V Supply Operation

APPLICATIONS
ADC Input Driver
Differential Amplifiers
IF/RF Amplifiers
Pulse Amplifiers
Professional Video
DAC Current-to-Voltage
Baseband and Video Communications
Active Filters/Integrators/Log Amps

CONNECTION DIAGRAM



 # OPTIONAL CAPACITOR CB CONNECTED HERE DECREASES SETTLING TIME (SEE TEXT).

GENERAL DESCRIPTION

The AD9623 is one of a family of very high speed and wide bandwidth amplifiers utilizing a voltage feedback architecture. These amplifiers define a new level of performance for voltage feedback amplifiers, especially in the categories of large signal bandwidth, slew rate, settling, low distortion, and low noise.

Proprietary design architectures have resulted in an amplifier family that combines the most attractive attributes of both current feedback and voltage feedback amplifiers. The AD9623 exhibits extraordinarily accurate and fast pulse response characteristics (8 ns settling to 0.1%) as well as extremely wide small and large signal bandwidth previously found only in current feedback amplifiers. When combined with balanced high impedance inputs and low input noise current more common to voltage feedback architectures, the AD9623 offers performance not previously available in a monolithic operational amplifier.

***Protected by U.S. Patent 5,150,074 and others pending.**

Other members of the AD962X amplifier family are the AD9621 (G = +1), AD9622 (G = +2), and the AD9624 (G = +6). A separate data sheet is available from Analog Devices for each model. Each generic device has been designed for a different minimum stable gain setting, allowing users flexibility in optimizing system performance. Dynamic performance specifications such as slew rate, settling time, and distortion vary from model to model. The table below summarizes key performance attributes for the AD962X family and can be used as a selection guide.

The AD9623 is offered in industrial and military temperature ranges. Industrial versions are available in plastic DIP, SOIC, and cerdip; MIL versions are packaged in cerdips.

PRODUCT HIGHLIGHTS

1. Wide Large Signal Bandwidth
2. High Slew Rate
3. Fast Settling
4. Low Distortion
5. Output Short-Circuit Protected
6. Low Intermodulation Distortion of High Frequencies

Parameter	AD9621	AD9622	AD9623	AD9624	Units
Minimum Stable Gain	+1	+2	+4	+6	V/V
Harmonic Distortion (20 MHz)	–52	–66	–64	–66	dB
Large Signal Bandwidth (4 V p-p)	130	160	190	200	MHz
SSBW (0.5 V p-p)	350	220	270	300	MHz
Slew Rate	1200	1500	2100	2200	V/μs
Rise/Fall Time (0.5 V Step)	2.4	1.7	1.6	1.5	ns
Settling Time (to 0.1%/0.01%)	7/11	8/14	8/14	8/14	ns
Input Noise (0.1 MHz – 200 MHz)	80	49	36	32	μV rms

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD9623–SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS ($\pm V_S$ = ±5 V, R_{LOAD} = 100 Ω; A_V = +4; R_F = 270 Ω, unless otherwise noted)

Parameter	Conditions	Temp	Test Level	AD9623AN/AQ/AR Min	AD9623AN/AQ/AR Typ	AD9623AN/AQ/AR Max	AD9623SQ Min	AD9623SQ Typ	AD9623SQ Max	Units
DC SPECIFICATIONS[1]										
Input Offset Voltage		+25°C	I	–8	±2	+8	–8	±2	+8	mV
		Full	VI	–10		+10	–10		+10	mV
Input Bias Current		+25°C	I		6	12		6	12	µA
		Full	VI			16			16	µA
Bias Current TC		Full	V		30			30		nA/°C
Input Offset Current		+25°C	I	–2	±0.3	+2	–2	±0.3	+2	µA
		Full	VI	–3		+3	–3		+3	µA
Offset Current TC		Full	V		2.0			2.0		nA/°C
Input Resistance		+25°C	V		600			600		kΩ
Input Capacitance		+25°C	V		1.2			1.2		pF
Common-Mode Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Common-Mode Rejection Ratio	ΔV_{CM} = 1 V	+25°C	I	52	63		52	63		dB
Open-Loop Gain	V_{OUT} = ±2 V p-p	+25°C	V		69			69		dB
Output Voltage Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Output Current		Full	VI	60	70		60	70		mA
Output Resistance		+25°C	V		0.3			0.3		Ω
FREQUENCY DOMAIN										
Bandwidth (–3 dB)										
Small Signal	V_{OUT} = 0.4 V p-p	Full	II	190	270		190	270		MHz
Large Signal	V_{OUT} = 4 V p-p	+25°C	V		190			190		MHz
Amplitude of Peaking	Full Spectrum	Full	II		0.1	1.2		0.1	1.2	dB
Amplitude of Roll-off	DC to 100 MHz	Full	II		0	0.7		0	0.7	dB
Phase Nonlinearity	0.3 to 100 MHz	+25°C	V		1.0			1.0		Degree
2nd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		–64	–56		–64	–56	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		–72	–65		–72	–65	dBc
Common-Mode Rejection Ratio	@ 20 MHz	+25°C	V		+21			+21		dB
Spectral Input Noise Voltage	1 to 200 MHz	+25°C	V		2.6			2.6		nV/√Hz
Spectral Input Noise Current	1 to 200 MHz	+25°C	V		2.5			2.5		pA/√Hz
Average Equivalent Integrated Input Noise Voltage	0.1 to 200 MHz	+25°C	V		36			36		µV rms
TIME DOMAIN										
Slew Rate	V_{OUT} = 5 V Step	Full	IV	1500	2100		1500	2100		V/µs
Rise/Fall Time	V_{OUT} = 0.5 V Step	+25°C	V		1.6			1.6		ns
	V_{OUT} = 5 V Step	Full	VI		2.4	3.1		2.4	3.1	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV		3	15		3	15	%
Settling Time										
To 0.1%	V_{OUT} = 2 V Step	+25°C	V		8			8		ns
To 0.01%	V_{OUT} = 2 V Step	Full	IV		15	20		15	20	ns
To 0.1%[2]	V_{OUT} = 4 V Step	+25°C	V		9			9		ns
To 0.01%[2]	V_{OUT} = 4 V Step	+25°C	V		17			17		ns
Overdrive Recovery	2× to ±2 mV	+25°C	V		150			150		ns
Differential Gain (4.3 MHz)	R_L = 150 Ω	+25°C	V		0.01			0.01		%
Differential Phase (4.3 MHz)	R_L = 150 Ω	+25°C	V		<0.01			<0.01		Degree
POWER SUPPLY REQUIREMENTS[1]										
Supply Voltage ($\pm V_S$)		Full	IV	3.0	5.0	5.5	3.0	5.0	5.5	V
Quiescent Current										
$+I_S$	$+V_S$ = +5 V	Full	VI		23	29		23	29	mA
$-I_S$	$-V_S$ = –5 V	Full	VI		23	29		23	29	mA
Power Supply Rejection Ratio	ΔV_S = 1 V	+25°C	I	60	71		60	71		dB

NOTES

[1]Measured at A_V = 21.

[2]Measured with a 0.001 µF C_B capacitor connected across Pins 1 and 8.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±6 V
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 6 V
Continuous Output Current[2] . . . . . 90 mA
Operating Temperature Ranges
  AN, AQ, AR . . . . . –40°C to +85°C
  SQ . . . . . –55°C to +125°C
Storage Temperature
  Ceramic . . . . . –65°C to +150°C
  Plastic . . . . . –65°C to +125°C
Junction Temperature
  Ceramic[3] . . . . . +175°C
  Plastic[3] . . . . . +150°C
Lead Soldering Temperature (1 minute)[4] . . . . . +220°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected; for maximum reliability, 90 mA continuous current should not be exceeded.
[3]Typical thermal impedances (part soldered onto board; no air flow):
  Ceramic DIP: θ_{JA} = 100°C/W; θ_{JC} = 30°C/W
  Plastic SOIC: θ_{JA} = 125°C/W; θ_{JC} = 45°C/W
  Plastic DIP: θ_{JA} = 90°C/W; θ_{JC} = 45°C/W
[4]Temperature shown is for surface mount devices, mounted by vapor phase soldering. Throughhole devices (ceramic and plastic DIPs) can be soldered at +300°C for 10 seconds.

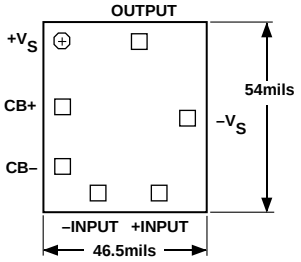
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9623AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD9623AQ	–40°C to +85°C	8-Pin Cerdip	Q-8
AD9623AR	–40°C to +85°C	8-Pin SOIC	R-8
AD9623SQ	–55°C to +125°C	8-Pin Cerdip	Q-8

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing of "A" grade devices done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



Chip Layout

THEORY OF OPERATION

The AD9623 is a wide bandwidth voltage feedback amplifier that is guaranteed for minimum gain stability of +4. Since its open-loop frequency response follows the conventional 6 dB/octave roll-off, its gain bandwidth product is basically constant. Increasing its closed-loop gain results in a corresponding decrease in small signal bandwidth. The AD9623 typically maintains a 60 degree unity loop gain phase margin. This high margin minimizes the effects of signal and noise peaking.

Feedback Resistor Choice

At minimum stable gain (+4), the AD9623 provides optimum dynamic performance with $R_F \cong 390\ \Omega$. When using this value and following the high speed layout guidelines, a shunt capacitor (C_F) should not be required. This value for R_F provides the best combination of wide bandwidth, low peaking, and distortion.

However, if improved gain flatness is desired, a shunt capacitor (C_F) will provide extra phase margin. This reduces both overshoot and peaking with only a slight reduction of bandwidth. See Figure 1.

As an example, if the amplifier exhibits (worst case) peaking of 1 dB with $R_G \| R_F = 98\ \Omega$ ($A_V = 4$), then using an effective C_F of ≈0.5–1 pF across R_F will reduce this peaking to 0 dB. In addition, overshoot, noise, and settling time (0.01%) will also improve. This comes at the expense of slightly decreased closed-loop bandwidth due to the $R_F \times C_F$ time constant created.

If total input capacitance greatly exceeds 3 pF (due to source drive or long input traces to the amplifier), then added shunt capacitance (C_F) will be necessary to maintain stability for minimum gain.

Likewise, if larger R_G/R_F minimum-gain setting resistors are used, C_F will be necessary. As a rule of thumb, if the product of $R_F \| R_G \times C_I \le 300 \times 10^{-12}$ seconds, then C_F is not required (for maximum bandwidth at minimum gain) and the amplifier's phase margin will maintain about 60°.

For $R_F \| R_G > 150\ \Omega$, use a C_F equal to $C_I \times R_G/R_F$. For C_I (total) @ 2 pF, requires C_F to be 0.5 pF. This can be achieved by two 1 pF capacitors in series, or by using a resistor divider network at the amplifier's output in conjunction with a larger capacitor. Increasing C_F much beyond these guidelines will also cause amplifier instability.

Pulse Response

Unlike a traditional voltage feedback amplifier in which slew speed is usually dictated by its front end dc quiescent current and gain bandwidth product, the AD9623 provides "on demand" transconductance current that increases proportionally to the input "step" signal amplitude. This results in slew speeds (2100 V/μs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (2.5 pA/$\sqrt{\text{Hz}}$), gives the AD9623 the best attributes of both voltage and current feedback amplifiers.

Bootstrap Capacitor (C_B)

In most applications, the C_B capacitor should not be required. Under certain conditions, it can be used to further enhance settling time performance.

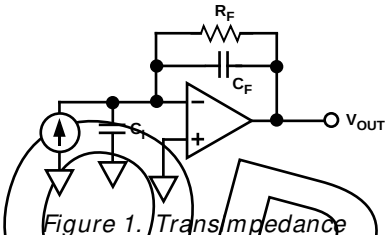


Figure 1. Transimpedance Configuration

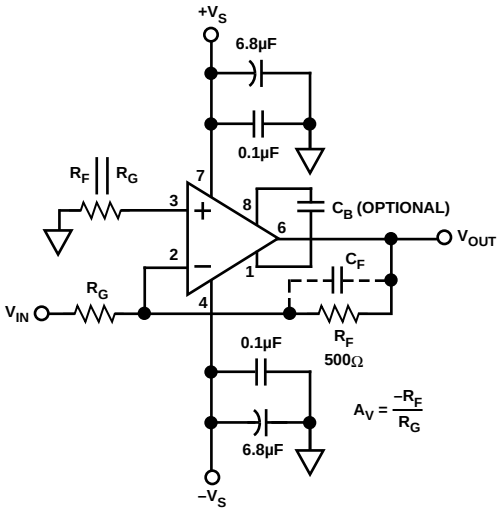


Figure 2. Inverting Gain Connection Diagram

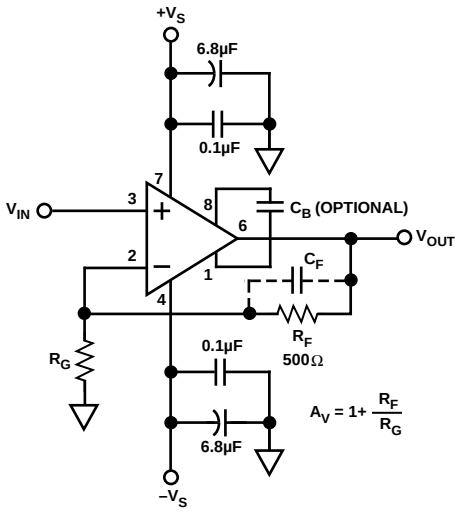


Figure 3. Noninverting Gain Connection Diagram

The C_B capacitor (0.001 µF) connects to the internal high impedance nodes of the amplifier. Using this capacitor will reduce the large signal (4 V) step output settling time by 3 ns to 5 ns for 0.05% or greater accuracy. For settling accuracy less than 0.05% or for smaller step sizes, its effect will be less apparent.

Under heavy slew conditions, this capacitor forces the internal signal (initial step) amplitude to be controlled by the "on" (slewed) transistor, preventing its complement from completely turning off. This allows for faster settling time of these (internal) nodes and thus, the output also.

In the frequency domain, total (high frequency) distortion will be approximately the same with or without C_B. Typically, the 3rd harmonic will be greater than the 2nd without C_B. This will be reversed with C_B in place.

APPLICATIONS

The AD9623 is a voltage feedback amplifier and is well suited for such applications as active filters, and log amplifiers. The device's wide bandwidth (270 MHz), phase margin (60°), low noise current (2.6 pA /$\sqrt{\text{Hz}}$), and slew rate (2100 V/µs) give higher performance capabilities to these applications over previous voltage feedback designs.

Its settling time of 15 ns to 0.01% and 8 ns to 0.1%, and its low harmonic distortion make it a good for choice for ADC signal amplification. With superb linearity at relatively high signal frequencies, it is an ideal driver for ADCs up to 14 bits.

Layout Considerations

As with all wide bandwidth components, printed circuit layout is critical to obtain best dynamic performance with the AD9623. The ground plane in the area of the amplifier and its associated components should cover as much of the component side of the board as possible (or first interior layer of a multilayer surface mount board).

The ground plane should be removed in the area of the inputs and R_F and R_G to minimize stray capacitance at the input. The same precaution should be used for C_B, if used. Each power supply trace should be decoupled close to the package with a 0.1 µF ceramic capacitor, plus a 6.8 µF tantalum nearby.

All lead lengths for input, output, and feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors and/or carbon resistors.

Microstrip techniques should be used for lead lengths in excess of one inch. Sockets should be avoided if at all possible because of their high series inductance. If sockets are necessary, individual pin sockets such as AMP p/n 6-330808-3 should be used. These contribute far less stray reactance than molded socket assemblies.

An evaluation board is available from Analog Devices for a nominal charge.

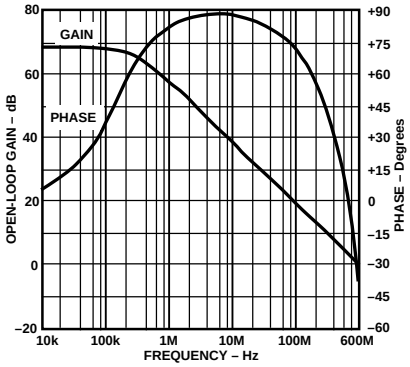


Figure 4. Open-Loop Gain and Phase

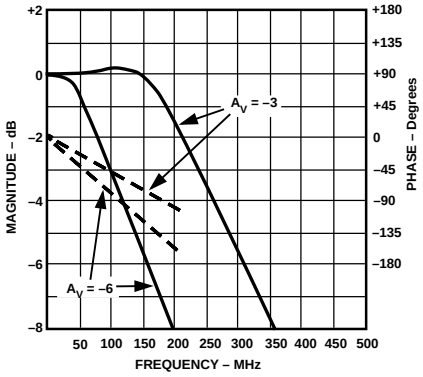


Figure 5. Inverting Frequency Response

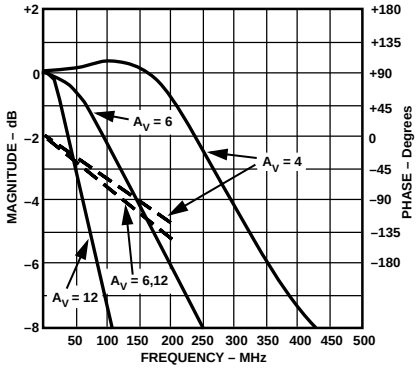


Figure 6. Noninverting Frequency Response

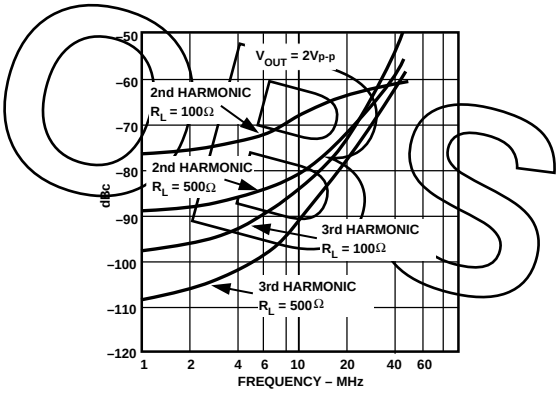


Figure 7. Harmonic Distortion vs. Frequency

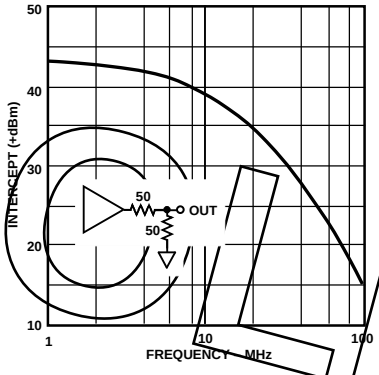


Figure 8. Third Order Intercept

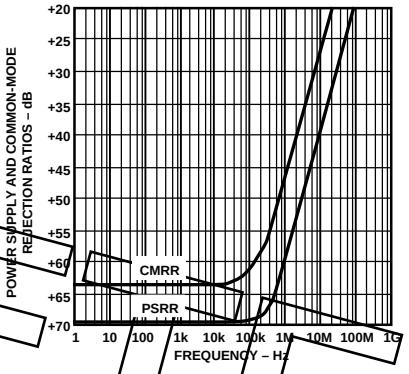


Figure 9. CMRR and PSRR vs. Frequency

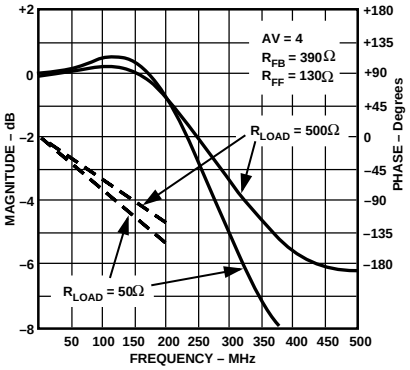


Figure 10. Frequency Response vs. R_{LOAD}

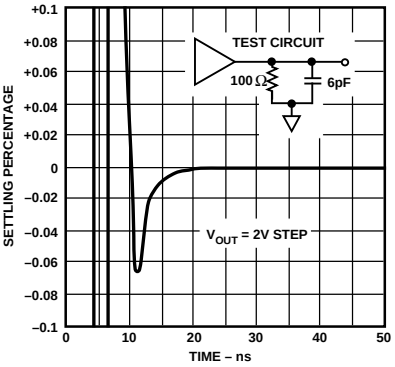


Figure 11. Short-Term Settling Time

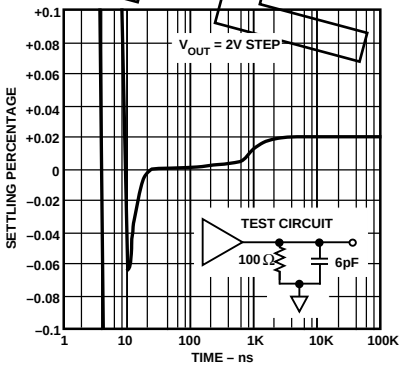


Figure 12. Long-Term Settling Time

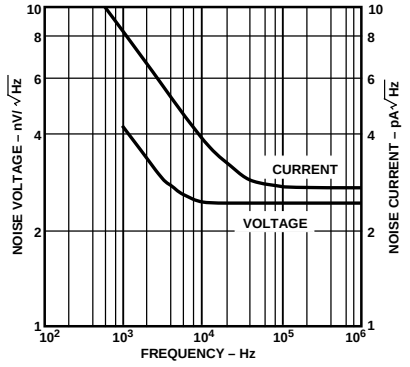


Figure 13. Input Spectral Noise Density

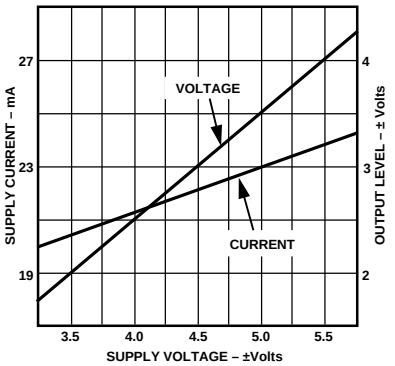


Figure 14. Output Level and Supply Current vs. Supply Voltage

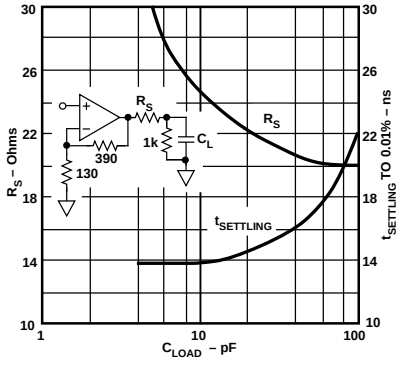


Figure 15. Settling Time vs. Capacitive Load

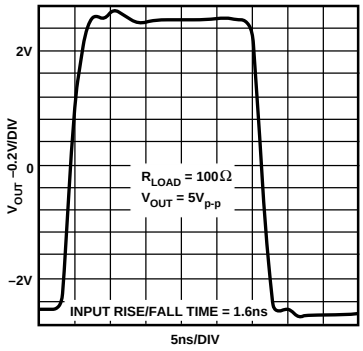


Figure 16. Large Signal Pulse Response

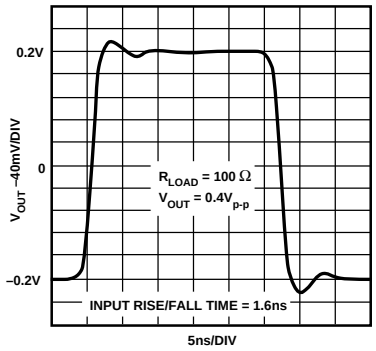


Figure 17. Small Signal Pulse Response

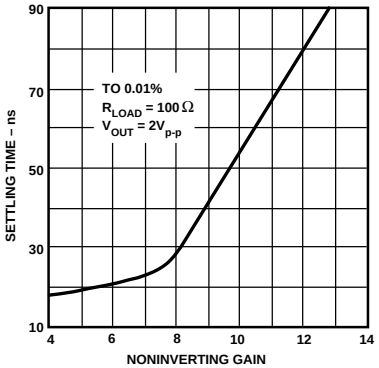


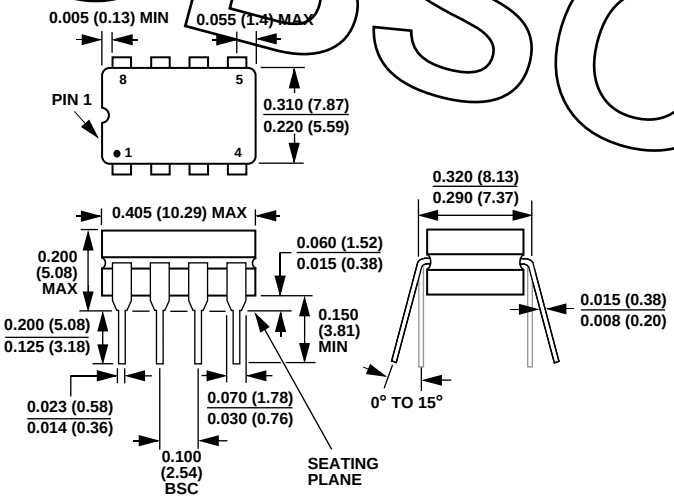
Figure 18. Settling Time vs. Noninverting Gain

C1723–24–10/92

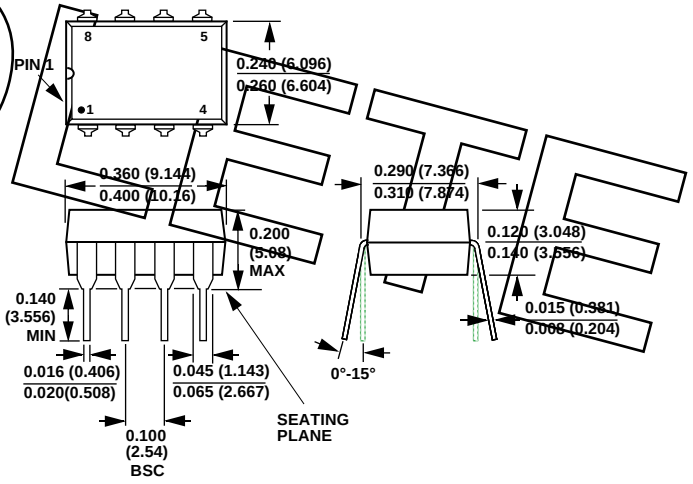
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

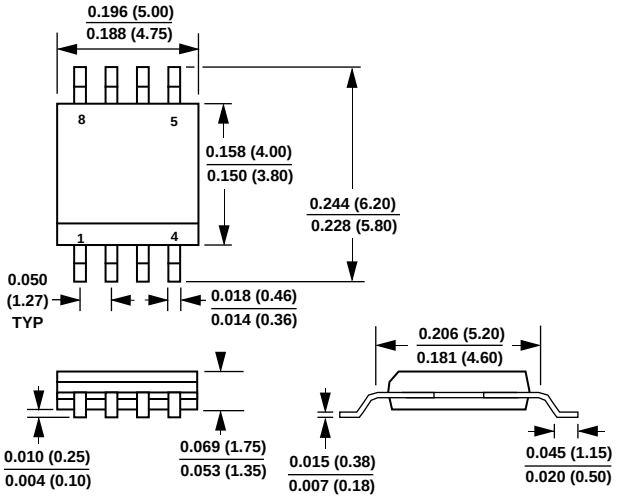
Cerdip (Suffix Q)



Plastic DIP (Suffix N)



Plastic SOIC (Suffix R)



PRINTED IN U.S.A.