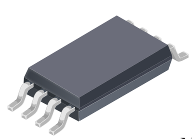
A1343

High-Precision, Highly Programmable Linear Hall-Effect Sensor IC with EEPROM, Output Protocols SENT and PWM, and Advanced Output Linearization

FEATURES AND BENEFITS

- Advanced 32-segment output linearization functionality enables high output accuracy and linearity in the presence of nonlinear input magnetic fields
- Selectable digital SENT (Single Edge Nibble Transmission) and PWM (Pulse-Width Modulation) output
- SENT output supports two modes: SAEJ2716 JAN2010 and Allegro Proprietary with Enhanced Programmable Features
- Customer-programmable magnetic range selection and offset, sensitivity, bandwidth, output clamps, 1st- and 2nd-order temperature compensation
- Simultaneous programming of all parameters for accurate and efficient system optimization with onboard EEPROM capable of supporting up to 100 read/write cycles
- Initial sensitivity temperature coefficient and magnetic offset drift preset at Allegro, for maximum device accuracy without requiring customer temperature testing
- Temperature-stable, mechanical stress immune, and extremely low noise device output via proprietary four-phase chopper stabilization and differential circuit design techniques
- Wide ambient temperature range: –40°C to 150°C
- Operates with 4.5 to 5.5 V supply voltage

PACKAGE: 8-PIN TSSOP (SUFFIX LE)



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DESCRIPTION

The A1343 device is a high-precision, programmable Hall-effect linear sensor integrated circuit (IC) with an open-drain output, configurable as pulse-width modulated (PWM) or single edge nibble transmission (SENT), for both automotive and nonautomotive applications. The signal path of the A1343 provides flexibility through external programming that allows the generation of an accurate and customized output voltage from an input magnetic signal. The A1343 provides 12 bits of output resolution, and supports a maximum bandwidth of 3 kHz.

The BiCMOS, monolithic integrated circuit incorporates a Hall sensor element, precision temperature-compensating circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element, a small-signal high-gain amplifier, proprietary dynamic offset cancellation circuits, and advanced output linearization circuitry.

With on-board EEPROM and advanced signal processing functions, the A1343 provides an unmatched level of customer reprogrammable options for characteristics such as gain and offset, bandwidth, output clamps, and magnetic range selection. In addition, the device supports separate hot and cold, 1st- and 2nd-order temperature compensation.

A key feature of the A1343 is its ability to produce a highly linear device output for nonlinear input magnetic fields. To achieve this, the device divides the output into 32 equal segments and applies a unique linearization coefficient factor to each segment. Linearization coefficients are stored in a lookup table in EEPROM.

The A1343 is available in a lead (Pb) free 8-pin TSSOP package (LE suffix), with 100% matte-tin leadframe plating.

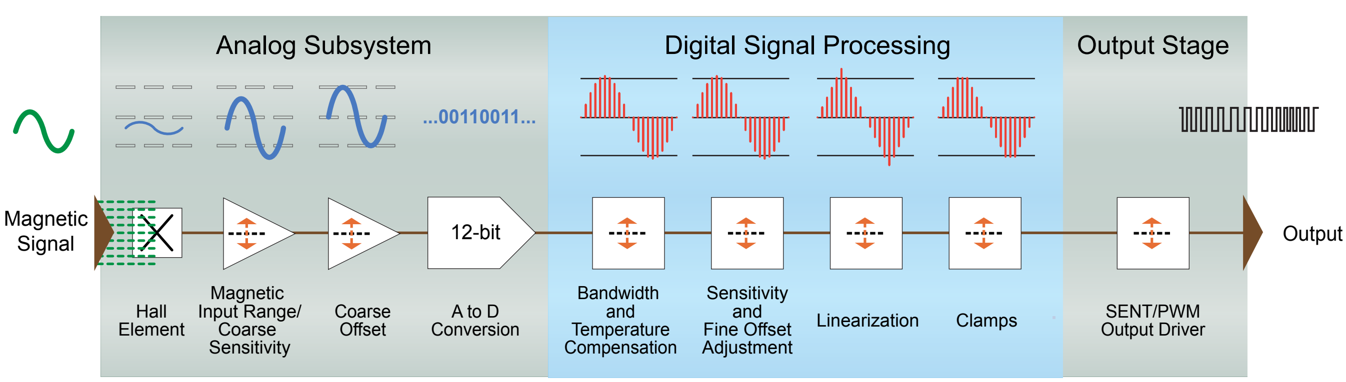

Figure 1: A1343 Signal Processing Path.
Functions with programmable parameters indicated by double-headed arrows.

Selection Guide

Part Number	Packing*
A1343LLETR-T	4000 pieces per 13-in. reel

*Contact Allegro™ for additional packing options.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		30	V
Reverse Supply Voltage	V_{RCC}		–20	V
Forward Supply Current	I_{CC}		30	mA
Reverse Supply Current	I_{RCC}		–30	mA
Forward Output Voltage (OUT Pin)	V_{OUT}		30	V
Reverse Output Voltage (OUT Pin)	V_{ROUT}		–0.5	V
Forward Output Sink Current (OUT Pin)	I_{SINK}	Current limited	60	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 165	ºC

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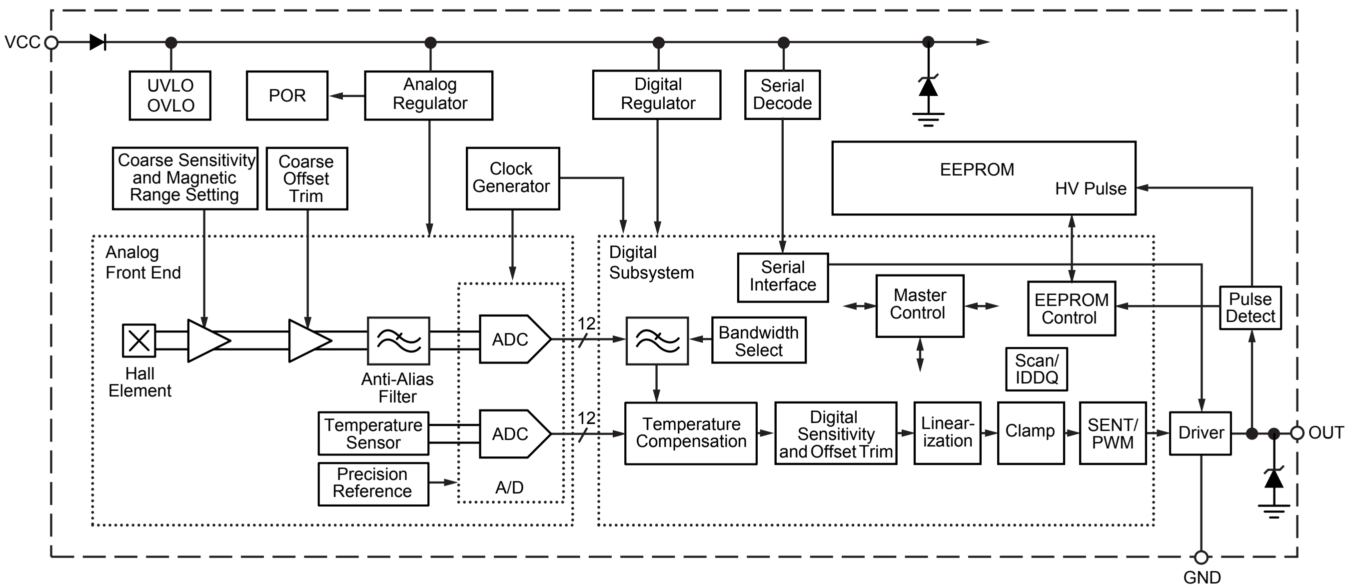
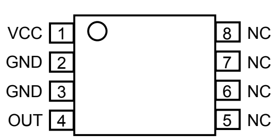
Functional Block Diagram



Pinout Diagram



Terminal List Table

Number	Name	Function
1	VCC	Input power supply
2	GND	Device ground
3	GND	Device ground
4	OUT	Output pin
5, 6, 7, 8	NC	Not connected; Recommend connecting pin to ground for application use.

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ELECTRICAL CHARACTERISTICS: Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
GENERAL ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	LVD_DIS = 1	4.5	–	5.5	V
Supply Current	I_{CC}		5	–	10	mA
Reverse Supply Current	I_{RCC}	V_{RCC} = 20 V	–	–	–3	mA
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	I_{CC} = I_{CC}(max) + 3 mA, T_A = 25°C	30	–	–	V
Hall Chopping Frequency	f_C	T_A = 25°C	–	128	–	kHz
Low Voltage Detection Threshold	$V_{CC(LVD)LOW}$	LVD_DIS = 0	4.25	4.4	4.55	V
	$V_{CC(LVD)HIGH}$	LVD_DIS = 0	4.35	4.5	4.65	V
Power-On Reset	POR_{LOW}		3.5	3.7	4.1	V
	POR_{HIGH}		3.6	3.8	4.15	V
Overvoltage Lockout Threshold	$V_{CC(OV)LOW}$	OVLO_LO = 1, T_A = 25°C	5.6	–	7.6	V
		OVLO_LO = 0, T_A = 25°C	18	–	20	V
	$V_{CC(OV)HIGH}$	OVLO_LO = 1, T_A = 25°C	5.8	–	7.9	V
		OVLO_LO = 0, T_A = 25°C	18.3	–	20.3	V
SENT Message Duration	t_{SENT}	Tick time = 3 µs	–	1	–	ms
Output PWM Period [2]	V_{PERIOD}	PWM_MODE = 1	–15	–	15	%
Minimum Programmable SENT Message Duration	$t_{SENTMIN}$	Tick time = 0.25 µs, 3 data nibbles of information, nibble length = 27 ticks	–	41	–	µs
OUTPUT ELECTRICAL CHARACTERISTICS						
Output Leakage Current	$I_{OUT(LOW)}$	Output FET off	–	–	100	µA
Output Saturation Voltage [3]	V_{SAT}	I_{SINK} = 4.7 mA	–	0.3	0.45	V
Output Current Limit	I_{LIMIT}	Output FET on, T_A = 25°C	20	35	60	mA
Output Zener Clamp Voltage	V_{ZOUT}	T_A = 25°C	30	–	–	V
Output Load Capacitance [4,5]	C_{LOAD}	OUT to GND	–	–	10	nF
Power-On Time [4,6]	t_{PO}	BW parameter = 1	–	0.5	–	ms
		BW parameter = 0,2	–	0.8	–	ms
		BW parameter = 3	–	2	–	ms
		BW parameter = 4	–	3	–	ms
		BW parameter = 5	–	6	–	ms
Signal Path Propagation Delay [4,6]	t_{SDLY}	BW parameter = 1	–	0.35	–	ms
		BW parameter = 0,2	–	0.7	–	ms
		BW parameter = 3	–	1.4	–	ms
		BW parameter = 4	–	2.8	–	ms
		BW parameter = 5	–	5.6	–	ms

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ELECTRICAL CHARACTERISTICS (continued): Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
OUTPUT ELECTRICAL CHARACTERISTICS (continued)						
Full Scale Output Range [7]	FSO	PWM_MODE = 1 (PWM mode), CLAMP_HIGH = CLAMP_LOW = 0 (PWM duty cycle)	–	–	96	%D
		PWM_MODE = 0 (SENT mode)	–	–	4096	LSB

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] The PWM period is ±15% of the setting determined by the register FPWM address. See EEPROM Customer-Programmable Parameter Reference for more information.
[3] Output pin can be loaded with a 1.2 kΩ pull-up resistor without V_{SAT} rising above 0.5 V.
[4] Determined from design and lab characterization on a limited number of samples; not tested in production.
[5] Clarity of a Read Acknowledge message from the device to the controller will be affected by the amount of capacitance and wire inductance on the device output. In cases of complex loads with higher capacitance, it is recommended to slow down the communication speed, and to lower the receiver threshold for reading the digital Manchester signal.
[6] See Definitions of Terms section.
[7] SENT mode Full Scale Output Range is 12 bit, 0 to 4095.

MAGNETIC CHARACTERISTICS: Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1,2]
INITIAL DEVICE VALUES (Before Customer Programming), V_{CC} = 5 V, T_A = 25°C						
Initial Magnetic Input Signal Range	B_{INinit}	SENS_COARSE = 3	–	±250	–	G
Initial Magnetic Signal Offset	$B_{INOFFSET}$	SIG_COARSE = 3	–	0	–	%FSI
Initial Sensitivity	$Sens_{init}$	SENS_COARSE = 3, SENS_MULT = 0	–	8.19	–	LSB/G
Initial Quiescent Output	$QOUT_{init}$	B_{IN} = 0 G	–	50	–	%FSO
Initial Output Clamp	$OUT_{CLP(H)init}$	PWM_MODE = 0 (SENT mode), CLAMP_HIGH = 0	–	4095	–	LSB
	$OUT_{CLP(L)init}$	PWM_MODE = 0 (SENT mode), CLAMP_LOW = 0	–	0	–	LSB
Initial SENT Output Configuration	$SENT_{CFG(tick)init}$	PWM_MODE = 0, SENT_TICK = 2	0.4	0.5	0.6	µs
	$SENT_{CFG(fixed)init}$	PWM_MODE = 0, SENT_FIXED = 1	–	4	–	tick
	$SENT_{CFG(update)init}$	PWM_MODE = 0, SENT_UPDATE = 3	–	3	–	–
	$SENT_{CFG(data)init}$	PWM_MODE = 0, SENT_DATA = 3	–	3	–	nibble
Initial Sensitivity Drift Over Temperature [3,4]	$\Delta Sens_{init}$	T_A = –40°C to 25°C	–	<±0.03	–	%/°C
		T_A = 25°C to 150°C	–	<±0.02	–	%/°C
Initial Offset (QVO) Drift Over Temperature [4]	$\Delta OUT_{(Q)init}$	T_A = –40°C to 150°C	–	<±0.005	–	%/°C

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] *FSO* means Full Scale Output. See Definitions of Terms section.
[3] Does not include drift over lifetime and package hysteresis. Sensitivity can drift 3% typical worse case over the life of the product. Package hysteresis can result in Sensitivity drift of 2% typical worse case.
[4] Offset and Sensitivity drifts with temperature changes may vary with adjustment to the initial Magnetic Input Signal Range and Magnetic Offset. Contact Allegro for more information on application requirements with alternative SENS_COARSE and SIG_OFFSET settings.

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PROGRAMMABLE CHARACTERISTICS: Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
MAGNETIC INPUT SIGNAL RANGE						
Magnetic Input Signal Range Programming Bits		SENS_COARSE	–	4	–	bit
Magnetic Input Signal Range Programming Values	RANGE	T_A = 25°C, for programming values, see SENS_COARSE in EEPROM Structure section	±100	–	±2250	G
MAGNETIC OFFSET COMPENSATION						
Magnetic Offset Programming Bits		SIG_OFFSET	–	5	–	bit
Typical Magnetic Offset Programming Range[2]	SIG_OFFSET	T_A = 25°C	–100	–	+93.75	%FSI
Magnetic Offset Programming Step Size[2]	$Step_{SIG\_OFFSET}$	T_A = 25°C	5.62	6.25	6.875	%FSI
INTERNAL BANDWIDTH PROGRAMMING						
Bandwidth Programming Bits		BW	–	3	–	bit
Bandwidth Programming Range	BW	T_A = 25°C; for programming values, see BW in EEPROM Structure section	188	–	3000	Hz
Bandwidth Post-Programming Tolerance	ΔBW	T_A = 25°C, measured as a percentage of BW	–	±5	–	%
FINE QUIESCENT OUTPUT						
Fine Quiescent Output Programming Bits		QOUT_FINE	–	12	–	bit
Fine Quiescent Output Programming Range	QOUT_FINE	T_A = 25°C, B_{IN} = 0 G	–50	–	49.98	%FSO
Fine Quiescent Output Programming Step Size	$Step_{QOUT\_FINE}$	T_A = 25°C, B_{IN} = 0 G	–	0.0244	–	%FSO
OUTPUT SENSITIVITY						
Output Sensitivity	SENS_OUT	T_A = 25°C	0.025	–	0.5	%FSO/G
Sensitivity Multiplier Programming Bits		SENS_MULT	–	12	–	bit
Sensitivity Multipler Programming Range	SENS_MULT	T_A = 25°C	0	–	2	–
Sensitivity Multiplier Programming Step Size	$Step_{SENS\_MULT}$	T_A = 25°C	–	0.00049	–	–
LINEARIZATION						
Linearization Positions		T_A = 25°C	–	33	–	data sampling point
Linearization Position Coefficient Bits	LINPOS_COEFF	LIN_x, programmed with output fitting method	–	12	–	bit
Output Polarity Bit		OUTPUT_INVERT	–	1	–	bit
Input Polarity Bit		LIN_INPUT_INVERT	–	1	–	bit

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PROGRAMMABLE CHARACTERISTICS (continued): Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
TEMPERATURE COMPENSATION (TC) For back-biased devices, values cannot be tested in production						
1st-Order Sensitivity TC Programming Bits		TC1_SENS_CLD	–	8	–	bit
		TC1_SENS_HOT	–	8	–	bit
1st-Order Sensitivity TC Programming Range[3]	TC1_SENS_CLD TC1_SENS_HOT		–98	–	+291	m%/°C
1st-Order Sensitivity TC Programming Step Size[3]	$Step_{TC1SENS}$		–	1.53	–	m%/°C
2nd-Order Sensitivity TC Programming Bits		TC2_SENS_CLD, T_A = 150°C	–	9	–	bit
		TC2_SENS_HOT, T_A = 150°C	–	9	–	bit
2nd-Order Sensitivity TC Programming Range[3]	TC2_SENS_CLD TC2_SENS_HOT		–1.53	–	+1.53	m%/°C^2
2nd-Order Sensitivity TC Programming Step Size[3]	$Step_{TC2SENS}$		–	0.00596	–	m%/°C^2
1st-Order Magnetic Offset TC Programming Bits		TC1_OFFSET	–	8	–	bit
1st-Order Magnetic Offset TC Programming Range[4]	TC1_OFFSET	SENS_COARSE = 3	–0.488	–	+0.484	G/°C
1st-Order Magnetic Offset TC Step Size	$Step_{TC1\_OFFSET}$	SENS_COARSE = 3	–	0.0038	–	G/°C
OUTPUT CLAMPING RANGE						
Clamp Programming Bits		CLAMP_HIGH	–	6	–	bit
		CLAMP_LOW	–	6	–	bit
Output Clamp Programming Range	$OUT_{CLP(H)}$	T_A = 25°C, V_{CC} = 5 V	50.78	–	100	%FSO
	$OUT_{CLP(L)}$	T_A = 25°C, V_{CC} = 5 V	0	–	49.22	%FSO
Clamp Programming Step Size	$Step_{CLP(H)}$	T_A = 25°C	–	0.78	–	%FSO
	$Step_{CLP(L)}$	T_A = 25°C	–	0.78	–	%FSO

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Accuracy (After Customer Programming)						
Linearity Sensitivity Error	Lin_{ERR}		–	<±1	–	%
Symmetry Sensitivity Error	Sym_{ERR}		–	<±1	–	%
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	Variation on final programmed Sensitivity value; measured at T_A = 25°C after temperature cycling	–	< ±2	–	%
Sensitivity Drift Over Lifetime	$\Delta Sens_{LIFE}$	T_A = 25°C, shift after AEC-Q100 grade 0 qualification in testing	–	±3	–	%
SENT Characteristics						
SENT Output Signal	$V_{SENT(L)}$	10 kΩ ≤ R_{pullup} ≤ 50 kΩ	–	–	0.05	V
	$V_{SENT(H)}$	Minimum R_{pullup} = 10 kΩ	0.9 × V_{CC}	–	–	V
		Maximum R_{pullup} = 50 kΩ	0.7 × V_{CC}	–	–	V
SENT Output Trigger Signal	$V_{SENTtrig(L)}$		–	–	1.2	V
	$V_{SENTtrig(H)}$		2.8	–	–	V

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] The unit %FSI = percentage of Full Scale Input. See Definitions of Terms section.
[3] The unit m% = 0.001%; for example, 25 m%/°C = 0.025 %/°C = 2.5×10^{-2} /°C.
[4] Parameter scales with SENS_COARSE. See programming information for more details.

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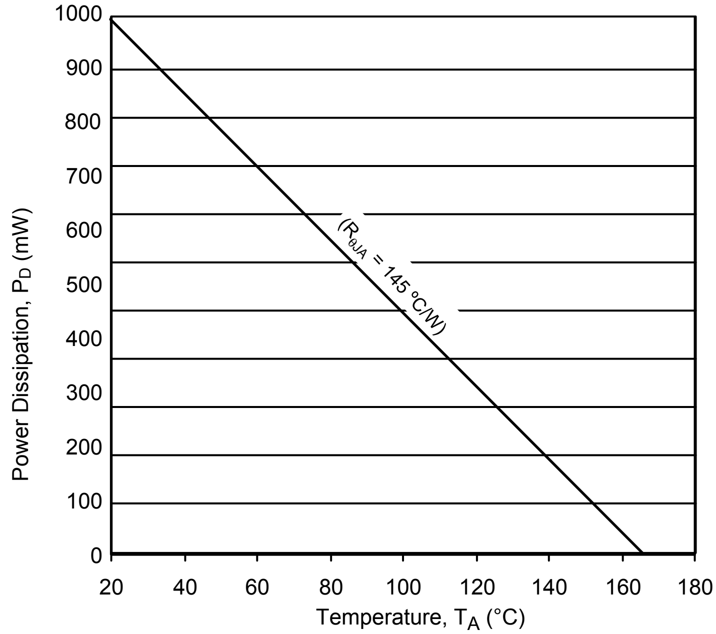
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	145	ºC/W

*Additional thermal information available on the Allegro website

Power Dissipation versus Ambient Temperature



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FUNCTIONAL DESCRIPTION

This section provides descriptions of the operating features and subsystems of the A1343. For more information on specific terms, refer to the Definitions of Terms section. Tables of EEPROM parameter values are provided in the EEPROM Structure section.

Signal Processing Parameter Setting

The A1343 has customer-programmable parameters that allow the user to optimize the signal processing performed by the A1343. Customer-programmable parameters apply to the analog front-end stages and the digital signal processing stages. Programmed settings are stored in on-board EEPROM. The programming communication protocol is described in the Programming Serial Interface section.

The initial analog processing can be customer-programmed to match the application environment in terms of magnetic field range and intensity. This allows optimization of the electrical signal presented to the digital signal processing (DSP) stage. The DSP stage provides customer-programmable sensitivity (gain) and offset adjusting, TC processing, and bandwidth, clamp, and linearization selection.

The output of the IC is a digital voltage signal, proportional to the applied magnetic signal. The format for the output signal is customer-selectable: either pulse-width modulation (PWM) or single edge nibble transmission (SENT) encoding scheme. The Full Scale Output range is proportional to the Full Scale Input range, but is optimized by customer-programmed parameters.

Analog Input Full Scale Range Determination

The Full Scale Input (FSI) range is the segment of the magnetic input signal that is used to generate the DSP input. This range is characterized by amplitude and centerpoint, which are adjustable using programming parameters for magnetic range and magnetic offset. Optimizing these two parameters allows the A1343 to best use the input range of the A-to-D converter and thereby maintain maximum input resolution (12 bits) for the DSP without clipping the magnetic input signal. The analog subsystem applies these two characteristics according to the following formula:

$$Y_{AD}\ (\%FSO) = SENS\_COARSE\ (\%FSO/G) \times B_{IN} + QOUT\_COARSE\ (\%FSO) \quad (1)$$

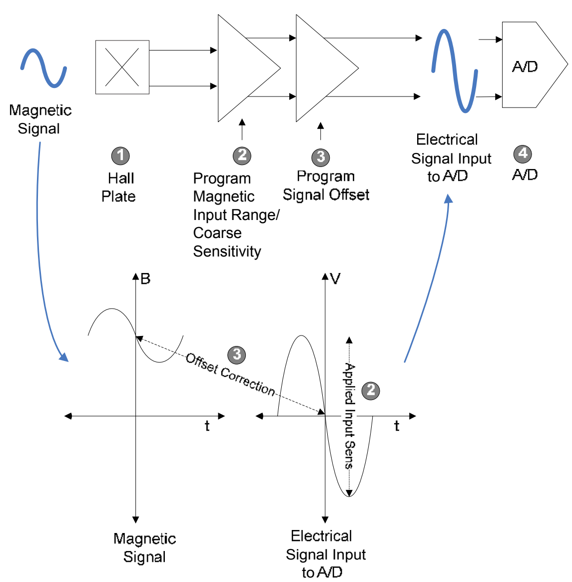

Figure 2: Signal Path for Analog Subsystem

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where:

Y_{AD} is the output signal from the analog subsystem—this signal is input to the analog-to-digital converter (ADC);

SENS_COARSE is the coarse sensitivity (described below);

B_{IN} is the magnetic input signal; and

QOUT_COARSE is the coarse offset applied to the input signal—this value is determined by the initial offset, Q_{OUT}, and the parameter SIG_OFFSET.

Analog Input Range Setting

The Hall element signal voltage, V_{HALL}, is directly proportional to the applied magnetic flux density, B_{IN}. B_{IN} is essentially the impinging magnetic field that is perpendicular to the branded face of the device case. The Magnetic Input Signal, RANGE, is adjusted to best match B_{IN}, (point 2 in Figure 2). The RANGE should be sufficiently large to account for the maximum peak-to-peak value of B_{IN}. Also, it should be sufficiently small to maximize the signal input to the ADC. RANGE is customer-programmable to any of 16 values, from ±100 G (lowest) to ±2250 G (highest) by setting the SENS_COARSE parameter. The default RANGE setting is ±500 G, SENS_COARSE equal to 0. For more details on the SENS_COARSE programming codes, see the EEPROM Customer-Programmable Parameter Reference section.

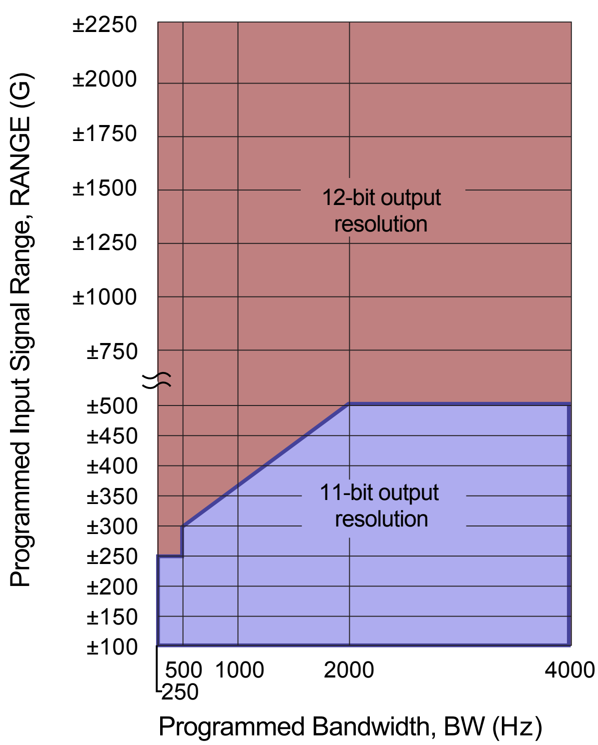

Figure 3: Output Resolution as a Function of Input Range and Bandwidth

The selected RANGE setting determines the coarse Sensitivity and impacts the output resolution. The relationship between the Magnetic Input Signal Range, Bandwidth, and maximum achievable output resolution is displayed in Figure 3.

Analog Magnetic Offset Selection

The magnetic offset parameter, SIG_OFFSET, adjusts the input signal to the center of the A-to-D range. The adjusted value is represented as QOUT_COARSE in equation 1.

The parameter SIG_OFFSET is used to adjust for typical magnetic influences in the application configuration itself (point 3 in Figure 2). It is programmed to any of 32 settings applied as percentages of FSI. These adjust the centerpoint between 100% of FSI more negative than 0 G (toward a more intense north polarity), to 93.75% of FSI more positive than 0 G (toward a more intense south polarity).

Digital Signal Processing

The adjusted input signal is converted to a digital signal for additional processing prior to the output stage. The DSP stage makes available many of the advanced programming features incorporated within the A1343. Some of the advanced programming features within the DSP include: fine Sensitivity adjustment, fine Offset adjustment, 1st- and 2nd-order Sensitivity Temperature Compensation, Offset temperature compensation, linearization, output clamps, and output configuration.

Bandwidth Selection

The 3-dB bandwidth, BW, determines the frequency at which the DSP function imports data from the analog front-end A-to-D converter. It is programmed by setting the BW parameter in EEPROM. The values chosen for BW and RANGE affect the DSP stage output resolution and the Signal Path Propagation Delay, t_{SDLY}. These tradeoffs are represented graphically in Figure 3, and in Table 1.

Table 1: Bandwidth-Related Tradeoffs

Bandwidth Selection [Internal Update Rate] (kHz)	DSP Output Resolution (bit)	Minimum RANGE for Full DSP Output Resolution (G)	Signal Path Propagation Delay, t_{SDLY} (ms)
0.500 [2.0]	11 to 12	±250	2.8
2.000 [8.0]	11 to 12	±500	0.7
4.000 [16.0]	10 to 11	±500	0.35

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Temperature Compensation

The magnetic properties of materials can be affected by changes in temperature, even within the rated ambient operating temperature range, T_A. Any change in the magnetic circuit due to temperature variation causes a proportional change in the device output. The A1343 features integrated temperature compensation (TC) circuitry that can be programmed to compensate for many of these external magnetic variations. TC coefficients can be programmed for Sensitivity and magnetic offset. The effect of temperature is referred to as *drift*.

The A1343 uses the 1st-Order Magnetic Offset TC algorithm to compensate for output offset drift across the ambient temperature range (see Figure 5). The programmable parameter, TC1_OFFSET, is used to adjust the Magnetic Offset TC. It is programmable within the specified range and scales with the SENS_COARSE parameter. The step size of TC1_OFFSET decreases with decreased RANGE and increases with increased RANGE. For an example of 1st-Order Magnetic Offset compensation, refer to the EEPROM Customer-Programmable Parameter Reference section.

In addition to the offset TC compensation, the A1343 also provides a means to compensate for variation of the applied magnetic flux density with temperature. This is accomplished by utilizing 1st- and 2nd-order segmented algorithms to dynamically adjust the sensitivity of the sensor IC. There are two segments that can be programmed: temperatures above 25°C, Hot, and temperatures below 25°C, Cold. See Table 2 and Figure 6 for illustrations of the Sensitivity TC compensation.

The algorithm is flexible in a way such that 1st- and 2nd-order coefficients are applied independently from one another, from hot to cold. This method allows the end user to select either, both, or neither of the coefficients. The 1st-order coefficients are adjusted using the programmable parameters, TC1_SENS_HOT and TC1_SENS_CLD. The 2nd-order coefficients are adjusted using the programmable parameters, TC2_SENS_HOT and TC2_SENS_CLD. The coefficients are applied according to equation 2.

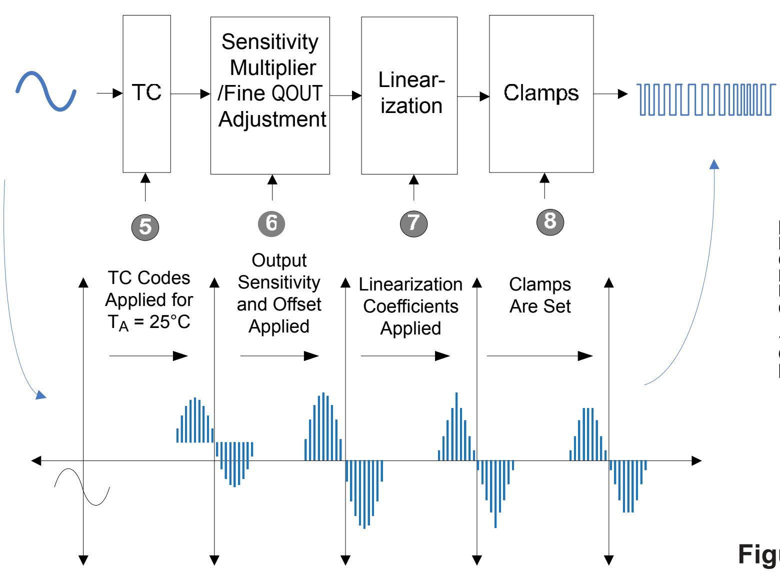

Figure 4: Signal Path for Digital Subsystem

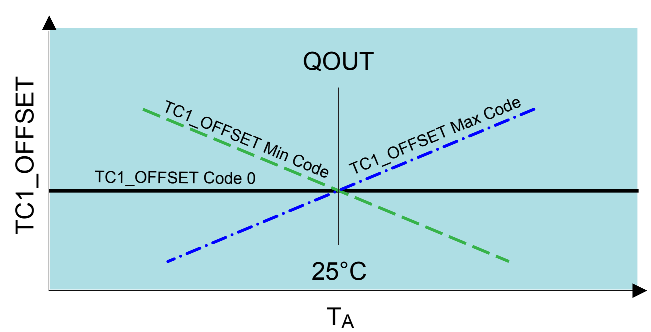

Figure 5: The 1st-Order Magnetic Offset Temperature Compensation coefficient, TC1_OFFSET, is used for linear adjustment of device output for temperature changes.

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The programmed values set the temperature compensation, Y_{TC}, according to the following formula:

$$Y_{TC}\,(\%FSO) = Y_{AD}\,(\%FSO) + [\,(TC1\_SENS\,(m\%/°C) \times \Delta T_A\,(°C)) + (TC2\_SENS\,(m\%/°C^2) \times \Delta T_A^2\,(°C))\,] \times Y_{AD}\,(\%FSO) + TC1\_OFFSET\,(G/°C) \times \Delta T_A\,(°C) \quad (2)$$

where:

Y_{AD} is the input from the analog subsystem via the A-to-D converter;

TC1_SENS is the first-order coefficient—either TC1_SENS_HOT or TC1_SENS_CLD depending on T_A;

TC2_SENS is the second-order coefficient—either TC2_SENS_HOT or TC2_SENS_CLD depending on T_A;

ΔT_A is the change in ambient temperature from 25°C (for example: at 150°C, ΔT_A = 150°C – 25°C = 125°C, or at –40°C, ΔT_A = –40°C – 25°C = –65°C);

SIG_OFFSET is the addition to the magnetic offset parameter (sets the centerpoint of Y_{AD}).

Table 2: Sensitivity Temperature Compensation Options

	T_A Range	
	< 25°C	> 25°C
1st Order	TC1_SENS_CLD	TC1_SENS_HOT
2nd Order	TC2_SENS_CLD	TC2_SENS_HOT

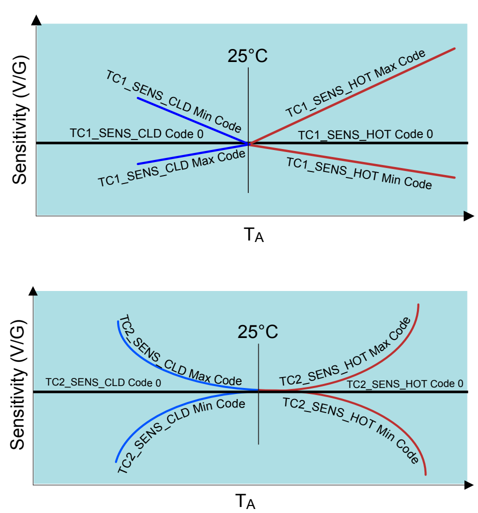

Figure 6: Sensitivity TC Functions — (upper) First Order, (lower) Second Order

Final Sensitivity (Gain) Adjustment

The A1343 has two programmable parameters to adjust Sensitivity, SENS_COARSE and SENS_MULT. The coarse Sensitivity value is determined by SENS_COARSE. For example, SENS_COARSE = 0 is approximately ±500G over 100% of the FSO range. This equates to an approximate Sensitivity of 0.1% FSO/G. Figure 7 shows approximate Sensitivity versus SENS_COARSE setting. The programmable parameter SENS_MULT, 6 in Figure 4, is used as a fine adjustment for Sensitivity. The value of this 12-bit parameter, applied in the digital subsystem, is multiplied to the coarse Sensitivity value (see equation 4). For example, SENS_MULT = 0 has a multiplier value of 1, SENS_MULT = 2047 has multiplier value of 2, and SENS_MULT = 2048 has a multiplier value of approximately 0. Please refer to the EEPROM Customer-Programmable Parameter Reference section for more information on parameter SENS_MULT.

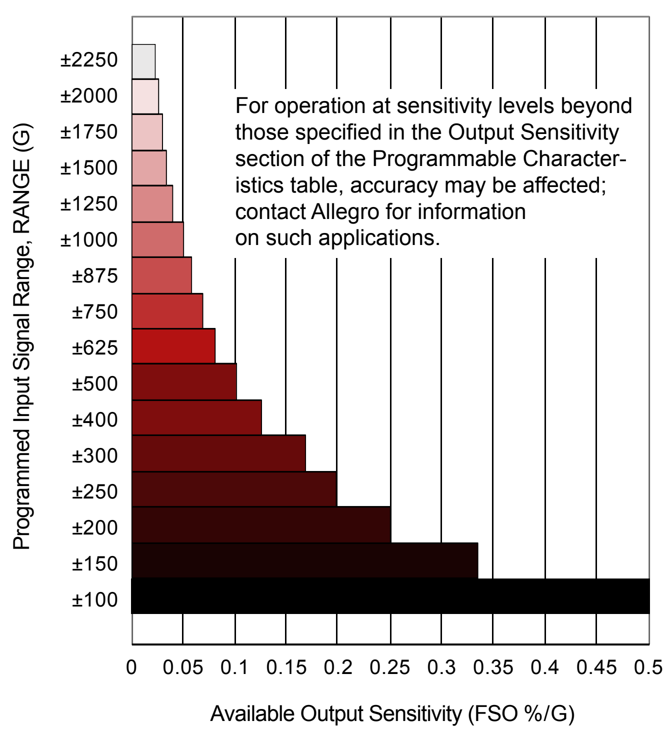

Figure 7: Correspondence of Magnetic Input Ranges and Resulting Available Output Sensitivity Levels

Output Fine Offset Adjustment

The A1343 DSP subsystem also includes a parameter to adjust the Quiescent Output, or offset. This programmable parameter QOUT_FINE, 6 in Figure 4, is used as a fine adjustment to the Quiescent Output. The value of QOUT_FINE is a percentage of the FSO. It is programmable to add or subtract as much as 50% of FSO. Refer to the EEPROM Customer-Programmable Parameter Reference section for more information on parameter QOUT_FINE.

The output of the digital subsystem, Y_{DA}, after applying the parameters for fine adjustment of Sensitivity and offset is shown in equation 3. This value is prior to the linearization and clamps.

$$Y_{DA}\ (\%FSO) = SENS\_MULT \times Y_{TC}\ (\%FSO) + QOUT\_FINE\ (\%FSO) \quad (3)$$

$$SENS\_OUT\ (\%FSO/G) = SENS\_MULT \times SENS\_COARSE\ (\%FSO/G) \quad (4)$$

where SENS_MULT is the multiplication factor from 0 to 2.

Linearization of Output

The A1343 programmable linear Hall-effect sensor IC provides an output that is proportional to a magnetic input, within a specified range. In some applications, the magnetic input signal is often nonideal and nonlinear. However, it is optimal for the sensor to best approximate the ideal linear output. The A1343 provides a programmable linearization feature for this purpose. Applied in the digital subsystem (7 in Figure 4) the A1343 linearization algorithm uses 33 programmable coefficients, 32 segments, to manipulate the output function.

The coefficients are stored in EEPROM as 12-bit two's complement integers, where B_{IN}(min) is indicated by –2048 and B_{IN}(max) is indicated by 2047. Figure 8 shows an example input-output curve. The *y*-axis represents the 32 equal full-scale position segments, and the *x*-axis represents the the application input range.

Contact Allegro for more information on using the Linearization feature and available tools for calculating linearization coefficients.

The polarity of the output function can be inverted by reversing the mapping of either the input or the output of the algorithm.

Setting the LIN_INPUT_INVERT parameter to 1 inverts the polarity of the calculated linearization coefficients by inverting the input values.

Output Polarity Setting

The OUTPUT_INVERT parameter sets the device output signal polarity with respect to the applied magnetic field polarity. The default (0) is increasing in a south magnetic field and decreasing in a north magnetic field. Setting this parameter to 1 causes output voltage decrease in a south field and increase in a north field.

Output Clamps Setting

The A1343 digital subsystem contains programmable clamp features to adjust the normal operating output range; see 8 in Figure 4. The A1343 output clamps are initially set to 0% and 100% of FSO, for low and high output clamp respectively. The parameters, CLAMP_HIGH and CLAMP_LOW are available to adjust limits for the normal operating output. The A1343 Diagnostic outputs levels are not bound by these parameters.

Output Protocol Selection

The A1343 supports an output in either PWM or SENT format. The PWM_MODE parameter in EEPROM sets the format. (Output format programming is described in the Linear Output Protocols section.)

Protection Features

Lockout and clamping features protect the A1343 internal circuitry and prevent spurious output when supply voltage is out of specification.

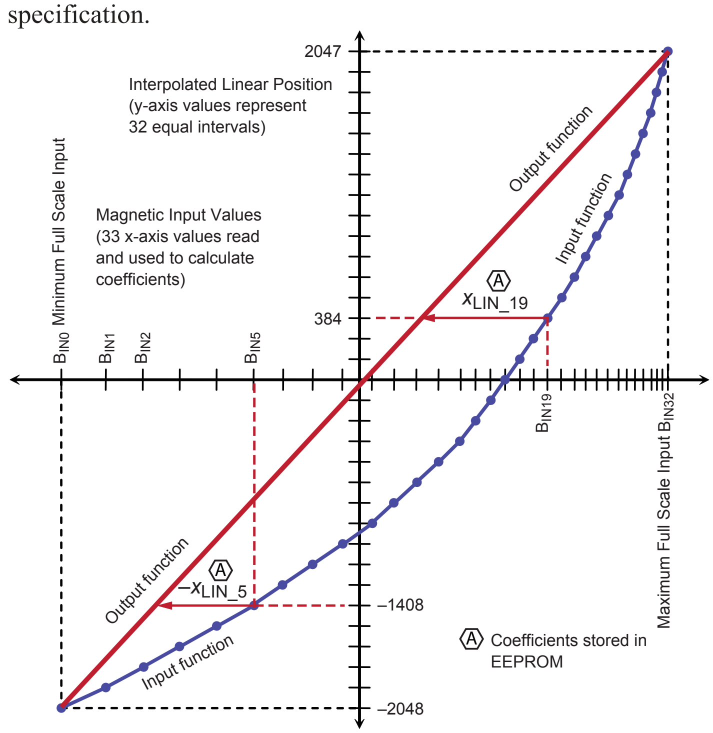

Figure 8: Sample of Linearization Function Transfer Characteristic

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Preprogrammed Default Values

Default values prevent system failures due to communication errors during real-time customer reprogramming of EEPROM. The default values also can be used as defaults for normal operation, reducing the initial customer programming requirements.

Operating Overvoltage and Undervoltage Lockout

Supply voltage detection features protect the A1343 internal circuitry and prevent spurious output when V_{CC} is out of specification. Diagnostic circuitry reuses the output pin (OUT) to provide feedback to the external controller. The A1343 provides protection for both overvoltage and undervoltage on the supply line.

The A1343 has two active circuits to identify when the supply voltage is below the minimum operating level. The internal power-on reset circuitry, POR, controls when an internal reset is triggered. If the supply voltage drops below POR_{LOW}, an internal reset occurs and the output is forced to a high-impedance state. When the supply voltage rises above POR_{HIGH}

The Low Voltage Detection feature, LVD, provides feedback to the external controller when V_{CC} is below minimum operating level but above the POR threshold. This feature is enabled by default and is disabled by setting LVD_DIS to logic 1. When configured for SENT output, if the supply voltage drops below $V_{CC(LVD)LOW}$, a status bit is set in the SENT message to indicate a low supply voltage condition. When configured for PWM output, if the supply voltage drops below $V_{CC(LVD)LOW}$, the output is forced to V_{SAT}. As the supply voltage rises above $V_{CC(LVD)HIGH}$, the output returns to normal operating state.

The Overvoltage Lockout Threshold, $V_{CC(OV)}$, is customer-programmable to one of two specified values, by setting the OVLO_LO parameter. When OVLO_LO = 1, programming pulses can cause the part to enter into and exit out of overvoltage lockout mode, resulting in an invalid output. If overvoltage conditions are reached, the PWM output will be brought to V_{SAT} or the SENT_STATUS bits will be set to indicate the condition.

Open Circuit Detection

Diagnostic circuitry reuses the output pin (OUT) to provide feedback to the external controller. A sense resistor, R_{OCD}, can be placed between OUT and a separate V_{BAT} reference, as shown in Table 3.

Memory Locking Mechanisms

The A1343 is equipped with two distinct memory locking mechanisms:

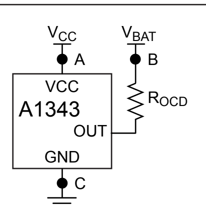
• **Default Lock.** At power-up, all registers of the A1343 are locked by default. EEPROM and volatile memory cannot be read or written. To disable Default Lock, a specific 30-bit customer access code is written to address 0x24 in less than 70 ms from power-up; see Write Access code. After this, device registers are accessible through the programming interface.

If VCC is power-cycled, the Default Lock automatically re-enables. This ensures that during normal operation, memory content will not be altered due to unwanted glitches on VCC or the output pin.

• **Lock Bit.** This is used after EEPROM parameters are programmed by the customer.

The customer programmable EELOCK feature disables the ability to read or write any register. This feature takes effect after writing the EELOCK bit and resetting power to the device. This prevents the ability to disable Default Lock using the method described above. Note that after EELOCK bit is set and VCC pin power-cycled, the customer will not have the ability to clear the EELOCK bit or to read/write any register.

Table 3: Open Circuit Diagnostic Truth Table

	Node A	Node B	Node C	OUT State
V_{BAT} Referenced				
	Open	Closed	Closed	0 V to V_{BAT}
	Closed	Open	Closed	GND
	Open	Open	Closed	GND
	Open	Closed	Open	V_{BAT}
	Closed	Open	Open	V_{CC}
	Closed	Closed	Open	V_{CC} to V_{BAT}

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Typical Application

Multiple A1343 linear devices can be connected to the external controller as shown in Figure 9. However, EEPROM programming in the A1343 occurs when the external control unit excites the A1343 OUT pin by EEPROM pulses generated by the ECU. Whichever A1343s that are excited by EEPROM pulses on their OUT pin will accept commands from the controller.

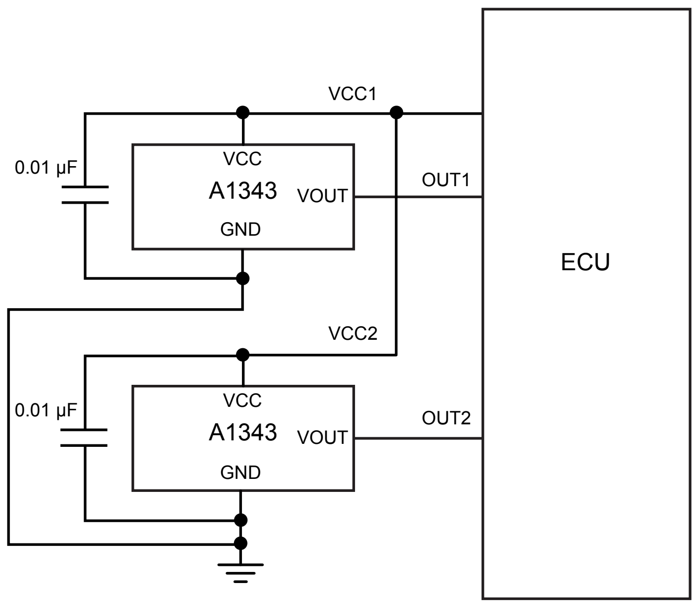

Figure 9: Typical Application

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PROGRAMMING SERIAL INTERFACE

The A1343 incorporates a serial interface that allows an external controller to read and write registers in the A1343 EEPROM and volatile memory. The A1343 uses a point-to-point communication protocol, based on Manchester encoding per G. E. Thomas (a rising edge indicates 0 and a falling edge indicates 1), with address and data transmitted MSB first.

Transaction Types

Each transaction is initiated by a command from the controller. The A1343 does not initiate any transactions. Two commands are recognized by the A1343: Write and Read. There also is a special function Write command: Write Access Code. One response frame type is generated by the A1343, Read Acknowledge.

If the command is Read, the A1343 responds by transmitting the requested data in a Read Acknowledge frame. If the command is any other type, the A1343 does not acknowledge.

As shown in Figure 10, the A1343 receives all commands via the VCC pin. It responds to Read commands via the OUT pin. This implementation of Manchester encoding requires the communication pulses be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages for the VCC line and the OUT line. The Write command pulses to EEPROM are supported by two high-voltage pulses on the OUT line.

Writing the Access Code

If the external controller will write to or read from the A1343 memory during the current session, it must establish serial communication with the A1343 by sending a Write command including the Access Code within 70 ms after powering up the A1343. If this deadline is missed, all write and read access is disabled until the next power-up.

Writing to EEPROM

When a Write command requires writing to EEPROM (all standard Writes), after the Write command the controller must also send two *Programming pulses*, well-separated, long high-voltage strobes via the OUT pin. These strobes are detected internally, allowing the A1343 to boost the voltage on the EEPROM gates.

The required sequence is shown in Figure 11.

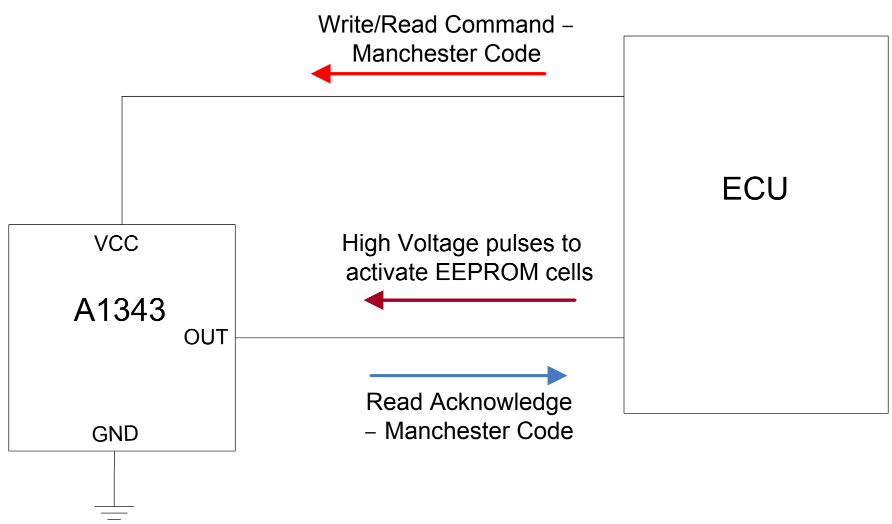

Figure 10: Top-Level Programming Interface

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Reading from EEPROM

A Read command with the register number is sent from the controller to the A1343. The device responds with a Read Acknowledge frame. Output is automatically disabled after the Read command from the controller is received and output is enabled after a Read Acknowledge command is sent.

Error Checking

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check).

The CRC algorithm is based on the polynomial

$$g(x) = x^3 + x + 1 \ ,$$

and the calculation is represented graphically in Figure 12.

The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111.

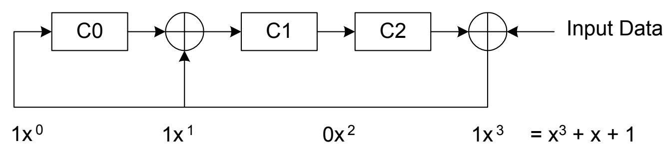

Figure 12: CRC Calculation

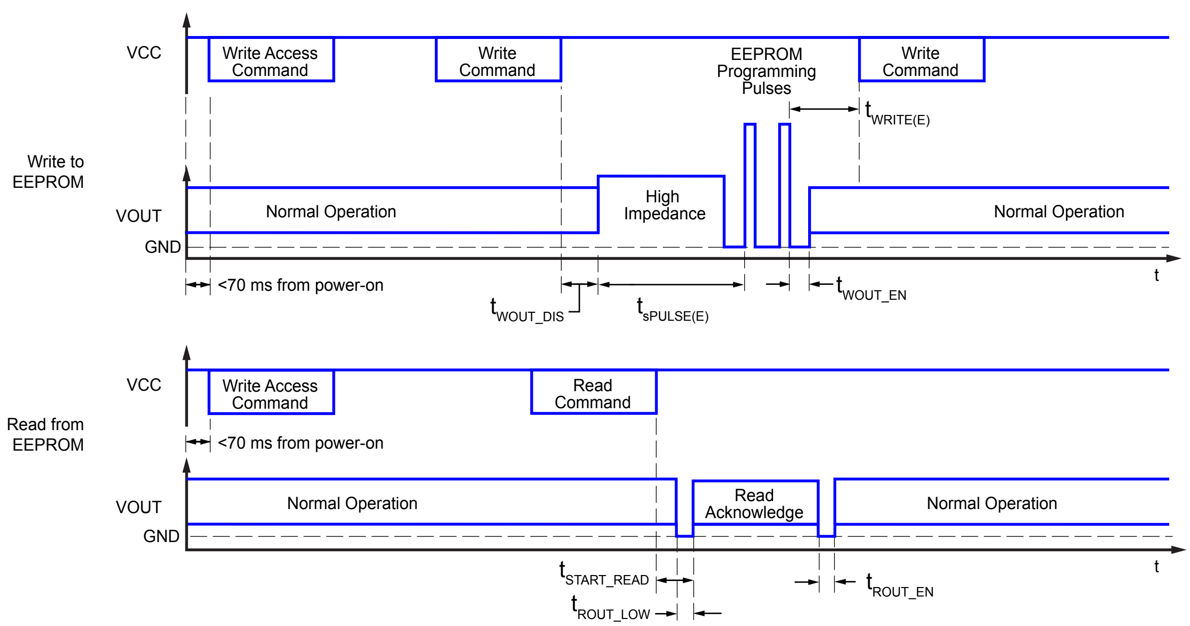

Figure 11: Programming Read and Write Timing Diagrams (see Serial Interface Reference section for definitions)

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SERIAL INTERFACE REFERENCE

Table 4: Serial Interface Protocol Characteristics [1]

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
INPUT/OUTPUT SIGNAL TIMING						
Access Code Timeout	t_{acc}	Customer Access Code should be fully entered in less than t_{ACC}, measured from when V_{CC} crosses $V_{CC(UV\_high)}$.	–	–	70	ms
Bit Rate		Defined by the input message bit rate sent from the external controller	4	–	100	kbps
Bit Time	t_{BIT}	Data bit pulse width at 4 kbps	243	250	257	µs
		Data bit pulse width at 100 kbps	9.5	10	10.5	µs
Bit Time Error	err_{TBIT}	Deviation in t_{BIT} during one command frame	–11	–	+11	%
Write Output Disable Delay	t_{WOUT_DIS}	Required delay from the trailing edge of certain Write command frames to output entering the high-impedance state	–	7 µs – 0.25 × t_{BIT}	60	µs
Write Delay	$t_{WRITE(E)}$	Required delay from the trailing edge of the second EEPROM Programming pulse to the leading edge of a following command frame	2 × t_{BIT}	–	–	µs
Write Output Enable Delay	t_{WOUT_EN}	Delay from the trailing edge of the final EEPROM programming pulse to output entering the normal operation state	–	6	60	µs
Read Acknowledge Delay	t_{READ}	Required delay from the trailing edge of a Read Acknowledge frame to the leading edge of a following command frame	2 × t_{BIT}	–	–	µs
Read Output Disable Delay	t_{ROUT_LOW}	Time the output is pulled low by device before Read Acknowledge message	–	45	60	µs
Read Delay [2]	t_{START_READ}	Delay from the trailing edge of a Read command frame to the leading edge of the Read Acknowledge frame	25 µs – 0.25 × t_{BIT}	50 µs – 0.25 × t_{BIT}	150 µs – 0.25 × t_{BIT}	µs
Read Output Enable Delay	t_{ROUT_EN}	Required delay from the trailing edge of the final Read Acknowledge pulse to output entering the normal operation state	–	45	60	µs
Disable Output Delay [2]	t_{DIS_OUT}	Delay from the trailing edge of a Disable Output command frame to the device output going from normal operation to the high-impedance state	1 µs – 0.25 × t_{BIT}	7 µs – 0.25 × t_{BIT}	15 µs – 0.25 × t_{BIT}	µs
Enable Output Delay [2]	t_{ENB_OUT}	Delay from the trailing edge of an Enable Output command frame to the device output going from the high-impedance state to normal operation	1 µs – 0.25 × t_{BIT}	7 µs – 0.25 × t_{BIT}	15 µs – 0.25 × t_{BIT}	µs
EEPROM PROGRAMMING PULSE						
EEPROM Programming Pulse Setup Time	$t_{sPULSE(E)}$	Delay from last edge of write command to start of EEPROM programming pulse	40	–	–	µs
INPUT/OUTPUT SIGNAL VOLTAGE						
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to VCC line	7.3	–	–	V
		Read from OUT line	V_{CC} – 0.2	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to VCC line	–	–	5.7	V
		Read from OUT line	–	–	V_{SAT}	V

[1] Determined by design.
[2] In the case where a slower baud rate is used, the output responds before the transfer of the last bit in the command message is completed.

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Serial Interface Message Structure

The general format of a command message frame is shown in Figure 13. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.

The bits are described in Table 5.

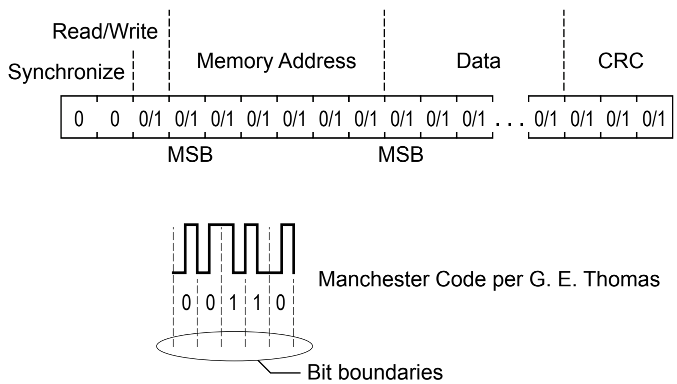

Figure 13: General Format for Serial Interface Commands

Table 5: Serial Interface Command General Format

Bits	Parameter Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
30	Data	0/1	[As required]
3	CRC	0/1	Incorrect value indicates errors

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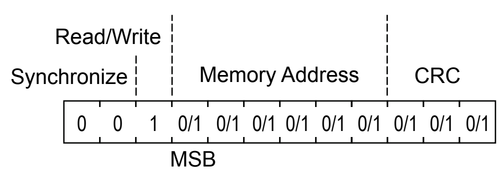
The following command messages can be exchanged between the device and the external controller:

- Read
- Read Acknowledge
- Write
- Write Access Code

For EEPROM address information, refer to the EEPROM Structure section.

READ

Function	Provides the address in A1343 memory to be accessed to transmit the contents to the external controller in the next Read Acknowledge command.
Syntax	Sent by the external controller on the A1343 VCC pin.
Related Commands	Read Acknowledge
Pulse Sequence	
Options	Requires disabling of memory locking mechanisms.
Examples	Read address 0x08 Read/Write = 1 Memory Address = 001000 CRC bits = 110

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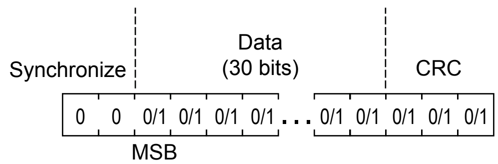
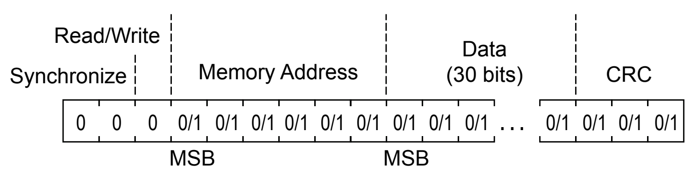
READ ACKNOWLEDGE

Function	Transmits to the external controller data retrieved from the A1343 memory in response to the most recent Read command.
Syntax	Sent by the A1343 on the A1343 OUT pin. Sent after a Read command.
Related Commands	Read
Pulse Sequence	
Options	The 6 MSBs are EEPROM data error checking bits. Refer to the EEPROM Structure section for more information.
Examples	–

WRITE

Function	Transmits to the A1343 data prepared by the external controller.
Syntax	Sent by the external controller on the A1343 VCC pin.
Related Commands	Write Access Code
Pulse Sequence	
Options	Requires disabling of memory locking mechanisms.
Examples	–

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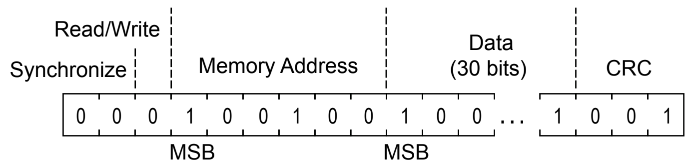
WRITE ACCESS CODE

Function	Transmits the Access Code to the A1343; data prepared by the external controller, but must match the internal 30-bit code in the A1343 memory.
Syntax	Sent by the external controller on the A1343 VCC pin. Sent within 10 ms of A1343 power-on, and before any other command.
Related Commands	
Pulse Sequence	
Options	None
Examples	Standard Customer Access Code: 0x2781_1F77 to address 0x24 Read/Write = 0 Memory Address = 100100 Data bits = 10 0111 1000 0001 0001 1111 0111 0111 CRC bits = 001

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LINEAR OUTPUT PROTOCOLS

The operating output of the A1343 is digital voltage signal that transfers information proportionally to the applied magnetic input signal. Two customer-selectable options are provided for output signal formatting: pulse-wave modulated (PWM), and single edge nibble transmission encoding scheme (SENT, SAEJ2716).

Note: The device response to the applied magnetic field is on the OUT pin. However, that pin is also used to transmit data in response to a serial read command, during which the normal output operation is suppressed. Refer to the Programming Serial Interface section for more information. The EEPROM is described in the EEPROM Structure section.

The output falling edge slew rate is adjustable using the OUTDRV_CFG parameter. Adjusting this can improve EMC performance by reducing high-frequency currents. This parameter can also increase the output fall time and result in longer minimum pulse durations for serial communication or SENT transmission.

PWM Output Mode

PWM involves converting the output voltage amplitude to a series of constant-frequency binary pulses, with the percentage of the of high portion of the pulse varied in direct proportion to the applied magnetic field.

The PWM output mode is configured by setting the following parameters in EEPROM:

- PWM_MODE set to 1 to select the PWM option (for programming parameters, see EEPROM Structure section)
- FPWM sets the PWM carrier frequency
- CALIBRATE_PWM parameter can be set to enable calibration of the output 50% duty cycle level at power-on

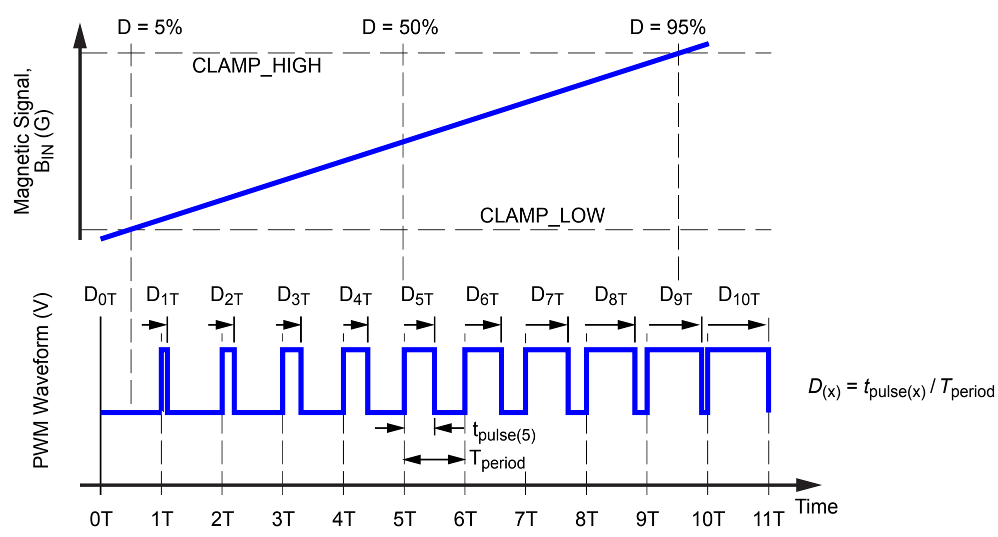

Figure 14: PWM mode outputs a duty-cycle-based waveform that can be read by the external controller as a cumulatively changing continuous voltage.

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SENT Output Mode

The SENT output mode converts the input magnetic signal to a binary value mapped to the Full Scale Output, FSO, range of 0 to 4095, shown in Figure 15. This data is inserted into a binary pulse message, referred to as a *frame*, that conforms to the SENT data transmission specification (SAEJ2716 JAN2010). Certain parameters for configuration of the SENT messages can be set in EEPROM.

The SENT output mode is configured by setting the following parameters in EEPROM:

- PWM_MODE set to 0 (default) to select the SENT option
- SENT_x programming parameters (see EEPROM Structure section)

Message Structure

A SENT message is a series of *nibbles*, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval
- Either interval can be the *delimiting state*, which only sets a boundary for the nibble; to assign the delimiting state, select a fixed duration for the interval (the SENT_LOVAR parameter selects the interval, and SENT_FIXED sets the duration)
- The other interval in the pair becomes the *information state* and is variable in duration in order to contain the data payload of the nibble

The duration of a nibble is denominated in clock *ticks*. The period of a tick is set by dividing a 4-MHz clock by the value of the SENT_TICK parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The nibbles of a SENT message are arranged in the following required sequence (see Figure 16):

1. Synchronization and Calibration: flags the start of the SENT message
2. Status and Communication: provides A1343 status and the format of the data
3. Data: magnetic field and optional data
4. CRC: error checking
5. Pause Pulse (optional): sets timing relative to A1343 updates

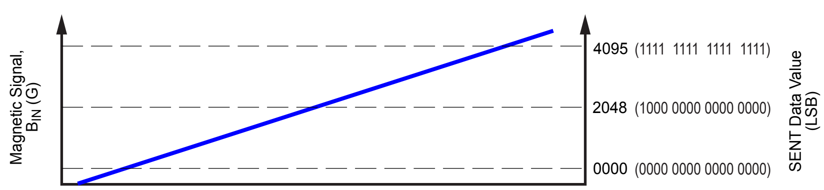

Figure 15: SENT mode outputs a digital value that can be read by the external controller and combined with accompanying range setting data to calculate the corresponding voltage level.

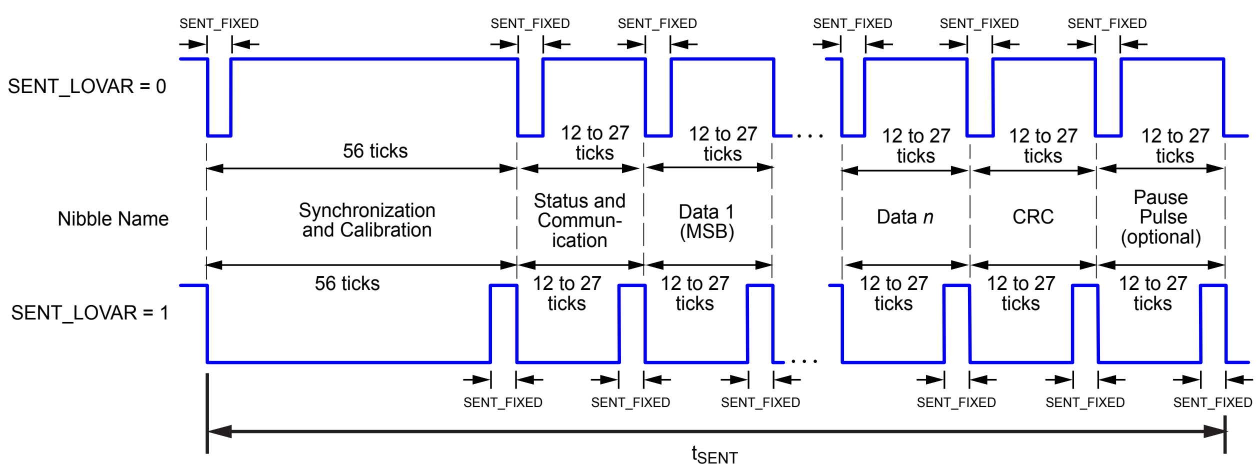

Figure 16: General Format for SENT Message Frame — (upper panel) low state fixed, (lower panel) high state fixed

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Optional Serial Output Protocol

In the Status and Communication section, the data format selection can be:

• Normal device output (voltage proportional to applied magnetic field) in SENT protocol (SENT_SERIAL = 0).

• Augmented data on the magnetic parameters and device settings, in an optional Serial Output protocol (SENT_SERIAL = 1, 2, or 3). Any of these three protocols enables transmission of values from the following EEPROM parameters, in the following order:

Message ID (4 or 8 bits)	Data (8, 12, or 16 bits)
0	Corrected temperature
1	SENS_COARSE
1	SIG_OFFSET
3	QOUT_FINE
4	SENS_MULT
5	CLAMP_HIGH
6	CLAMP_LOW
7	DEVICE_ID (always 1343_{10})

▫ Additional Short serial protocol (SENT_SERIAL = 1). Has a message payload of 12 bits: 8 bits are for value data, and 4 bits for the message ID (identification). A total of 6 separate SENT messages are required to transmit the entire data group.

▫ Additional Enhanced 16-bit serial protocol (SENT_SERIAL = 2). Has 12 bits for value data, and 4 bits for the message ID. A total of 8 SENT messages are required to transmit the entire data group.

▫ Additional Enhanced 24-bit serial protocol (SENT_SERIAL = 3). Has 16 bits for value data, and 8 bits for the message ID. A total of 12 SENT messages are required to transmit the entire data group.

Data Nibble Format

When transmitting normal operation data, information about the magnetic field is embedded in the first three Data nibbles. Each Data nibble consists of 4 bits with values ranging from 0 to 15. In order to present an output with the resolution of 12 bits, 3 Data nibbles are required. The Data nibble containing the MSB of the whole Data section is sent first.

Three additional optional Data nibbles can be associated with other parameters, by setting the parameter SEND_DATA:

• Counter – Each message frame has a serial number in each Counter nibble

• Temperature – Temperature data from the A1343 internal temperature sensor, in two's complement format, with MSB first:

  ▫ All zeros = 25°C
  ▫ For SENT_SERIAL = 2 or 3 temperature slope = 8 LSB/°C
  ▫ For SENT_SERIAL = 1, temperature slope = 0.5 LSB/°C.

• Inverted – The last nibble in the message frame is the first nibble, inverted (as an additional error check)

Pause Pulse Timing Synchronization

In the Pause Pulse section, additional time can be added at the end of a SENT message frame to ensure all message frames are of appropriate length. The SENT_UPDATE parameter selects one of these options:

• Allow message frame duration to vary according to the contents; no Pause pulse is applied. (SENT_UPDATE = 0)

• The device sends messages with constant duration. If a particular message is shorter, a Pause pulse is inserted with a length that completes the message period. (SENT_UPDATE = 1)

• Synchronize the message frame transmission rate with the A1343 internal update rate (set by BW value) by inserting a calculated Pause pulse to complete required period. (SENT_UPDATE = 2)

Figure 17, Figure 18, and Figure 19 show examples of the timing relationship between SENT message Pause pulse configurations and the internal update rate of the A1343.

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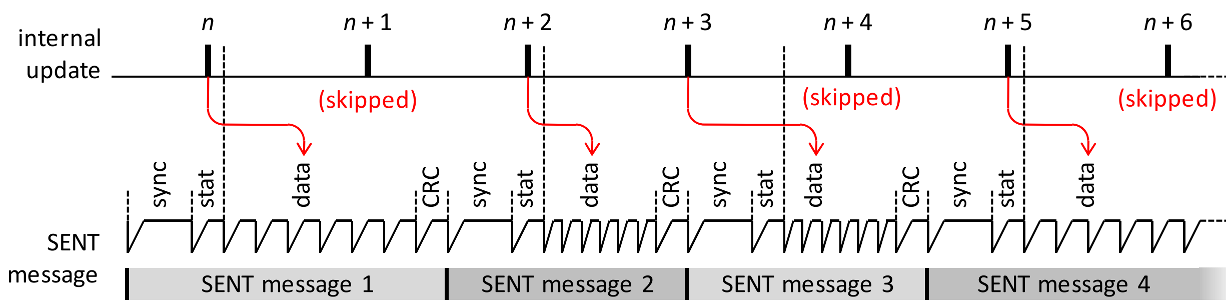

Figure 17: Messages do not contain a Pause pulse (SENT_UPDATE = 0), so the SENT message frame rate is not constant. The value transmitted in a message is taken from the last internal update ready before the first Data nibble of the message is composed. Therefore, individual internal updates may be skipped or repeated, depending on the BW bandwidth and SENT_TICK time settings.

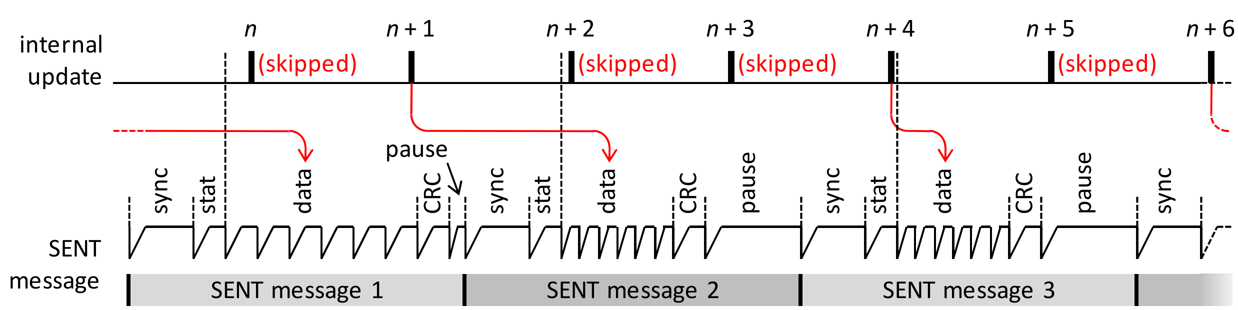

Figure 18: A constant message frame rate is used, and for each message, a Pause pulse is used to extend the message to match the frame rate (SENT_UPDATE = 1). Internal updates may be skipped or repeated depending on the BW bandwidth and SENT_TICK time settings. The quantity of skipped or repeated internal updates can vary from message to message.

Note: Although the frame transmission rate is constant, discrete SENT messages do not represent equal time interval sampling of the magnetic field.

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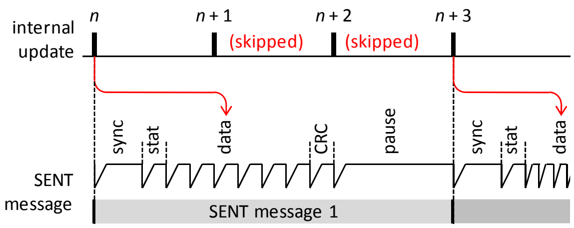
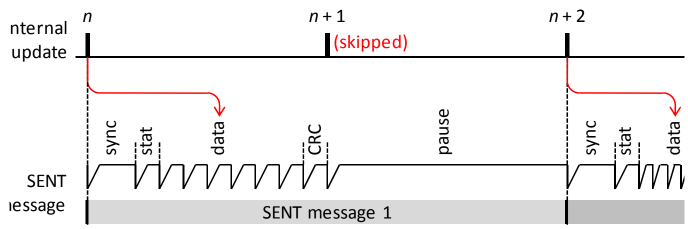
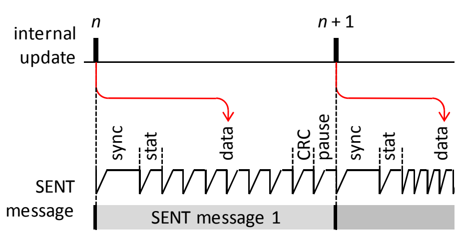


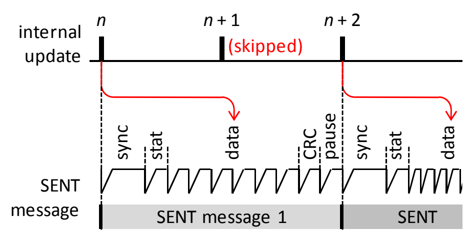
Panel 19(a). The longest possible SENT message is synchronized at three times the internal update rate. The first update is ready before the synchronization nibble is composed, and is transmitted. Three more updates occur before the next SENT message, so only the third update data is included, and the two intervening updates are skipped.



Panel 19(b). The filter bandwidth is reduced by twice relative to the bandwidth in panel (a), which doubles the internal update interval. The longest possible SENT message is now synchronized at two times the internal update rate. The first update is ready before the synchronization nibble is composed, and is transmitted. Two more updates occur before the next SENT message, so only the second update data is included, and the one intervening update is skipped.



Panel 19(c). The internal update rate is the same as in panel (b), but the tick duration is reduced slightly. The longest possible SENT message is now synchronized at the internal update rate. Each update is ready before the synchronization nibble is composed, and is transmitted. No updates are skipped.



Panel 19(d). The faster update rate of panel (a) and the shorter tick duration of panel (c) are applied. Because the panel (d) higher bandwidth setting also applies, the overall A1343 response time is faster than that shown in panel (c). However, the panel (c) settings reduce front-end noise better than those of panel (d), because of the lower bandwidth.

Figure 19: The SENT message rate is synchronized with the internal A1343 internal update rate. For each message, a Pause pulse is used to extend the message to match the internal update rate (SENT_UPDATE = 2). A consistent number of updates are skipped or repeated from message to message. The internal update value transmitted is from the last update ready before the Synchronization and Calibration nibble of the message is composed.

The SENT_UPDATE parameter has two other options, which allow direct control of when magnetic field data is sent to the external controller:

- Tandem data latching and sending (SENT_UPDATE = 3)
- Immediate data latching with a controllable delay before sending (SENT_UPDATE = 4)

When SENT_UPDATE = 3 (upper panel in Figure 20), while the A1343 has a Pause pulse on the device output, the controller triggers a latch-and-send sequence by pulling the A1343 output low. When the controller releases the output, the current magnetic field data is latched, and after a delay of t_{dSENT} the latched data is sent to the controller. This option is useful when the controller requires a prompt response on the current magnetic field.

When SENT_UPDATE = 4 (lower panel in Figure 20), while the A1343 has a Pause pulse on the device output, the controller triggers a latch-and-send sequence by pulling the output low. With this option, the current magnetic field data is latched immediately. This allows the controller to postpone receiving the data. When the output is eventually released, the data is sent to the controller after a delay of t_{dSENT}. This option is useful where multiple A1343s are connected to the controller (see Typical Application, Figure 9). All the A1343s can be instructed at the same time to latch magnetic field data, and the controller can then retrieve the data from each A1343 individually.

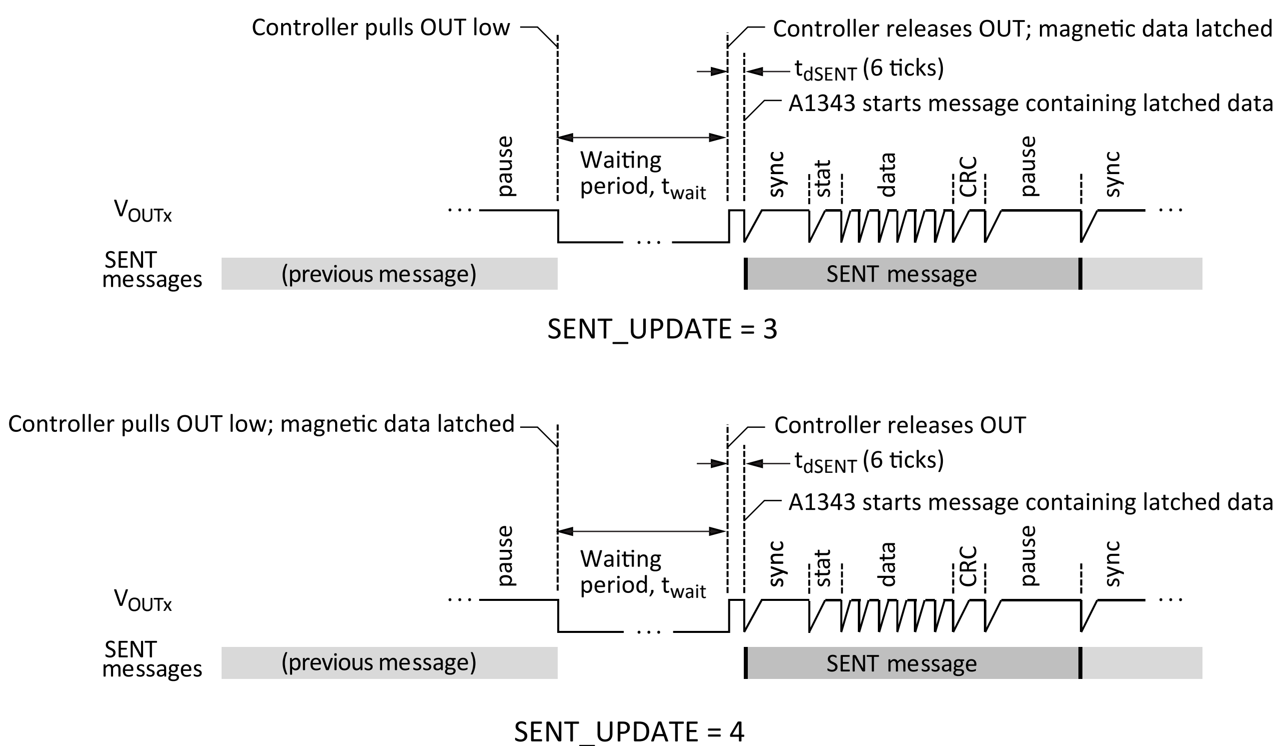


Figure 20: Device output behavior where normal operation magnetic field data is latched at a defined time: (upper panel) if SENT_UPDATE = 3, latched and sent at end of a low pulse, or (lower panel) if SENT_UPDATE = 4, latched at the beginning of a low pulse, but not sent until the end of the pulse. The total delay from the beginning of the low pulse until the data message begins is: $t_{wait} + t_{dSENT}$.

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The general format of a command message frame is shown in Figure 16. The individual sections of a SENT message are described in Table 6.

Table 6: SENT Message Frame Section Definitions

Section	Description
SYNCHRONIZATION AND CALIBRATION	
Function	Provide the external controller with a detectable start of the message frame. The large quantity of ticks distinguishes this section, for ease of distinction by the external controller.
Syntax	Nibbles: 1 Quantity of ticks: 56 Quantity of bits: 1
STATUS AND COMMUNICATION	
Function	Provides the external controller with the status of the A1343 and indicates the format and contents of the Data section.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 Quantity of bits: 4 1:0 Device status (set by SENT_STATUS parameter) 3:2 Message serial data protocol (set by SENT_SERIAL parameter)
DATA	
Function	Provides the external controller with data selected by the SENT_SERIAL parameter.
Syntax	Nibbles: 3 to 6 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4 (each nibble)
CRC	
Function	Provides the external controller with cyclic redundancy check (CRC) data for certain error detection routines applied to the Data nibbles.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4
PAUSE PULSE	
Function	(Optional) Additional time can be added at the end of a SENT message frame to ensure all message frames are of appropriate length. The SENT_UPDATE parameter sets format.
Syntax	Nibbles: 1 Quantity of ticks: 12 minimum (length determined by SENT_UPDATE option and by the individual structure of each SENT message) Quantity of bits: n.a.

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EEPROM STRUCTURE

Programmable values are stored in an on-board EEPROM, including both volatile and nonvolatile registers. Although it is separate from the digital subsystem, it is accessed by the digital subsystem EEPROM Controller module.

Note: All customer-programmable registers are set to 0 as the initial default value when the devices are shipped from the factory.

Because EEPROM can be read by multiple devices, an arbiter controls access to EEPROM. In the case of simultaneous accesses to EEPROM, priority is assigned as follows:

1. Static Registers (highest)
2. Temperature Compensation
3. Linearization
4. Serial Interface (lowest)

The EEPROM is organized as 30-bit wide words, and by default each word has 24 data bits and 6 ECC (Error Checking and Correction) check bits, stored as shown in Figure 21.

EEPROM Bit	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15
Contents	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	C5	D10

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D9	D8	D7	D6	D5	D4	C4	D3	D2	D1	C3	D0	C2	C1	C0

Figure 21: EEPROM Word Bit Sequence; C# – Check Bit, D# – Data Bit

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Table 7. EEPROM Register Map of Customer-Programmable Parameters

Address	Bits	Parameter Name	Description	DAC profile
0x08	23:15	TC2_SENS_HOT	2nd-Order Sensitivity Temperature Coefficient, ΔT (from 25°C) > 0	Two's complement
0x08	14:6	TC2_SENS_CLD	2nd-Order Sensitivity Temperature Coefficient, ΔT (from 25°C) < 0	Two's complement
0x08	5:2	SENS_COARSE	Coarse Sensitivity and Magnetic Input Signal Range	Nonuniform
0x08	1:0	Reserved		
0x09	23:16	TC1_SENS_HOT	1st-Order Sensitivity Temperature Coefficient, ΔT (from 25°C) > 0	Shifted two's complement
0x09	15:8	TC1_SENS_CLD	1st-Order Sensitivity Temperature Coefficient, ΔT (from 25°C) < 0	Shifted two's complement
0x09	7:0	TC1_OFFSET	1st-Order Magnetic Offset TC Compensation	Two's complement
0x0A	23:12	SCRATCH_C	Customer Scratchpad	Two's complement
0x0A	11:0	SENS_MULT	Sensitivity Multiplier	Two's complement
0x0B to 0x1A	23:12	LINPOS_COEFF (LIN_1, LIN_3, ..., LIN_31)	Linearization Coefficients (odd-numbered sampling positions)	Two's complement
0x0B to 0x1B	11:0	LINPOS_COEFF (LIN_0, LIN_2, ..., LIN_32)	Linearization Coefficients (even-numbered sampling positions)	Two's complement
0x1B	23	LIN_TABLE_DONE	Linearization Coefficients Loaded Flag	
0x1B	22	OUTPUT_INVERT	Invert polarity of device output	
0x1B	21	LIN_INPUT_INVERT	Linearization Input Polarity Inversion	
0x1B	20:12	ID_C	Customer Identification Number	
0x1C	23:18	CLAMP_HIGH	Clamp Upper Limit	
0x1C	17:12	CLAMP_LOW	Clamp Lower Limit	
0x1C	11	Reserved		
0x1C	10	OVLO_LO	Overvoltage Lockout Threshold	
0x1C	9	LVD_DIS	Low-Voltage Detection Disable	
0x1C	8:4	SIG_OFFSET	Magnetic Offset Compensation (Coarse)	Two's complement
0x1C	3	PWM_MODE	Normal Operation Output Mode (SENT / PWM)	
0x1C	2:0	BW		Nonuniform
0x1D	23:12	SCRATCH_C_1	Customer Scratchpad	
0x1D	11:0	QOUT_FINE	Quiescent Output Duty Cycle	Two's complement
0x1E	23	EELOCK	Setting this bit prevents any future communication to the device	
0x1E	22:21	Reserved		
0x1E	20:18	OUTDRV_CFG	Output Driver Setting	Exponential
0x1E	17:0	SENTPWM_CFG	SENT and PWM output mode configuration parameters (assignment determined by PWM_MODE bit)	Nonuniform
	17:11	SENT_TICK	Sets Tick Rate Coefficient (PWM_MODE = 0)	
	10:9	SENT_FIXED	Sets Fixed State Interval (PWM_MODE = 0)	
	8	SENT_LOVAR	Sets Fixed State Assignment (PWM_MODE = 0)	
	7:5	SENT_UPDATE	Sets Pause Pulse and Message Frame Rate (PWM_MODE = 0)	
	4:3	SENT_DATA	Sets Data Nibble Format (PWM_MODE = 0)	
	2	SENT_STATUS	Sets Error Condition (PWM_MODE = 0)	
	1:0	SENT_SERIAL	Sets Message Series Format (PWM_MODE = 0)	
	3	CALIBRATE_PWM	Enables 50% Duty Cycle Calibration (PWM_MODE = 1)	
	2:0	FPWM	Sets PWM Carrier Frequency (PWM_MODE = 1)	
0x1F	23:0	SCRATCH_C_2	Customer Scratchpad	

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EEPROM CUSTOMER-PROGRAMMABLE PARAMETER REFERENCE

BW: Address 0x1C, bits 2:0

Function	Filter Bandwidth Selects the filter bandwidth (3-dB frequency) for the digitized applied magnetic field signal, applied when passed to the digital system after analog front-end processing. This selection also sets the internal update rate.		
Syntax	Quantity of bits: 3		
Related Commands	SIG_OFFSET, SENS_COARSE		
Values (typical)	Code	Bandwidth (Hz)	Internal Update Rate (kHz)
	000 (Default)	2000	8
	001	4000	16
	010	2000	8
	011	1000	4
	100	500	2
	101	250	1
	110	Not recommended	–
	111	Not recommended	–
Options	–		
Examples	–		

CALIBRATE_PWM: Address 0x1E, bit 3

Function	PWM Calibration Sent at power-on, commands the device to calculate the PWM 50% duty cycle to the centerpoint of the Full Scale Output range.
Syntax	Quantity of bits: 1
Related Commands	PWM_MODE (see EEPROM Structure Section)
Values	0: Disable calibration (Default) 1: Enable calibration
Options	Requires PWM_MODE = 1 for operation.
Examples	–

CLAMP_HIGH: Address 0x1C, bits 23:18

Function	Clamp Upper Limit Sets the percentage of the upper half of the Full Scale Output signal passed through at the end of the Digital Signal Processing stage.
Syntax	Quantity of bits: 6
Related Commands	CLAMP_LOW
Values	000000: Default (Maximum specified value, $OUT_{CLP(H)}$) 111111: (Minimum specified value, $OUT_{CLP(H)}$)
Options	The factory-programmed default, $OUT_{CLP(H)init}$, is used if this parameter is not set.
Examples	–

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CLAMP_LOW: Address 0x1C, bits 17:12

Function	Clamp Lower Limit Sets the percentage of the lower half of the Full Scale Output signal passed through at the end of the Digital Signal Processing stage.
Syntax	Quantity of bits: 6
Related Commands	CLAMP_HIGH
Values	000000: Default (Minimum specified value, $OUT_{CLP(L)}$) 111111: (Maximum specified value, $OUT_{CLP(L)}$)
Options	The factory-programmed default, $OUT_{CLP(L)init}$, is used if this parameter is not set.
Examples	–

EELOCK: Address 0x1E, bit 23

Function	Disables all communication to the device.
Syntax	Quantity of bits: 1
Related Commands	–
Values	0 (default): Default memory lock mechanism 1: Prevents any Read or Write transaction with the device
Options	Lock bit feature is enabled following a reset of the device power after setting the EELOCK bit.
Examples	Refer to Memory Locking Mechanisms section for more information.

FPWM: Address 0x1E, bits 2:0

Function	PWM Carrier Frequency Sets the carrier frequency for PWM mode normal output (voltage response to applied magnetic field). Selected frequency determines maximum output resolution.		
Syntax	Quantity of bits: 3		
Related Commands	PWM_MODE (see EEPROM Structure Section)		
Values (typical)	Code	PWM Frequency (kHZ)	Maximum Output Resolution (bits)
	000 (Default)	0.125	12
	001	0.25	12
	010	0.5	12
	011	1	11
	100	2	10
	101	4	9
	110	0.125	12
	111	0.125	12
Options	Requires PWM_MODE = 1 for selection		
Examples	–		

ID_C: Address 0x1B, bits 20:12

Function	Customer Identification Number Available register for identifying the A1343.
Syntax	Quantity of bits: 9
Related Commands	SCRATCH_C
Values	Free-form
Options	Values do not affect device operation.
Examples	–

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LIN_INPUT_INVERT: Address 0x1B, bit 21

Function	Linearization Input Polarity Inversion Inverts the polarity of the calculated linearization coefficients by inverting the input values.
Syntax	Quantity of bits: 1
Related Commands	LINPOS_COEFF, OUTPUT_INVERT
Values	0: Coefficients saved with calculated polarity (Default) 1: Coefficient polarity inverted before storage
Options	–
Examples	–

LINPOS_COEFF: Addresses 0x0B to 0x1B
(LIN_0, LIN_2, ..., LIN_32) bits 11:0
(LIN_1, LIN_2, ..., LIN_33) bits 23:12

Function	Linearization Coefficients These addresses are available to store customer-generated and loaded coefficients used for linearization of the temperature-compensated and offset digital signal. Note: These are not used by the device unless the LIN_TABLE_DONE bit is set.
Syntax	Quantity of bits: 12 (each) LIN_x corresponds to Input Sample B_{INx} Coefficient data stored in two's complement format Values must be monotonically increasing
Related Commands	LIN_INPUT_INVERT, LIN_TABLE_DONE, OUTPUT_INVERT
Values	Calculated according to applied magnetic field
Options	(see table below)
Examples	–

Options:

Input Sample	Output Position (%FSI)	EEPROM Address	Bits		Input Sample	Output Position (%FSI)	EEPROM Address	Bits
B_{IN0}	100	0x0B	11:00		B_{IN16}	16/32	0x13	11:00
B_{IN1}	31/32	0x0B	23:12		B_{IN17}	15/32	0x13	23:12
B_{IN2}	30/32	0x0C	11:00		B_{IN18}	14/32	0x14	11:00
B_{IN3}	29/32	0x0C	23:12		B_{IN19}	13/32	0x14	23:12
B_{IN4}	28/32	0x0D	11:00		B_{IN20}	12/32	0x15	11:00
B_{IN5}	27/32	0x0D	23:12		B_{IN21}	11/32	0x15	23:12
B_{IN6}	26/32	0x0E	11:00		B_{IN22}	10/32	0x16	11:00
B_{IN7}	25/32	0x0E	23:12		B_{IN23}	9/32	0x16	23:12
B_{IN8}	24/32	0x0F	11:00		B_{IN24}	8/32	0x17	11:00
B_{IN9}	23/32	0x0F	23:12		B_{IN25}	7/32	0x17	23:12
B_{IN10}	22/32	0x10	11:00		B_{IN26}	6/32	0x18	11:00
B_{IN11}	21/32	0x10	23:12		B_{IN27}	5/32	0x18	23:12
B_{IN12}	20/32	0x11	11:00		B_{IN28}	4/32	0x19	11:00
B_{IN13}	19/32	0x11	23:12		B_{IN29}	3/32	0x19	23:12
B_{IN14}	18/32	0x12	11:00		B_{IN30}	2/32	0x1A	11:00
B_{IN15}	17/32	0x12	23:12		B_{IN31}	1/32	0x1A	23:12
					B_{IN32}	0	0x1B	11:00

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LIN_TABLE_DONE: Address 0x1B bit 23

Function	Linearization Table Loaded Set by the customer to indicate custom coefficients have been loaded (into the LINPOS_COEFF area of EEPROM). When this flag is set, the device uses the customer coefficients for output linearization. Allows correction for targets that generate nonlinear magnetic fields.
Syntax	Quantity of bits: 1
Related Commands	LINPOS_COEFF
Values	0: Default, Linearization disabled. Linearization algorithm coefficients are bypassed. 1: Linearization enabled. Linearization algorithm applies customer-programmed coefficients to the processed signal.
Options	–
Examples	–

LVD_DIS: Address 0x1C bit 9

Function	Low Voltage Detection Disable Disable the low voltage detection feature
Syntax	Quantity of bits: 1
Related Commands	–
Values	0: Default, Low Voltage Detection enabled. 1: Low Voltage Detection disabled.
Options	–
Examples	–

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OUTDRV_CFG: Address 0x1E bits 20:18

Function	Output Signal Configuration Sets configuration of the output signal slew-rate control. Sets the ramp rate on the gate of the output driver, thereby changing slew rate at the output.			
Syntax	Quantity of bits: 3			
Related Commands	–			
Values	Code	Typical Fall Time (µs)		
		C_{LOAD} = 100 pF	C_{LOAD} = 1 nF	C_{LOAD} = 10 nF
	000 (Default)	0.048	0.149	1.324
	001	0.114	0.217	1.323
	010	0.202	0.309	1.404
	011	0.290	0.400	1.492
	100	0.760	0.854	1.948
	101	1.539	1.555	2.669
	110	3.161	2.978	4.118
	111	4.819	4.442	5.557
Options	–			
Examples	–			

OUTPUT_INVERT: Address 0x1B bit 22

Function	Output Polarity Inversion Inverts the polarity of the device output.
Syntax	Quantity of bits: 1
Related Commands	LINPOS_COEFF, LIN_INPUT_INVERT
Values	0: Positive output polarity. South field increases output voltage, north field decreases output voltage. 1: Negative output polarity. South field decreases output voltage and north field increases output voltage.
Options	–
Examples	–

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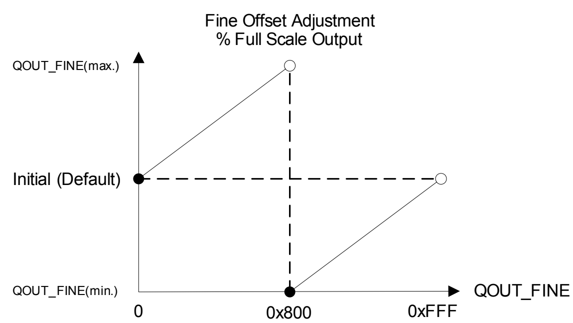
OVLO_LO: Address 0x1C, bit 10

Function	Overvoltage Lockout Threshold Sets the typical threshold value.
Syntax	Quantity of bits: 1
Related Commands	–
Values	0: Default (Higher value) 1: (Lower value) See $V_{CC(OV)LOW}$ and $V_{CC(OV)HIGH}$ for threshold limits.
Options	–
Examples	See Operating Overvoltage and Undervoltage Lockout section for description.

PWM_MODE: Address 0x1C, bit 3

Function	Normal Operation Output Mode Changes normal output (response to applied magnetic field) from SENT to PWM.
Syntax	Quantity of bits: 1
Related Commands	CALIBRATE_PWM, FPWM
Values	0: SENT (Default) 1: PWM
Options	–
Examples	–

QOUT_FINE: Address 0x1D, bits 11:0

Function	Quiescent Output (QOUT) Adjusts the device normal output (digital response to applied magnetic field) to set the baseline output level: for a quiescent applied magnetic field (B_{IN} ≈ 0 G).
Syntax	Quantity of bits: 12 Code stored in two's complement format
Related Commands	SIG_OFFSET
Values	
Options	The factory-programmed default, $QOUT_{init}$, is used if this parameter is not set.
Examples	Application Target: Required offset 0x800 (50% FSO). Offset after coarse adjustments and Sensitivity adjustments: 0x852 (52 %FSO). Selected Offset Adjustment: QOUT_FINE = 0xFAE (–2% FSO)

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SCRATCH_C_1: Address 0x1D, bits 23:12
SCRATCH_C_2: Address 0x1F, bits 23:0

Function	Customer Scratchpad For optional customer use in storing values in the device.
Syntax	Quantity of bits: SCRATCH_C_1, 12 SCRATCH_C_2, 24
Related Commands	IC
Values	Free-form field
Options	Values do not affect device operation.
Examples	–

SENS_COARSE: Address 0x08, bits 5:2

Function	Coarse Sensitivity Sets the nominal (coarse) sensitivity of the device, SENS_COARSE, which can be defined as OUT/ΔB_{IN}. Selection determines the RANGE, the extent of the applied magnetic flux intensity, B_{IN}, sampled for signal processing. (Use SIG_OFFSET to adjust the B_{IN} level at which RANGE is centered.)		
Syntax	Quantity of bits: 4		
Related Commands	SIG_OFFSET, SENS_MULT		
Values (typical)	Code	Typical Coarse Sensitivity At V_{CC} = 5 V and T_A = 25°C (%FSO/G)	RANGE (G)
	0000 (Default)	0.100	±500
	0001	0.333	±150
	0010	0.250	±200
	0011	0.200	±250
	0100	0.167	±300
	0101	0.125	±400
	0110	0.080	±625
	0111	0.067	±750
	1000	0.057	±875
	1001	0.050	±1000
	1010	0.040	±1250
	1011	0.033	±1500
	1100	0.029	±1750
	1101	0.025	±2000
	1110	0.050	±100
	1111	0.022	±2250
Options	The typical default Sensitivity, SENSinit, is selected when SENS_COARSE = 0. Output accuracy is reduced with codes 1110 and 1111.		
Examples	For an application with a maximum B_{IN} range of 500 G, the recommended RANGE setting is ±250 G (SENS_COARSE = 0011). This corresponds to an approximate Coarse Sensitivity of 0.2% FSO/G.		

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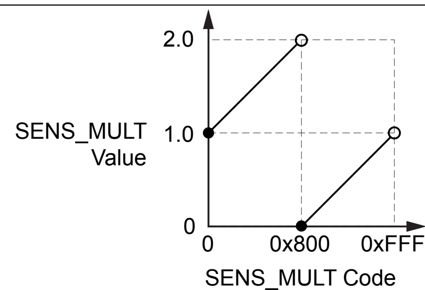
SENS_MULT: Address 0x0A, bits 11:0

Function	Sensitivity Multiplier After temperature compensation, establishes the gain of the device in normal output (response to a change in the applied magnetic field) by indicating a multiplier value. The resulting values for final Output Sensitivity, SENS_OUT, are expressed in terms of percentage of the full scale output, FSO, per gauss of applied magnetic field, B_{IN}. Both the magnitude of the available Sensitivity and the programmable increments (step size) are affected by the SENS_COARSE value.
Syntax	Quantity of bits: 12
Related Commands	RANGE (SENS_COARSE), TC1_SENS_CLD, TC1_SENS_HOT, TC2_SENS_CLD, TC2_ SENS_HOT
Values	
Options	The Sensitivity excluding linearization compensation is determined from the Coarse Sensitivity multiplied by the Sensitivity Multiplier.
Examples	Example targets: 10 %FSO at –210 G, and 90 %FSO at 210 G Maximum Input Field, B_{IN}: 480 G SENS_COARSE = 0 (RANGE = ±250 G) Nominal SENS_MULT = 0xF98 (Sensitivity multiplication factor of 0.95) Nominal Sensitivity = 0.19 %FSO

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SENT_DATA: Address 0x1E, bits 4:3

Function	Data Nibble Format Quantity and contents of Data nibbles in message. (Does not relate to data contained in the Status and Communication nibble.)
Syntax	Quantity of Bits: 2
Related Commands	PWM_MODE
Values	0 0: Nibbles 1,2,3: magnetic field data; nibbles 4,5: counter data; nibble 6: inverted nibble 1 (Default) 0 1: Nibbles 1,2,3: magnetic field data; nibbles 4,5: counter data; nibble 6: all zeros 1 0: Nibbles 1,2,3: magnetic field data; nibbles 4,5,6: current temperature data 1 1: Nibbles 1,2,3: magnetic field data (nibbles 4,5,6 skipped)
Options	Requires PWM_MODE = 0 for use.
Examples	–

SENT_FIXED: Address 0x1E, bits 10:9

Function	Fixed Interval Duration Indicates the quantity of ticks in fixed-duration intervals.
Syntax	Quantity of Bits: 2
Related Commands	SENT_LOVAR, PWM_MODE
Values	0 0: 5 ticks (Default) 0 1: 4 ticks 1 0: 7 ticks 1 1: 8 ticks
Options	SENT_FIXED = 0 recommend for standard SENT specification. Additional options are available to increase or decrease the communication rate. Requires PWM_MODE = 0 for use.
Examples	–

SENT_LOVAR: Address 0x1E, bit 8

Function	State Assignments Assigns fixed-duration state (becomes delimiting state; other interval becomes the information state)
Syntax	Quantity of Bits: 1
Related Commands	SENT_FIXED, PWM_MODE
Values	0: Low interval of every nibble is fixed in duration, and the high interval duration is set by SENT_FIXED (high interval becomes the information state) (Default) 1: High interval of every nibble is fixed in duration, and the low interval duration is set by SENT_FIXED (low interval becomes the information state)
Options	SENT_LOVAR = 0 recommended for standard SENT specification. For SENT_UPDATE = 3 or 4, the Pause pulse has a fixed low time regardless of the SENT_LOVAR setting. Requires PWM_MODE = 0 for use.
Examples	–

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SENT_SERIAL: Address 0x1E, bits 1:0

Function	Status and Communication Nibble Format Defines values of bits 2 and 3 inside the Status and Communication nibble.
Syntax	Quantity of Bits: 2
Related Commands	PWM_MODE
Values	0 0: Bits 2 and 3 are 0 (Default) 0 1: Bits 2 and 3 are 0 part of the Short Serial protocol: 8-bit value data, 4-bit message ID, 16 SENT frames are required to send an entire serial message 1 0: Bits 2 and 3 are part of the Enhanced 16-bit Serial protocol: 12-bit value data, 4-bit message ID, 18 SENT frames are required to send an entire serial message 1 1: Bits 2 and 3 are part of the Enhanced 24-bit Serial protocol: 16-bit value data, 8-bit message ID, 18 SENT frames are required to send an entire serial message
Options	If a serial protocol is set (SENT_SERIAL = 1, 2, or 3), bits 2 and 3 are serial data, so one SENT frame (the whole sent message) will contain only 2 bits. Requires PWM_MODE = 0 for use.
Examples	–

SENT_STATUS: Address 0x1E, bit 2

Function	Error Condition Status Defines values of bits 0 and 1 inside the Status and Communication nibble. Defines data inside the Status and Communication nibble on device error status.
Syntax	Quantity of Bits: 1
Related Commands	SENT_SERIAL, PWM_MODE, LVD_DIS
Values	(see tables below)
Options	Requires PWM_MODE = 0 for use. Low Voltage Detection requires LVD_DIS = 0.
Examples	A Status and Communication nibble value of 0010 indicates an overvoltage condition.

Values:

SENT_STATUS = 0

Bit 1	Bit 0	
0	0	No error (Default)
0	1	Low Voltage Detection, low supply voltage condition
1	0	Overvoltage condition
1	1	Nonrecoverable EEPROM error, bad Linearization table or other error

SENT_STATUS = 1

Bit 1	Bit 0	
0	0	No error (Default)
0	1	Error condition

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SENT_TICK: Address 0x1E, bits 17:11

Function	Tick Duration Sets the SENT tick rate coefficient: 4 MHz / SENT_TICK = tick (µs)
Syntax	Quantity of Bits: 7 Any value from 0 to 127 can be used
Related Commands	PWM_MODE
Values	000 0000: 3.0 µs (4 MHz / 12) (Default. Same as 000 1100) 000 0001: 0.25 µs (4 MHz / 1) 000 0010: 0.5 µs (4 MHz / 2) 000 0011: 0.75 µs (4 MHz / 3) 000 1100: 3.0 µs (4 MHz / 12) 111 1110: 31.5 µs (4 MHz / 126) 111 1111: 31.75 µs (4 MHz / 127)
Options	SENT_TICK = 0 recommend for standard SENT specification. Additional options are available to increase or decrease the communication rate. Requires PWM_MODE = 0 for use.
Examples	–

SENT_UPDATE: Address 0x1E, bits 7:5

Function	Pause Pulse and Frame Rate Pause pulse usage and message frame rate.
Syntax	Quantity of Bits: 3
Related Commands	SENT_LOVAR, PWM_MODE
Values	000: No Pause pulse; new frame immediately follows previous frame (Default) 001: Pause pulse used for minimum constant frame rate (Length of other message sections, plus length of Pause Pulse nibble, is constant. For the maximum message length, Pause pulse information state is the minimum size of 12 ticks.) 010: Pause pulse used for constant frame rate, synchronized with A1343 internal update rate. (Handshaking occurs such that the Synchronization and Calibration nibble starts immediately after the next new data word is ready.) 011: Pause pulse held indefinitely until receipt of trigger pulse (OUT pulled low) from the controller, data latched after output released and message is sent. 100: Pause pulse held indefinitely until receipt of trigger pulse (OUT pulled low) from the controller, data latched immediately and sent when output is released. 101, 110, 111: Same function as 000.
Options	For SENT_UPDATE = 3 or 4, the Pause pulse has a fixed low time regardless of the SENT_LOVAR setting. Requires PWM_MODE = 0 for use.
Examples	–

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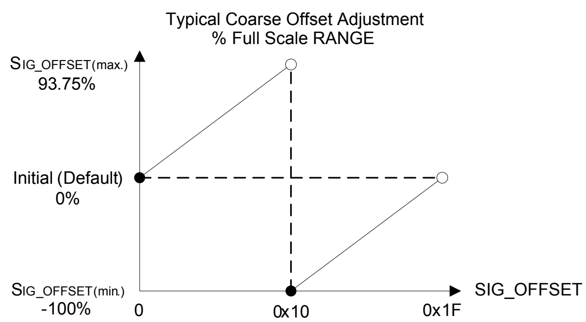
SIG_OFFSET: Address 0x1C, bits 8:4

Function	Adjusts the B_{IN} level at which RANGE is centered. The offset values are expressed in terms of a percentage of the full scale input of the selected RANGE determined by SENS_COARSE. Note: This is a coarse analog adjustment parameter to center in the sampled input signal within the range of the Analog-to-Digital converter. The specified step size and adjustment range is typical and the actual offset values may vary slightly.
Syntax	Quantity of bits: 5 Code stored in two's complement format.
Related Commands	SENS_COARSE, TC1_OFFSET
Values	
Options	The RANGE is centered at 0 G, default, if this parameter is not set.
Examples	Application Target: Adjust the input range for a maximum input signal of 0 to 1000 G, with a centerpoint at +500 G. Selected RANGE = ±500 G (SENS_COARSE = 0, ≈ 0.1 %FSO / G) establishes the full-scale input RANGE of 1000 G. Selected SIG_OFFSET = 0x18 (code 24, –50 %FSI). SIG_{OFFSET} = (Centerpoint (G) / Full Scale Input (G) - 1) × 100 = (500/1000 – 1) × 100 = –50 %FSI.

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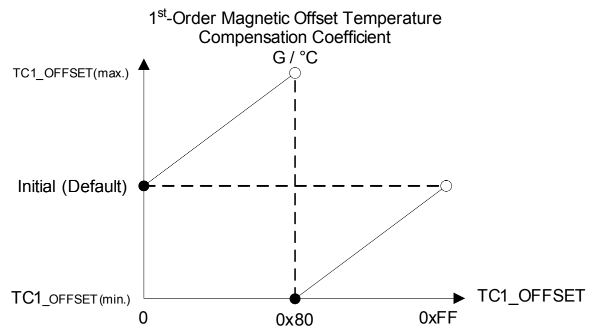
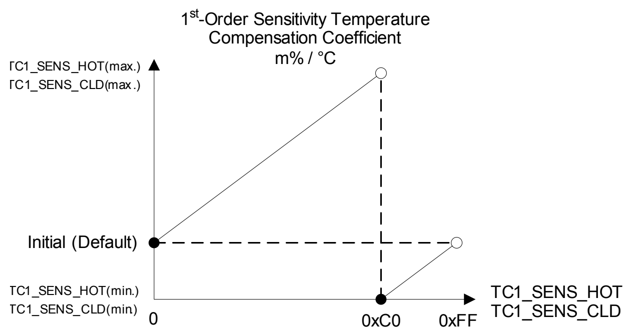
TC1_OFFSET: Address 0x09, bits 7:0

Function	1st-Order Magnetic Offset Temperature Compensation coefficient See Temperature Compensation section for more details.
Syntax	Quantity of bits: 8 Code stored in two's complement format.
Related Commands	SENS_COARSE, TC1_SENS_CLD, TC1_SENS_HOT, TC2_SENS_CLD, TC2_SENS_HOT
Values	
Options	This parameter scales with RANGE selection. The following equation is used to adjust the step size for the selected RANGE: $STEP_{TC1\_OFFSET}$ = $STEP_{TC1\_OFFSET}$ (default, G/LSB) × Selected RANGE (G) / RANGE (Default, G). The values for TC1_OFFSET (min) and TC1_OFFSET (max) also scale accordingly.
Examples	Application Target: Required offset drift = 0 G/°C. Selected RANGE = ±250 G (SENS_COARSE = 6) Output offset drift prior to 1st-order offset temperature compensation: 0.048 G/°C Selected TC1_OFFSET = 0xF3 (–0.048 G/°C). Note: TC1_OFFSET step size adjusted for the selected RANGE is: 0.0076 × (±250 G) / (±500 G) = 0.0038 G

TC1_SENS_CLD: Address 0x09, bits 15:8
TC1_SENS_HOT: Address 0x09, bits 23:16

Function	1st-Order Sensitivity Temperature Coefficient. Refer to the Temperature Compensation section for more details. Two different parameters are set, one for increasing values relative to T_A = 25°C, and the other for decreasing values, as follows: • TC1_SENS_HOT: ΔT_A (from 25°C) > 0 • TC1_SENS_CLD: ΔT_A (from 25°C) < 0
Syntax	Quantity of bits: 8 (each parameter) Code stored in shifted two's complement format.
Related Commands	TC2_SENS_HOT, TC2_SENS_CLD
Values	
Options	The factory-programmed default, $TC_{SENSinit}$, is used if neither these parameters, nor the TC2_SENS_HOT, TC2_SENS_CLD parameters, are set.
Examples	–

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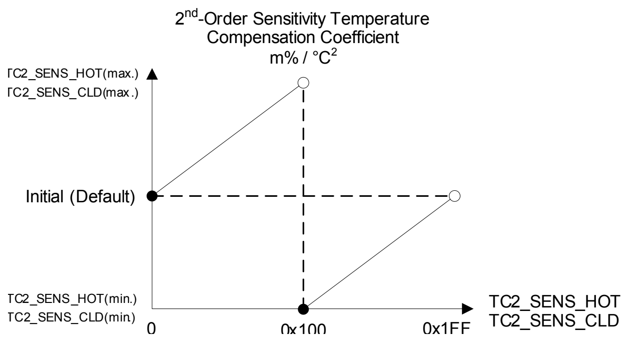
TC2_SENS_CLD: Address 0x08, bits 14:6
TC2_SENS_HOT: Address 0x08, bits 23:15

Function	2nd-Order Sensitivity Temperature Coefficient. Refer to Temperature Compensation section for more details. Two different parameters are set, one for increasing values relative to T_A = 25°C, and the other for decreasing values, as follows: • TC2_SENS_HOT: ΔT (from 25°C) > 0 • TC2_SENS_CLD: ΔT (from 25°C) < 0
Syntax	Quantity of bits: 9 (each parameter) Code stored in two's complement format.
Related Commands	SENS_MULT, TC1_SENS_HOT, TC1_SENS_CLD
Values	
Options	The factory-programmed default, $TC_{SENSinit}$, is used if neither these parameters, nor the TC1_SENS_HOT, TC1_SENS_CLD parameters, are set.
Examples	–

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DEFINITIONS OF TERMS

GENERAL PROGRAMMING

PROGRAMMING STEP SIZE

The average change in a parameter value for each bit set in the programming range for that parameter. The step size for a single device is determined using the following calculation:

$$Step_X = \frac{X_{maxcode} - X_{mincode}}{2^n - 1} \quad (5)$$

where

n is the quantity of available programming bits in the range,

$2^n - 1$ is the value of the maximum programming code in the range,

$X_{maxcode}$ is the value resulting from the maximum programming code in the range, and

$X_{mincode}$ is the value resulting from minimum programming code in the range.

PROGRAMMING RANGE

The values of a programmable parameter that are within a central range bounded by the distributions of the values that could result from programming the minimum and maximum codes available for that parameter (see Figure 22). Because the endpoints of a programmable range have normal distributions, they are excluded from the range of values. The limits of the range are indicated by the minimum and maximum values in the Operating Characteristics table. For customer-programmable parameters, the typical default initial value lies within the programming range, and usually serves as the reference point for setting value ranges.

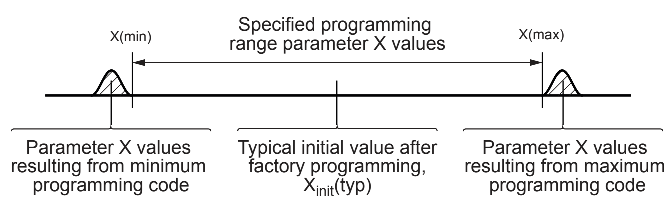

Figure 22: Definition of a Programming Range

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FULL SCALE INPUT, FSI

The range of the applied magnetic field processed by the device, and is used in determining SIG_OFFSET.

FULL SCALE OUTPUT, FSO

The available output range of the A1343 for a given applied input magnetic field. When configured for PWM output mode, the device has a FSO of 2% to 98% duty cycle. When configured for SENT output mode, the device has an FSO of 0 to 4095 LSBs. See Figure 23.

TIMING

POWER-ON TIME, T_{PO}

The time required for device output to begin the transmission of either the first valid output message frame (SENT mode) or the first valid duty cycle (PWM mode), after the power supply has reached its minimum specified operating voltage, V_{CC}(min). When the supply is ramped to its operating voltage, the device requires a finite time to power internal circuits before supplying a valid output value.

SIGNAL RESPONSE TIME

Typically Signal Response Time is defined as propagation delay, t_{SDLY}, plus length of the SENT/PWM message. However if filter bandwidth is chosen such that the corresponding internal output update rate (see BW parameter in EEPROM) is slower than the output digital message length, it might take a couple of output messages to update the user.

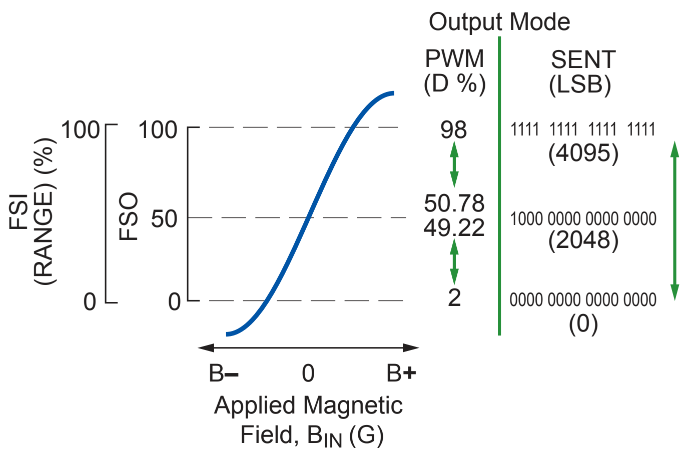

Figure 23: Full Scale Input (FSI) and Full Scale Output (FSO)

QUIESCENT FIELD BASELINE

COARSE OFFSET COMPENSATION

Customer-programmable biasing of the center of the Magnetic Input Signal Range, SENS_COARSE, in order to optimize the device response to variances. Set by EEPROM parameter SIG_OFFSET.

QUIESCENT OUTPUT, QOUT

The output value in the quiescent state (when no magnetic field is applied, B_{IN} = 0 G).

QUIESCENT OUTPUT RANGE

The central portion of the programmable range for Quiescent Output, QOUT. This range lies within the QOUT limits. The Quiescent Output, QOUT, can be customer-programmed (EEPROM parameters SIG_OFFSET and QOUT_FINE) around its typical value, which is 0 LSB (SENT mode) or 50% duty cycle (PWM mode). Refer to the Programming Range definition in this section for a conceptual explanation of how value distributions and ranges are related.

QUIESCENT OUTPUT PROGRAMMING STEP SIZE, $STEP_{QOUT\_FINE}$

The average change in Quiescent Output, QOUT, for each bit set in the programming range for QOUT_FINE. Refer to the Programming Step Size definition in this section for a conceptual explanation of how values and programming codes are related.

QUIESCENT OUTPUT DRIFT THROUGH TEMPERATURE RANGE

Due to internal component tolerances and thermal considerations, the temperature coefficient used to determine Quiescent Output may drift from its typical initial value, $QOUT_{init}$, when changes occur in the operating ambient temperature, T_A. For purposes of specification, the Quiescent Output Drift Through Temperature Range, $\Delta QOUT_{(\Delta T)}$, is defined as:

$$\Delta QOUT_{(\Delta T)} = QOUT_{(TA)} - QOUT_{(25°C)} \quad (6)$$

where $QOUT_{(TA)}$ is the QOUT at a given T_A and $QOUT_{(25°C)}$ is the QOUT at a T_A of 25°C. Note that $\Delta QOUT_{(\Delta T)}$ should be calculated using actual measured values, rather than target values used when programming.

CLAMP PROGRAMMING RANGE

The range of values that device digital processing is customer-programmed (EEPROM parameters CLAMP_HIGH and CLAMP_LOW) to optimize what segment of the processed Full Scale Input is scaled to the Full Scale Output. This determines

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the extent of truncation of the high and low peaks of the output of the Digital Signal Processing stage before input to the digital-to-analog converter in the output stage. (Note: This function is not related to the supply Zener clamp, for $V_{ZSUPPLY}$, and the output Zener clamp, for V_{ZOUT}, which are hardware overvoltage protection features.)

CLAMP PROGRAMMING STEP SIZE, $STEP_{CLPX}$

Refer to the definition of Programming Step Size in this section for a conceptual explanation.

DEVICE RESPONSE TO MAGNETIC FIELD

SENSITIVITY, SENS

The proportion of the output voltage to the magnitude of the applied magnetic field. This proportionality is specified as the Sensitivity, Sens (ΔLSB/G for SENT mode, ΔD/G for PWM mode), and is effectively the gain of the device.

An individual A1343 device may be *unipolar*, and respond to the presence of either a south (positive) polarity magnetic field, or a north (negative) polarity magnetic field (but not both). Or it may be *bipolar*, and respond to both polarities. If responsive to a south field, a south field opposite and perpendicular to the branded face of the package will increase the output from its quiescent value toward the maximum output limit. If responsive to a north field, a north field opposite and perpendicular to the branded face of the package will decrease the output from its quiescent value.

For bipolar configurations, Sensitivity is defined as:

$$\text{Sens} = \frac{OUT_{(BPOS)} - OUT_{(BNEG)}}{B_{POS} - B_{NEG}} \quad , \qquad (7)$$

and for unipolar configurations (south field responsive) as:

$$\text{Sens} = \frac{OUT_{(BPOS)} - OUT_{(Q)}}{B_{POS}} \quad , \qquad (8)$$

where B_{POS} and B_{NEG} are two magnetic fields with the indicated opposite polarities.

SENSITIVITY PROGRAMMING RANGE

The central portion of the programmable range for Sensitivity, SENS. This range lies within the Sens limits (Sensitivity Programming Range digital subsystem customer programming): SENS_OUT(min) and SENS_OUT(max). The Sensitivity, Sens, can be customer-programmed (EEPROM parameter SENS_MULT) around its typical value, $Sens_{init}$, which is 0.1% of Full Scale Input. Refer to the Programming Range definition in this section for a conceptual explanation of how value distributions and ranges are related.

SENSITIVITY PROGRAMMING STEP SIZE, $STEP_{SENS\_MULT}$

Refer to the definition of Programming Step Size in this section for a conceptual explanation.

DEVICE ACCURACY

MAGNETIC OFFSET DRIFT THROUGH TEMPERATURE RANGE

Due to internal component tolerances and thermal considerations, the temperature coefficient used to determine magnetic offset may drift from its typical initial value, and the expected value after customer programming (EEPROM parameter TC1_OFFSET) when changes occur in the operating ambient temperature, T_A. For purposes of specification, the Sensitivity Drift Through Temperature Range, $\Delta B_{OFF(TC)}$, is defined as:

$$\Delta B_{OFF(TC)} = \frac{B_{OFF(TA)} - B_{OFFEXPECTED(TA)}}{B_{OFFEXPECTED(TA)}} \times 100\ (\%) \qquad (9)$$

where $B_{OFF(TA)}$ is the actual magnetic offset at the current ambient temperature, and $B_{OFFEXPECTED(TA)}$ is the magnetic offset calculated based on programmed parameters.

SENSITIVITY DRIFT THROUGH TEMPERATURE RANGE

Due to internal component tolerances and thermal considerations, the temperature coefficient used to determine Sensitivity may drift from its typical initial value, $Sens_{TCinit}$, and the expected value after customer programming (EEPROM parameters TC1_SENS_CLD, TC1_SENS_HOT, TC2_SENS_CLD, TC2_SENS_HOT) when changes occur in the operating ambient temperature, T_A. For purposes of specification, the Sensitivity Drift Through Temperature Range, $\Delta Sens_{TC}$, is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{EXPECTED(TA)}}{Sens_{EXPECTED(TA)}} \times 100\ (\%) \qquad (10)$$

where $Sens_{TA}$ is the actual Sens at the current ambient temperature, and $Sens_{EXPECTED(TA)}$ is the Sens calculated based on programmed parameters.

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LINEARITY SENSITIVITY ERROR

The A1343 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic field strengths, B1 and B2. Ideally, the sensitivity of a device is the same for both field strengths, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity error is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{Bx}}{Sens_{Bx/2}}\right) \times 100\ (\%) \quad (11)$$

$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{-Bx}}{Sens_{-Bx/2}}\right) \times 100\ (\%)$$

where:

$$Sens_{Bx} = \frac{|OUT_{(Bx)} - OUT_{(Q)}|}{B_x} \quad (12)$$

and B_X and $-B_X$ are positive and negative magnetic fields.

Final Linearity Sensitivity Error (Lin_{ERR}) is the maximum value of the absolute positive and absolute negative linearization errors. Note that unipolar devices only have positive linearity error (Lin_{ERRPOS}).

SYMMETRY SENSITIVITY ERROR

The magnetic sensitivity of an A1343 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{OUT_{(+B)} - OUT_{(Q)}}{OUT_{(Q)} - OUT_{(+B)}}\right) \times 100\ (\%) \quad (13)$$

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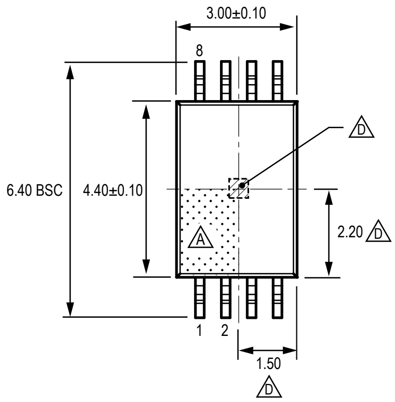
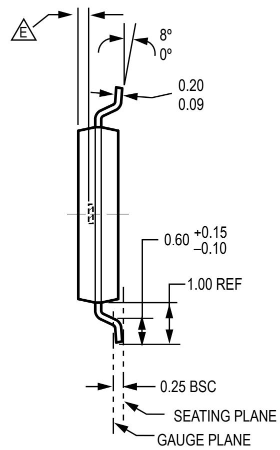
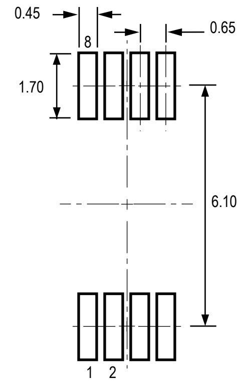
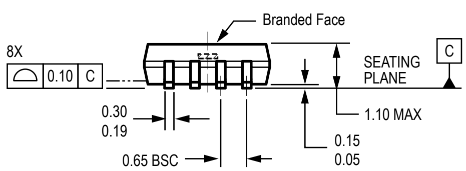
PACKAGE LE, 8-PIN TSSOP

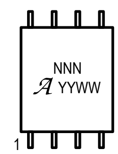






B PCB Layout Reference View





C Standard Branding Reference View

N = Last 3 digits of device part number
𝒜 = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
Branding scale and appearance at supplier discretion

For Reference Only; not for tooling use (reference MO-153 AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-8M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Branding scale and appearance at supplier discretion

D Hall element, not to scale

E Active Area Depth 0.36 mm REF

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DOCUMENT REVISION HISTORY

Revision	Change	Pages	Responsible	Date
– (was 1.0)	Created from DS_A1343_GS_R22Final_r1d0 Jan. 23, 2013 Mag. Char. updated: B_{INinit}, $B_{INOFFSET}$, $Sens_{init}$, $OUT_{CLP(H)init}$, $OUT_{CLP(L)init}$ Mag Char. added: $SENT_{CFG(tick)init}$, $SENT_{CFG(fixed)init}$, $SENT_{CFG(update)init}$, $SENT_{CFG(data)init}$ Prog. Char. updated: TC1_OFFSET, StepTC1_OFFSET	All 5 5 7	J. Lapomardo	February 8, 2013
1 (was 1.0)	EC table update: TC1_OFFSET Prog. Char. update: TC1_OFFSET	7 44	J. Lapomardo	February 14, 2013
2 (was 1.1)	Updated Description to indicate open drain output Added Low Voltage Detection Feature Electrical Characteristics: Supply Voltage conditions Replaced Undervoltage Lockout with Low Voltage Detection Added Power-On Reset Operating Overvoltage Lockout and Low Voltage Detection Updated text to match device behavior with Low Voltage Detection Feature Table 7. EEPROM Register Map of Customer-Programmable Parameters Added LVD_DIS reg. 0x1C bit 9 EEPROM Customer-Programmable Parameter Reference Added LVD_DIS Updated Typical Application circuit to show external pull-up resistor on V_{OUT}	1 4 4 4 15 32 36 16	J. Lapomardo	June 27, 2013
3 (was 1.2)	Electrical Characteristics Updated: POR_{LOW} , POR_{HIGH} Magnetic Characteristics Updated: $\Delta Sens_{init}$, $\Delta OUT_{(Q)init}$ Programmable Characteristics Added: Sensitivity Drift Over Lifetime, $\Delta Sens_{LIFE}$ Updated: $\Delta Sens_{PKG}$	4 5 8	J. Lapomardo	September 24, 2013
4 (was 1.3)	Fixed typographical errors in Output Serial Protocol and Data Nibble Format.	26, 30	J. Lapomardo	February 26, 2014
5	Increased maximum output current limit Corrected BW settings Corrected Operating Overvoltage Lockout and Low Voltage Detection Corrected Figure 7	2,4 4, 33 15 13	J. Lapomardo	March 10, 2016
6	Corrected Selection Guide	2	J. Lapomardo	May 3, 2016
7	Updated Table 6: SENT Message Frame Section Definitions, CRC Function description.	30	N. Kozomora	May 25, 2017
8	Minor editorial updates	All	R. Couture	June 20, 2018
9	Minor editorial updates	All	R. Couture	August 13, 2019
10	Updated Features and Benefits	1	J. Hollins	October 22, 2019

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