

## EA OPTICAL MODULATOR DRIVER, DC - 20 GHz



### Typical Applications

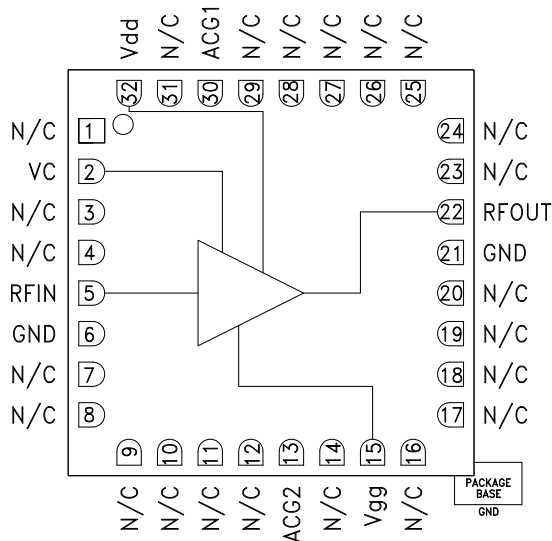
The HMC871LC5 is ideal for:

- SONET OC-192 & SDH-STM-64 Transmission Systems
- 10 GbE Transmitters
- 10 Gbps VSR Modules
- Pre-driver for 40 Gbps DQPSK Modules
- Broadband Gain Block for Test & Measurement Equipment

### Features

- Wide Supply Range from 5V to 8V
- Adjustable Output Amplitude up to 4 Vp-p
- Low Additive RMS Jitter, <300 fs
- Low DC Power Consumption, 0.25W for  $V_{out} = 2.5$  Vp-p at  $V_{dd} = 5V$
- Cross Point Adjustment
- 32 Lead 5x5mm SMT Package: 25mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC871LC5 is a GaAs MMIC PHEMT Distributed Driver Amplifier packaged in a leadless 5x5mm surface mount package. The amplifier operates between DC and 20 GHz and provides 15 dB of gain. The output swing cross point is adjustable and saturated output swing is 4Vp-p. Gain flatness is excellent at  $\pm 0.5$  dB as well as very low additive RMS jitter of 300 fs for 10 Gbps operation. The HMC871LC5 provides VSR and Gigabit Ethernet designers with scalable power dissipation for varying output drive requirements (<0.25W at  $V_{out} = 2.5$  Vp-p and <0.6W at  $V_{out} = 4$  Vp-p). The HMC871LC5 has a very wide supply ( $V_{dd}$ ) operating range from +5V to +8V and the I/Os are internally matched to 50 Ohms.

### Electrical Specifications, $T_A = +25^\circ C$ , $V_{dd} = 8V$ , $VC = 0.5V$ , $I_{dd} = 75mA^*$

Parameter	Conditions	Min.	Typ.	Max.	Units
Gain	Frequency = 1 - 8 GHz	13	16		dB
	Frequency = 8 - 16 GHz	12	15		dB
	Frequency = 16 - 20 GHz	10	13.5		dB
Small Signal Bandwidth	3-dB cutoff		17.5		GHz
Input Return Loss	Frequency = 1 - 10 GHz		20		dB
	Frequency = 10 - 20 GHz		10		dB
Output Return Loss	Frequency = 1 - 10 GHz		15		dB
	Frequency = 10 - 20 GHz		10		dB
Gain Variation Over Temperature	Frequency = 1 - 10 GHz		0.016	0.022	dB/ $^\circ C$
	Frequency = 10 - 20 GHz		0.025	0.36	dB/ $^\circ C$
Group Delay Variation	Frequency = 1 - 12 GHz		$\pm 15$		ps
Saturated Output Power ( $P_{sat}$ )	Frequency = 1 - 12 GHz		18		dBm
	Frequency = 12 - 20 GHz		16		dBm

\* Adjust  $V_{gg}$  between -1V to 0V to achieve  $I_{dd} = 75$  mA typical.

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### Electrical Specifications, $T_A = +25^\circ\text{C}$ , $V_{dd} = 8\text{V}$ , $V_C = 0.5\text{V}$ , $I_{dd} = 75\text{mA}^*$ Continued

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Power for 1 dB Compression (P1dB)	Frequency = 1 - 12 GHz	14	16.5		dBm
	Frequency = 12 - 20 GHz	11	14		dBm
Rise Time [1]	20% - 80%		20		ps
Fall Time [1]	20% - 80%		19		ps
Additive RMS Jitter [2]				300	fs
Supply Current (I <sub>dd</sub> ) (V <sub>gg</sub> = -0.7V Typ.)			75		mA
Bias Current Adjust (V <sub>gg</sub> )		-2		0	V
Output Voltage Adjust (V <sub>C</sub> )		0		2	V

[1] Data input = 22.5 Gbps NRZ PRBS 2<sup>23</sup>-1 pattern, 0.5 V<sub>p-p</sub>.

[2] RMS jitter is calculated with 22.5 Gbps 10101... pattern.

\* Adjust V<sub>gg</sub> between -1V to 0V to achieve I<sub>dd</sub> = 75mA typical.

### Electrical Specifications, $T_A = +25^\circ\text{C}$ , $V_{dd} = 5\text{V}$ , $V_C = 0.5\text{V}$ , $I_{dd} = 50\text{mA}^*$

Parameter	Conditions	Min.	Typ.	Max.	Units
Gain	Frequency = 1 - 8 GHz	11.5	14.5		dB
	Frequency = 8 - 16 GHz	11	14		dB
	Frequency = 16 - 20 GHz	8	11.5		dB
Small Signal Bandwidth	3-dB cutoff		18.5		GHz
Input Return Loss	Frequency = 1 - 10 GHz		15		dB
	Frequency = 10 - 20 GHz		10		dB
Output Return Loss	Frequency = 1 - 10 GHz		10		dB
	Frequency = 10 - 20 GHz		10		dB
Gain Variation Over Temperature	Frequency = 1 - 10 GHz		0.017	0.024	dB/°C
	Frequency = 10 - 20 GHz		0.024	0.034	dB/°C
Group Delay Variation	Frequency = 1 - 12 GHz		±15		deg
Saturated Output Power (P <sub>sat</sub> )	Frequency = 1 - 12 GHz		14		dBm
	Frequency = 12 - 20 GHz		11		dBm
Output Power for 1 dB Compression (P1dB)	Frequency = 1 - 12 GHz	8	11		dBm
	Frequency = 12 - 20 GHz	4	8		dBm
Rise Time [1]	20% - 80%		20		ps
Fall Time [1]	20% - 80%		20		ps
Additive RMS Jitter [2]				300	fs
Supply Current (I <sub>dd</sub> ) (V <sub>gg</sub> = -0.8V Typ.)			50		mA
Bias Current Adjust (V <sub>gg</sub> )		-2		0	V
Output Voltage Adjust (V <sub>C</sub> )		0		2	V

[1] Data input = 22.5 Gbps NRZ PRBS 2<sup>23</sup>-1 pattern, 0.5 V<sub>p-p</sub>.

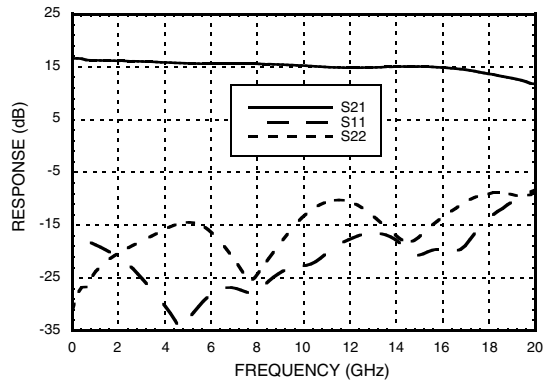
[2] RMS jitter is calculated with 22.5 Gbps 10101... pattern.

\* Adjust V<sub>gg</sub> between -1V to 0V to achieve I<sub>dd</sub> = 50mA typical.

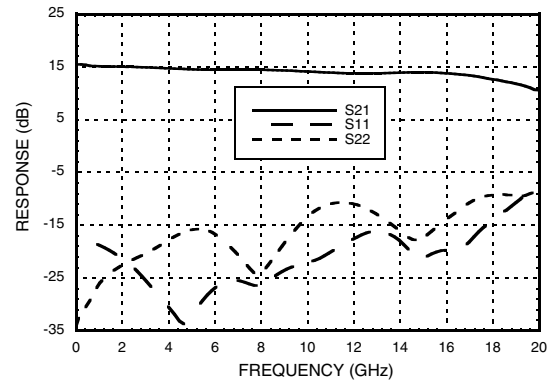


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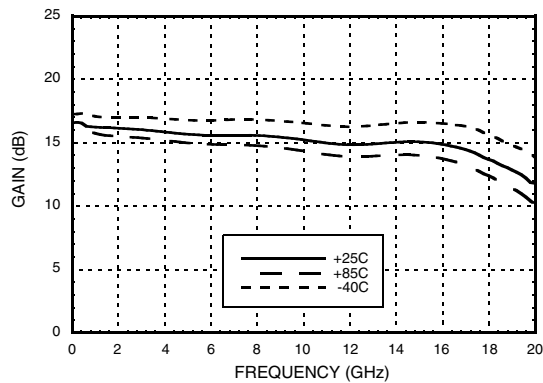
**Gain & Return Loss @ Vdd = 8V**



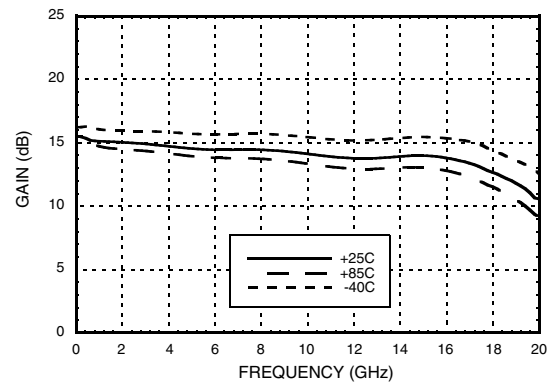
**Gain & Return Loss @ Vdd = 5V**



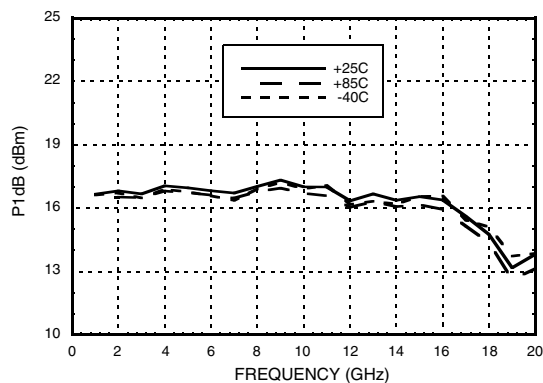
**Gain vs. Temperature @ Vdd = 8V**



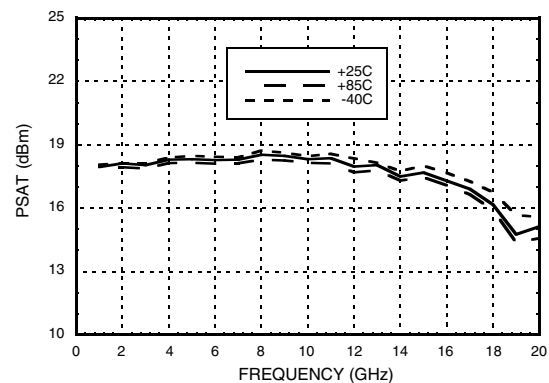
**Gain vs. Temperature @ Vdd = 5V**



**P1dB vs. Temperature @ Vdd = 8V**



**Psat vs. Temperature @ Vdd = 8V**



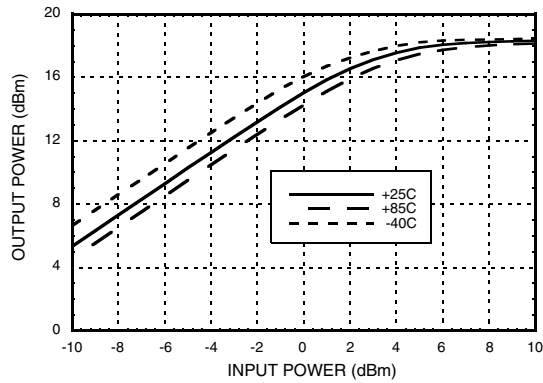
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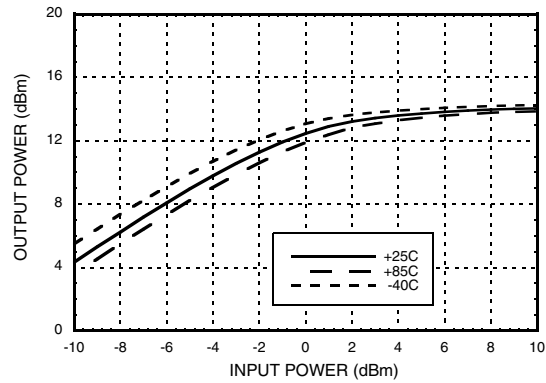


**EA OPTICAL MODULATOR DRIVER, DC - 20 GHz**

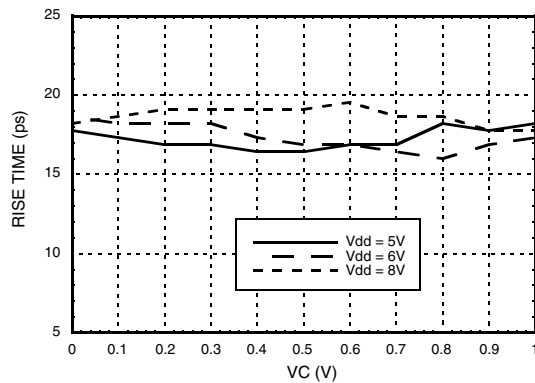
**Output Power vs. Input Power @ 10 GHz, Vdd = 8V**



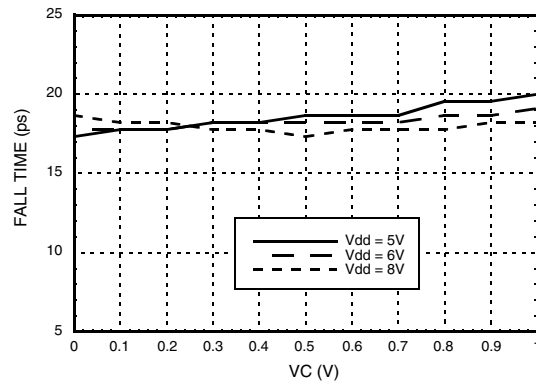
**Output Power vs. Input Power @ 10 GHz, Vdd = 5V**



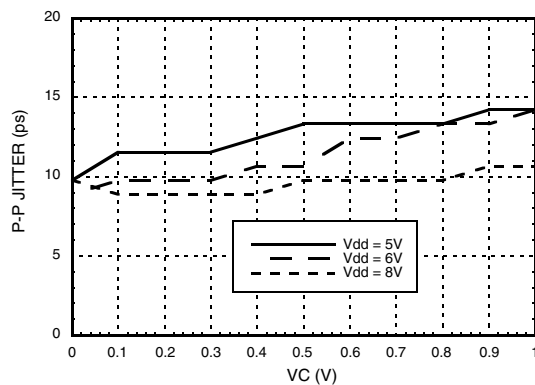
**Rise Time vs. Vdd @ 22.5 Gbps [2]**



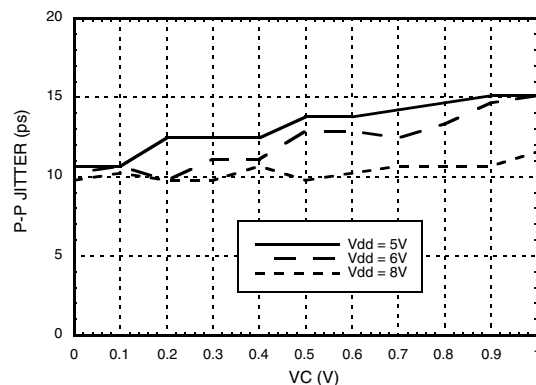
**Fall Time vs. Vdd @ 22.5 Gbps [2]**



**Peak-to-Peak Jitter vs. Vdd @ 11.25 Gbps [1]**



**Peak-to-Peak Jitter vs. Vdd @ 22.5 Gbps [2]**



[1] Data input = 11.25 Gbps NRZ PRBS 2<sup>23</sup>-1 pattern, 0.5 Vp-p.

[2] Data input = 22.5 Gbps NRZ PRBS 2<sup>23</sup>-1 pattern, 0.5 Vp-p.

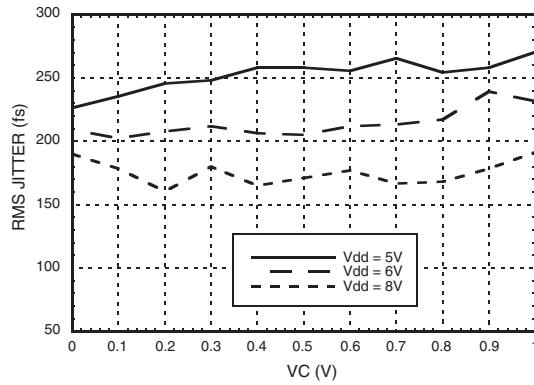
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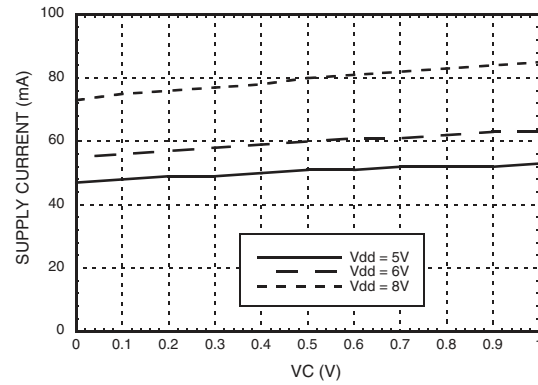


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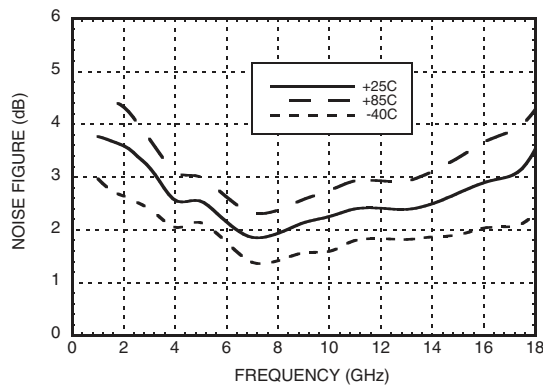
**RMS Jitter vs. Vdd @ 22.5 Gbps [4]**



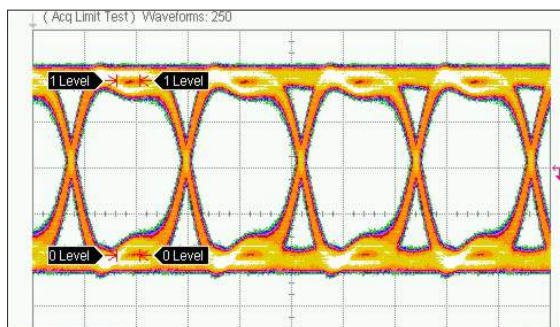
**Supply Current vs. Vdd @ 22.5 Gbps [3]**



**Noise Figure vs. Temperature @ Vdd = 8V**



**11.25 Gbps NRZ Output Eye Diagrams**



	Measurements			
	Current	Min	Max	Units
Jitter p-p	9.78 ps	7.11 ps	9.78 ps	V
Rise Time	19.6 ps	18.7 ps	19.6 ps	ps
Fall Time	19.6 ps	18.7 ps	19.6 ps	ps
Eye Amp	3.03 V	3.03 V	3.03 V	ps

Time scale: 40 ps/div  
Amplitude scale: 800 mV/div

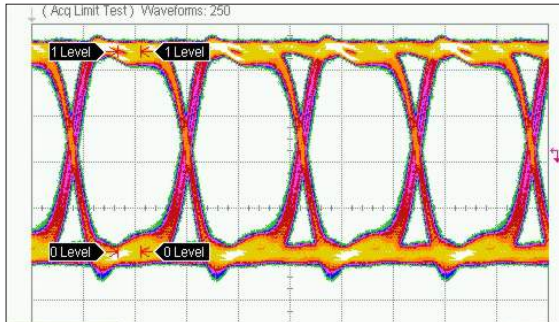
Vdd = 8V, Vin: 11.25 Gbps NRZ PRBS 2<sup>31</sup>-1, 0.5 Vp-p  
Vout: 3.03Vp-p

[1] Data input = 11.25 Gbps NRZ PRBS 2<sup>23</sup>-1 pattern, 0.5 Vp-p. [3] Data input 22.5 Gbps NRZ PRBS 2<sup>23</sup>-1 pattern, 0.5 Vp-p.  
[2] Source jitter was not de-embedded [4] RMS jitter is measured with 22.5 Gbps 10101...pattern



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### 11.25 Gbps NRZ Output Eye Diagrams

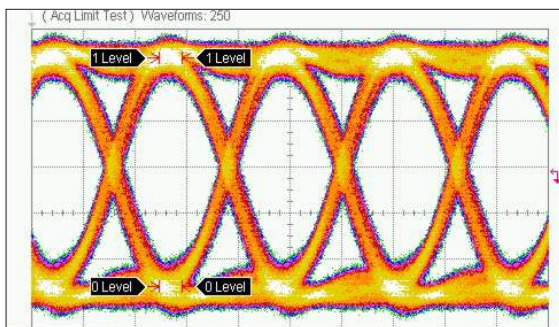


	Measurements			Units
	Current	Min	Max	
Jitter p-p	11.56 ps	8.89 ps	11.56 ps	V
Rise Time	16.9 ps	16.9 ps	16.9 ps	ps
Fall Time	16.9 ps	16.9 ps	17.8 ps	ps
Eye Amp	2.60 V	2.60 V	2.60 V	ps

Time scale: 40 ps/div  
Amplitude scale: 600 V/div

Vdd = 5V, Vin: 11.25Gbps NRZ PRBS 2<sup>31</sup>-1, 0.5V p-p,  
Vout: 2.60Vp-p

### 22.5 Gbps NRZ Output Eye Diagrams

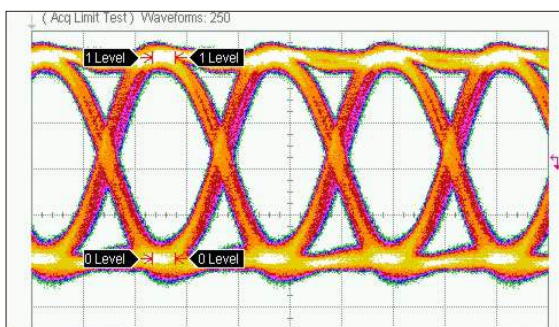


	Measurements			Units
	Current	Min	Max	
Jitter p-p	9.333 ps	8.000 ps	9.333 ps	V
Rise Time	17.78 ps	17.78 ps	18.67 ps	ps
Fall Time	17.78 ps	17.33 ps	18.67 ps	ps
Eye Amp	3.00 V	3.00 V	3.00 V	ps

Time scale: 20 ps/div  
Amplitude scale: 800 mV/div

Vdd = 8V, Vin: 22.5 Gbps NRZ PRBS 2<sup>31</sup>-1, 0.5 Vp-p  
Vout: 3.00Vp-p

### 22.5 Gbps NRZ Output Eye Diagrams



	Measurements			Units
	Current	Min	Max	
Jitter p-p	10.667 ps	8.889 ps	11.556 ps	V
Rise Time	16.00 ps	10.67 ps	16.00 ps	ps
Fall Time	17.78 ps	16.89 ps	17.78 ps	ps
Eye Amp	2.63 V	2.63 V	2.64 V	ps

Time scale: 20 ps/div  
Amplitude scale: 800 V/div

Vdd = 5V, Vin: 22.5Gbps NRZ PRBS 2<sup>31</sup>-1, 0.5V p-p,  
Vout: 2.63Vp-p







### Pin Descriptions

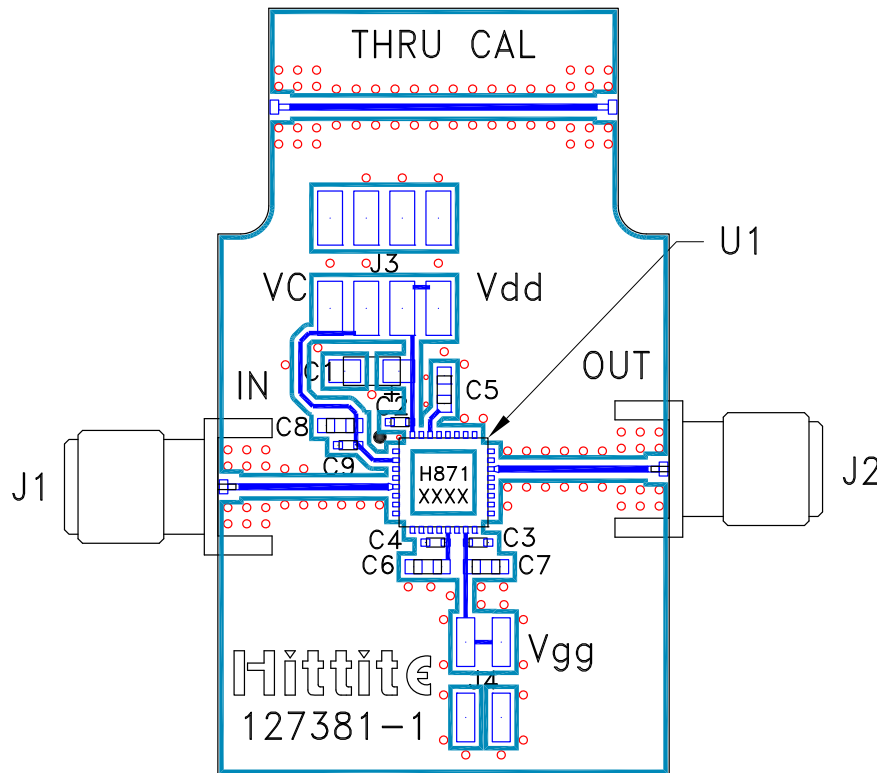
Pin Number	Function	Description	Interface Schematic
1, 3, 4, 7 - 12, 14, 16 - 20, 23 - 29, 31	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
2	VC	Output voltage swing adjust. +0.5V should be applied for nominal operation.	
5	RFIN	This pin is DC coupled and matched to 50 Ohms. DC blocking is required.	
6, 21	GND	These pins and exposed package base must be connected to RF/DC ground.	
13	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein.	
15	Vgg	Gate control for amplifier. Please follow "MMIC Amplifier Biasing Procedure" application note.	
22	RFOUT	This pin is DC coupled and matched to 50 Ohms. DC blocking is required.	
30	ACG1	Low frequency termination. Attach bypass capacitor per application circuit herein.	
32	Vdd	Power supply for the amplifier. External bypass capacitors are required.	





## EA OPTICAL MODULATOR DRIVER, DC - 20 GHz

### Evaluation PCB



### List of Materials for Evaluation PCB 127517 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3 - J4	2mm Molex Header
C1	4.7 $\mu$ F Capacitor, Tantalum
C2, C3	1000 pF Capacitor, 0402 Pkg.
C4, C9	100 pF Capacitor, 0402 Pkg.
C5	0.1 $\mu$ F Capacitor, 0603 Pkg.
C6	0.01 $\mu$ F Capacitor, 0603 Pkg.
C7	2.2 $\mu$ F Capacitor, 0603 Pkg.
C8	1000 pF Capacitor, 0603 Pkg.
U1	HMC871LC5, Modulator Driver
PCB [2]	127381 Evaluation PCB

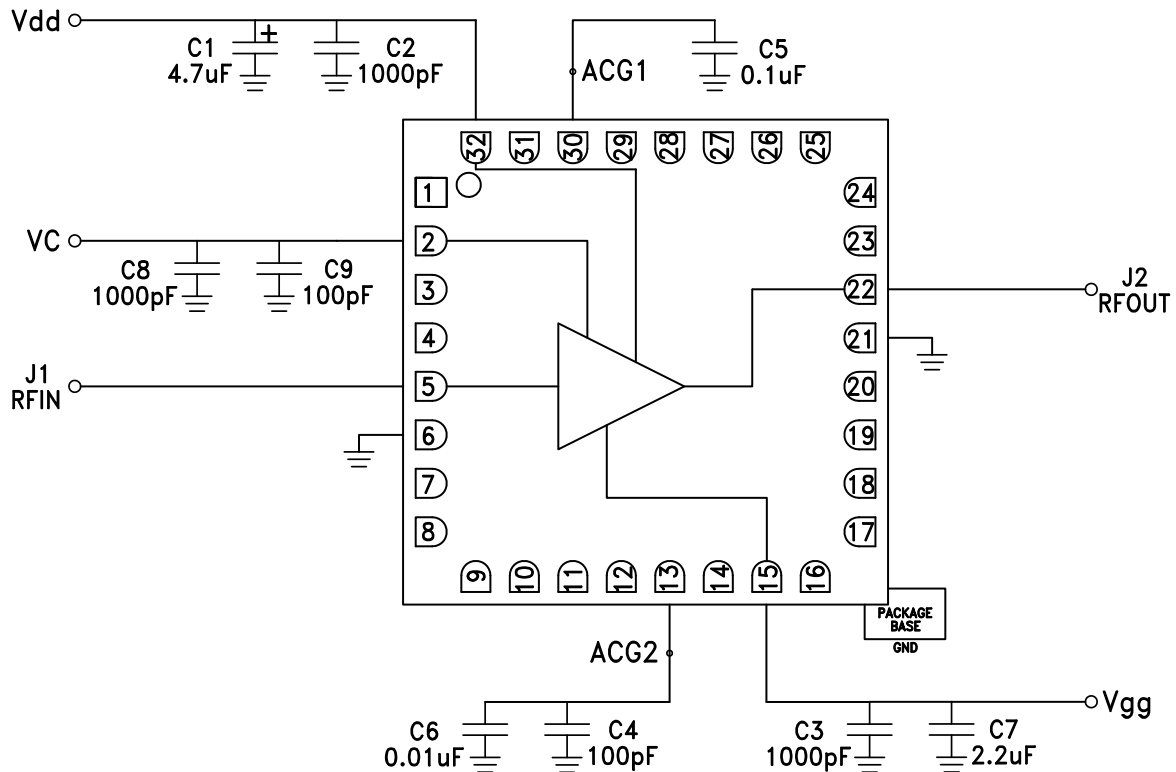
[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.



### Application Circuit



### Device Operation

These devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

The input to this device should be AC-coupled. To provide the typical 4Vp-p output voltage swing, a 0.5Vp-p AC coupled input voltage swing is required.

### Device Power Up Instructions

1. Ground the device, no RF signal applied to device
  2. Set Vgg to -2V (no drain current)
  3. Set VC to +0.5V (no drain current)
  4. Set Vdd to +5V or +8V (no drain current)
  5. Adjust Vgg for I<sub>dd</sub> = 50mA (V<sub>dd</sub> = 5V) or I<sub>dd</sub> = 75mA (V<sub>dd</sub> = 8V)
  6. Apply RF signal.
- Vgg may be varied between -1V and 0V to provide the desired eye crossing point percentage (i.e. 50% crosspoint) and a limited cross point control capability (±20%)

### Device Power Down Instructions

1. Reverse the sequence identified above in steps 1 through 6.