

SURMOUNT™ Silicon PIN Diode SPDT Switch 6 - 14 GHz



MASW-011021

Rev. V6

Features

- Specified from 8 - 12 GHz
- Low Insertion Loss
- High Isolation
- Low Parasitic Capacitance and Inductance
- Surface Mountable, Fully Monolithic Die
- Glass Encapsulated Construction
- 20 W Pulsed Power Handling⁴
- Silicon Nitride Passivation
- Polymer Scratch Protection
- RoHS* Compliant

Applications

- Aerospace & Defense

Description

This device is a SURMOUNT™ X-Band monolithic SPDT switch designed for high power, high performance applications. This surface mount chip-scale configuration is designed with minimal parasitics usually associated with hybrid MIC designs incorporating beam lead and/or bondable PIN diodes that require chip and wire assembly.

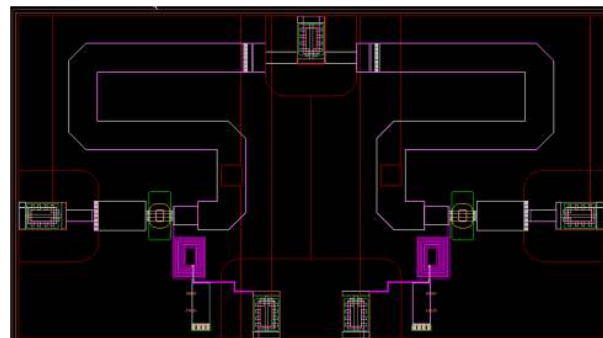
This device is fabricated using MACOMs' patented HMIC™ (Heterolithic Microwave Integrated Circuit) process, US Patent 5,268,310. This process allows the incorporation of silicon pedestals that form series and shunt diodes and/or vias by embedding them in low loss, low dispersion glass.

Selective backside metalization is applied producing a surface mount device. The topside is fully encapsulated with silicon nitride and has an additional polymer layer for scratch and impact protection. These protective coatings prevent damage to the junction and the anode airbridge during handling and assembly.

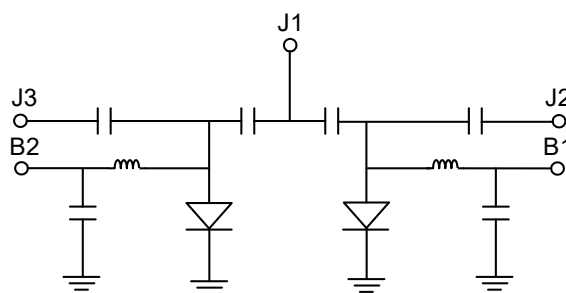
Ordering Information¹

Part Number	Package
MASW-011021-14010G	25 piece gel pack
MASW-011021-001SMB	Sample Test Board

1. Reference Application Note M513 for reel size information.



Functional Schematic



Pin Configuration²

Pin	Function
J1	RF C
J2	RF 1
J3	RF 2
B1	Bias 1
B2	Bias 2

2. The exposed pad centered on the chip bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Electrical Specifications: Bias: -5 V, +30 mA, T_A = 25°C, P_{IN} = 0 dBm, Z₀ = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	8 GHz	dB	—	0.70	0.85
	10 GHz			0.70	
	12 GHz			0.65	
Input to Output Isolation	8 GHz	dB	30	34	—
	10 GHz			36	
	12 GHz			34	
Return Loss	—	dB	—	15	—
IIP3	—	dBm	—	60	—
Voltage Rating ³	—	V	—	—	80
Switching Speed	10% to 90 % of detected RF signal driven by TTL compatible drivers	ns	—	130	—
CW Power Handling ⁴	-30 V, +30 mA	W	—	10	—

3. Maximum reverse leakage current in the shunt PIN diodes shall be 0.1 μA maximum.

4. 20 W up to 300 μs 40% Duty Cycle

Absolute Maximum Ratings^{5,6}

Parameter	Absolute Maximum
Bias Current @ +25°C	100 mA
DC Reverse Voltage	80 V
Junction Temperature	+175°C
Operating Temperature	-65°C to +125°C
Storage Temperature	-65°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.

6. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1A HBM devices.

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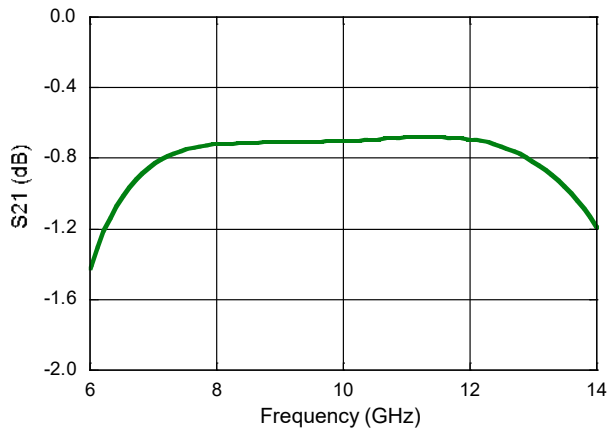


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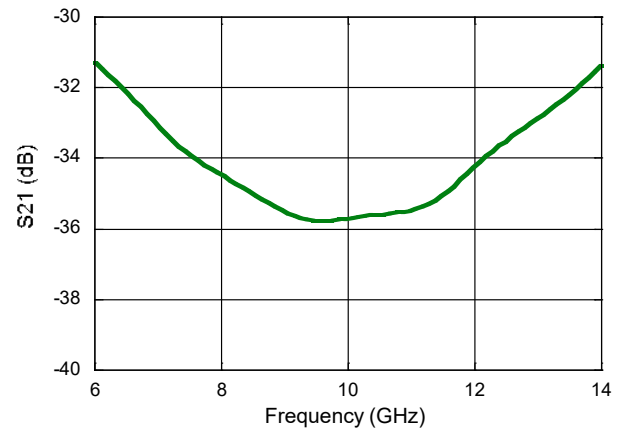
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Typical Performance Curves (on wafer probed results): Bias: -30 V, +30 mA

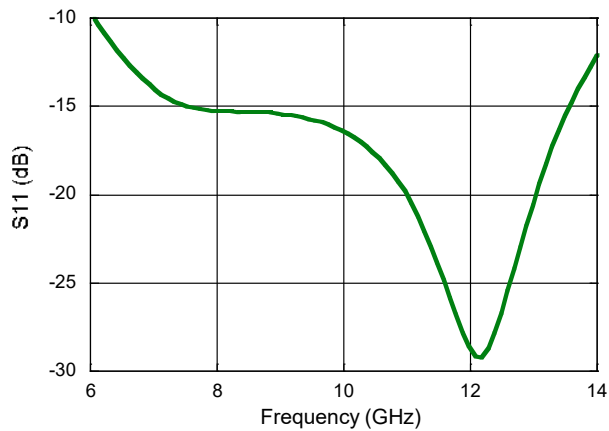
Insertion Loss



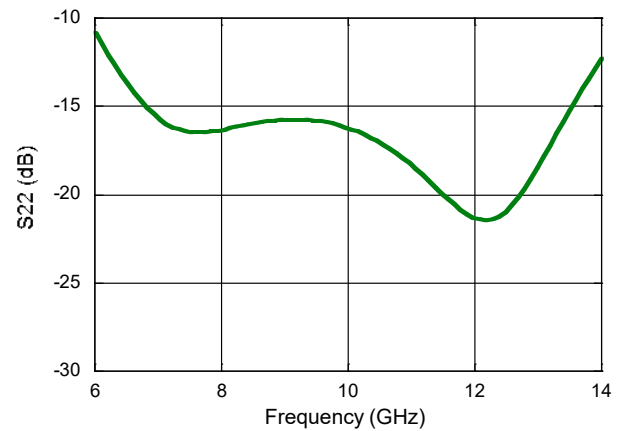
Isolation



Input Return Loss



Output Return Loss



Bias Control

Optimal operation is achieved by simultaneous application of negative DC voltage to the low loss switching arm and positive DC current to the isolating switching arm. Assuming 1 V voltage drop for the forward biased diode, the bias resistor value is determined using the formula $(V_{CC} - 1) / I_{bias}$.

In the low loss state, the diode is reverse biased with voltage. In the isolated state, the shunt diode is forward biased with current.

Minimum Reverse Bias Required:

At X-Band, with a 1:1 match, 5 V of negative reverse bias is required. With a 4:1 match, 10 V of negative reverse bias is required⁷.

However MACOM suggests a reverse bias voltage of -30 V to achieve optimal insertion loss.

7. R. Caverly and G. Hiller, "Establishing the Minimum Reverse Bias for a P-I-N Diode in a High Power Switch," IEEE Transactions on Microwave Theory and Techniques, Vol.38, No.12, December 1990

Driver Connections

Control Level (DC Currents and Voltages)		Condition of RF Output	
B1	B2	J1-J2	J1-J3
-30 V	+30 mA	Low Loss	Isolation
+30 mA	-30 V	Isolation	Low Loss

Handling Procedures

Attachment to a circuit board is made simple through the use of standard surface mount technology. Mounting pads are conveniently located on the bottom surface of these devices and are removed from the active junction locations. These devices are well suited for solder attachment onto hard and soft substrates. The use of 80Au/20Sn, or RoHS compliant solders is recommended. For applications where the average power is ≤ 1 W, conductive silver epoxy may also be used. Cure per manufacturers recommended time and temperature. Typically 1 hour at 150°C.

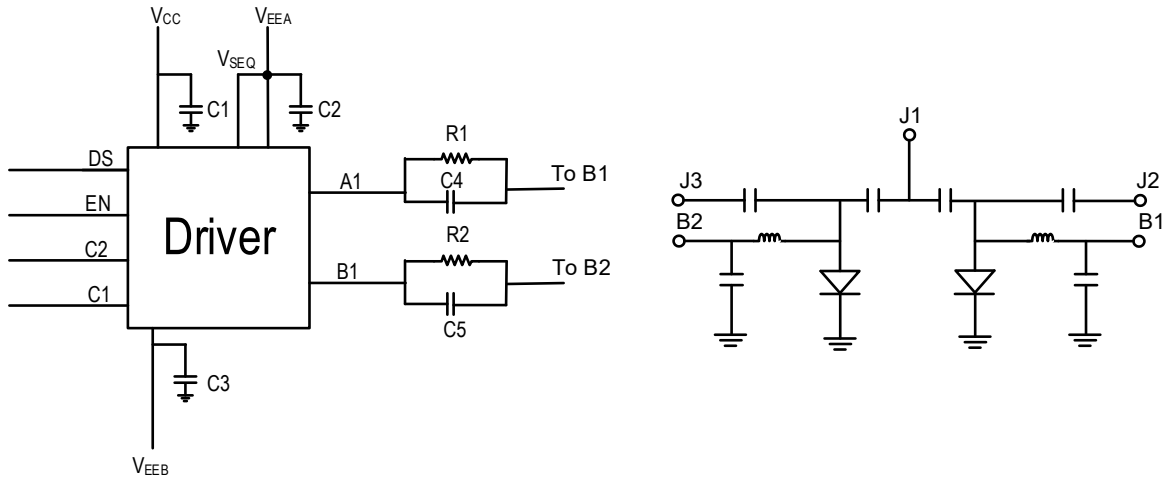
When soldering these devices to a hard substrate, a solder re-flow method is preferred. A vacuum tip pick-up tool and a force of 60 to 100 grams applied to the top surface of the device while placing the chip is recommended. When soldering to soft substrates, such as Duroid, it is recommended to use a soft solder at the circuit board to mounting pad interface to minimize stress due to any TCE mismatches that may exist. Position the die so that its mounting pads are aligned with the circuit board mounting pads. Solder reflow should not be performed by causing heat to flow through the top surface of the die to the back. Since the HMIC glass is transparent, the edges of the mounting pads can be visually inspected through the die after attachment is completed.

Typical re-flow profiles for Sn60/Pb40 and RoHS compliant solders is provided in Application Note M538, "Surface Mounting Instructions" and can be viewed MACOM website.

Sample Board

Samples test boards are available upon request.

MASW-011021 with MADR-011020 Driver Application Schematic



Parts List⁸

Part	Value
C1,C3	0.1 μ F
C2	47 pF
C4,C5	470 pF
R1,R2	130 Ω

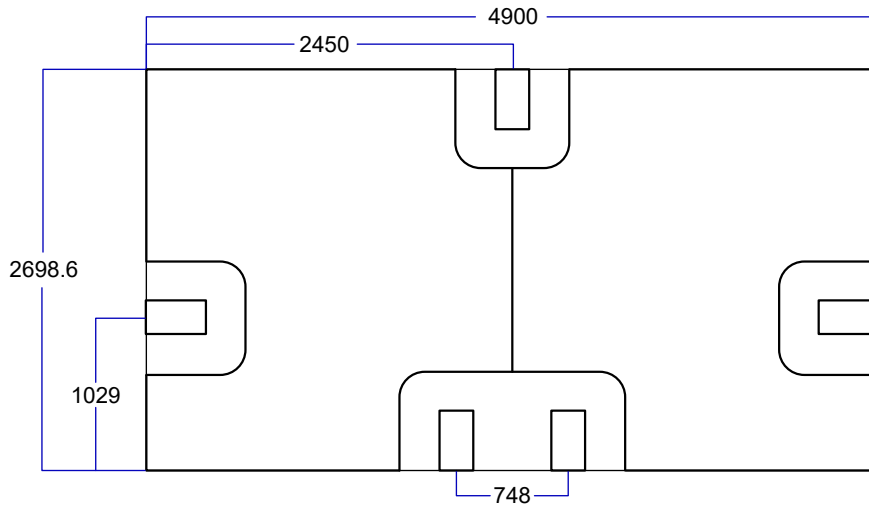
8. Resistor values calculated to provide 30 mA of bias current given $V_{CC} = 5$ V.

Minimum Reverse Bias Voltage⁹

Frequency (GHz)	DC Voltage (V)
6	8
8	6
10	5
12	4
14	3.5

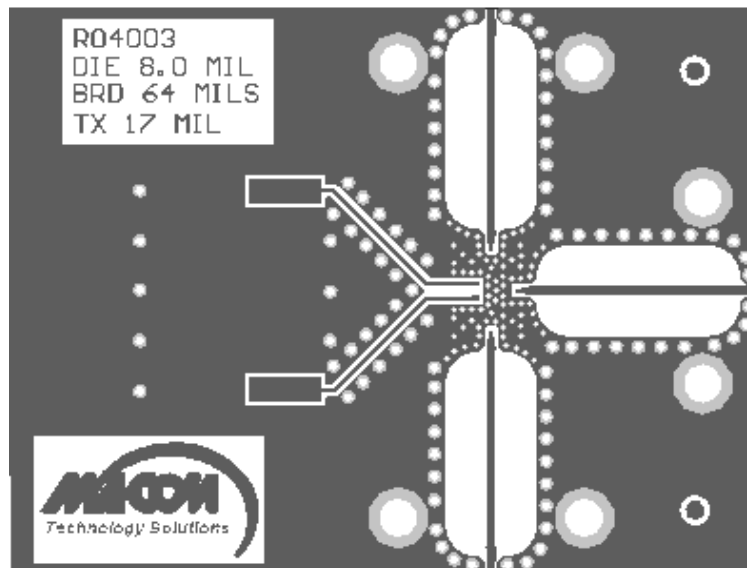
9. Minimum DC bias voltage to maintain low loss under 20 W of power with 1.5:1 VSWR.

Outline Drawing - Back Metal



All dimensions are in μm .

PWB for testing purposes



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