NVMFS5C677NL

[MOSFET](#) – Power, Single N-Channel
60 V, 15.0 mΩ, 36 A

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C677NLWF − Wettable Flank Option for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

ON Semiconductor®

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	15.0 mΩ @ 10 V	36 A
	21.5 mΩ @ 4.5 V	

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	60	V
Gate−to−Source Voltage		V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State / T_C = 25°C	I_D	36	A
	T_C = 100°C		25	
Power Dissipation $R_{\theta JC}$ (Note 1)	T_C = 25°C	P_D	37	W
	T_C = 100°C		18	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State / T_A = 25°C	I_D	11	A
	T_A = 100°C		7.8	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	T_A = 25°C	P_D	3.5	W
	T_A = 100°C		1.8	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs	I_{DM}	166	A
Operating Junction and Storage Temperature		T_J, T_{stg}	−55 to + 175	°C
Source Current (Body Diode)		I_S	31	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 2.87 A)		E_{AS}	65	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

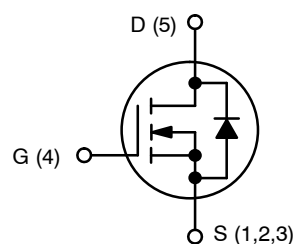| Parameter	Symbol	Value	Unit
Junction−to−Case – Steady State	$R_{\theta JC}$	4.1	°C/W
Junction−to−Ambient – Steady State (Note 2)	$R_{\theta JA}$	43	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
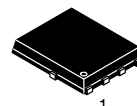3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

D (5)

G (4)

S (1,2,3)

N−CHANNEL MOSFET

**DFN5
(SO−8FL)
CASE 488AA
STYLE 1**

MARKING DIAGRAM

```
S        D    D
S   XXXXXX    D
S   AYWZZ
G            D
        D
```
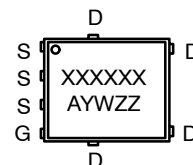
XXXXXX = 5C677L
    (NVMFS5C677NL) or
    677LWF
    (NVMFS5C677NLWF)
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMFS5C677NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				26		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C			10	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 25 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 10 A		12.5	15.0	mΩ
		V_{GS} = 4.5 V	I_D = 10 A		17.9	21.5	
Forward Transconductance	g_{FS}	V_{DS} =15 V, I_D = 15 A			27.5		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			620		pF
Output Capacitance	C_{OSS}				340		
Reverse Transfer Capacitance	C_{RSS}				7		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 48 V; I_D = 10 A			4.5		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 10 A			9.7		nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 10 A			1.3		nC
Gate−to−Source Charge	Q_{GS}				2.1		
Gate−to−Drain Charge	Q_{GD}				1		
Plateau Voltage	V_{GP}				3.0		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 10 A, R_G = 1 Ω			7		ns
Rise Time	t_r				13		
Turn−Off Delay Time	$t_{d(OFF)}$				25		
Fall Time	t_f				6		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.85	1.2	V
			T_J = 125°C		0.72		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 10 A			23.8		ns
Charge Time	t_a				11.9		
Discharge Time	t_b				11.8		
Reverse Recovery Charge	Q_{RR}				11.6		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

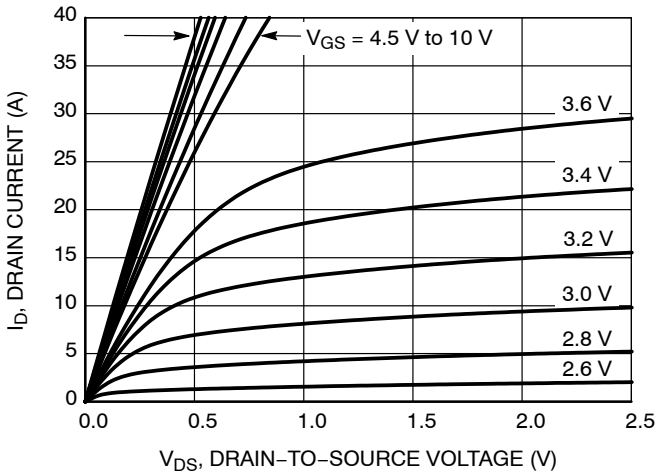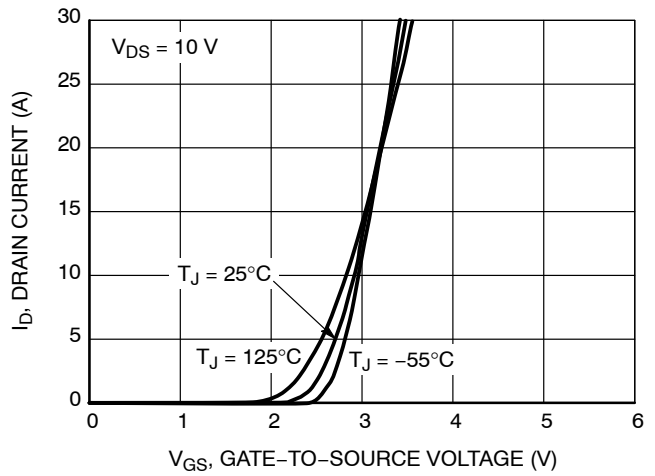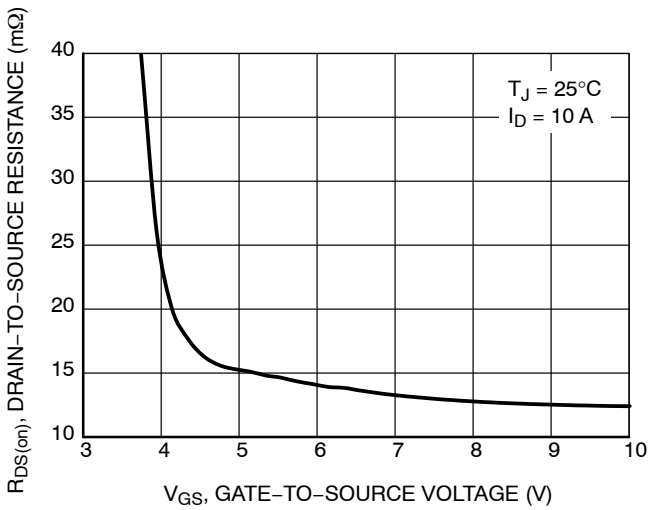**Figure 1. On−Region Characteristics**

Figure 2. Transfer Characteristics

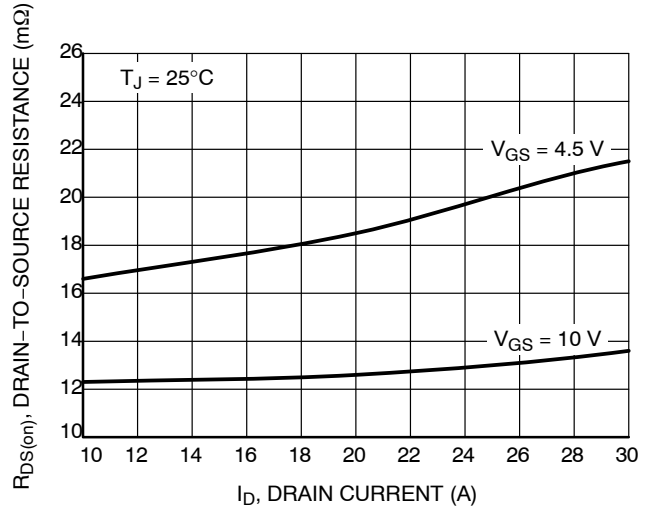**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

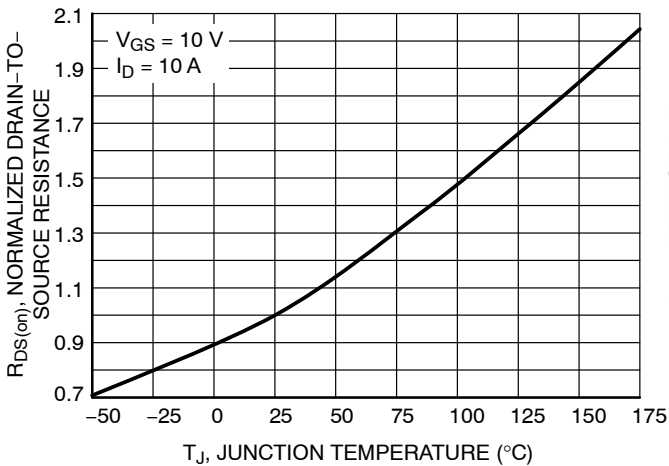**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

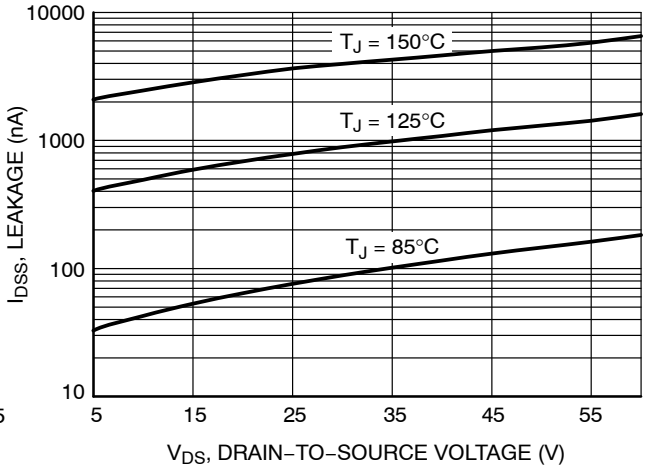**Figure 5. On−Resistance Variation with Temperature**

Figure 6. Drain−to−Source Leakage Current vs. Voltage
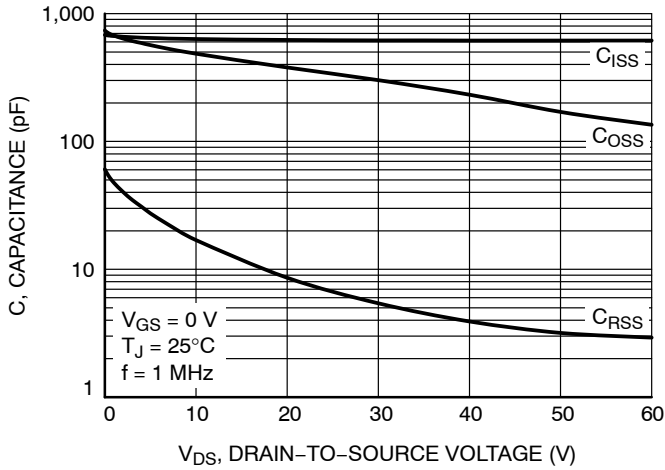
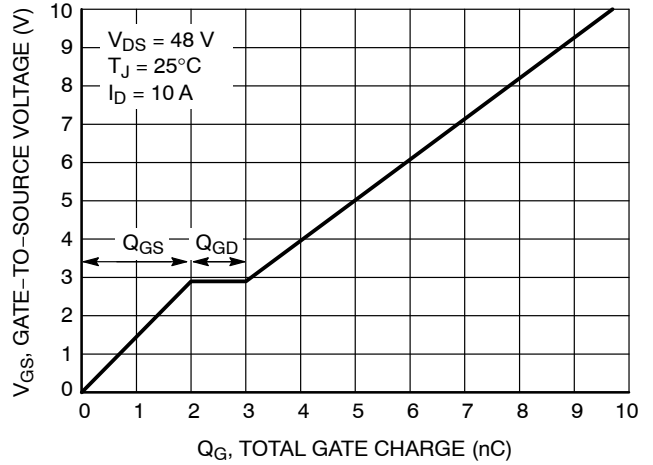## TYPICAL CHARACTERISTICS

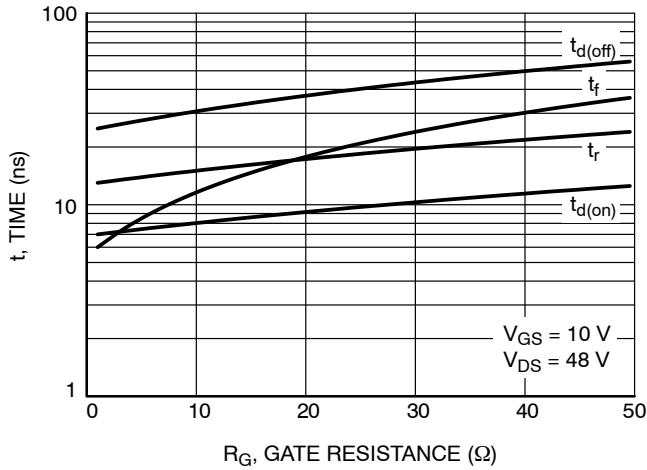Figure 7. Capacitance Variation

Figure 8. Gate−to−Source vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance
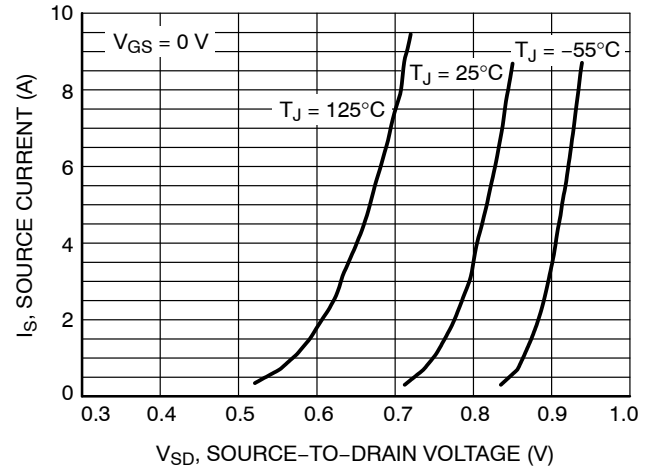
Figure 10. Diode Forward Voltage vs. Current
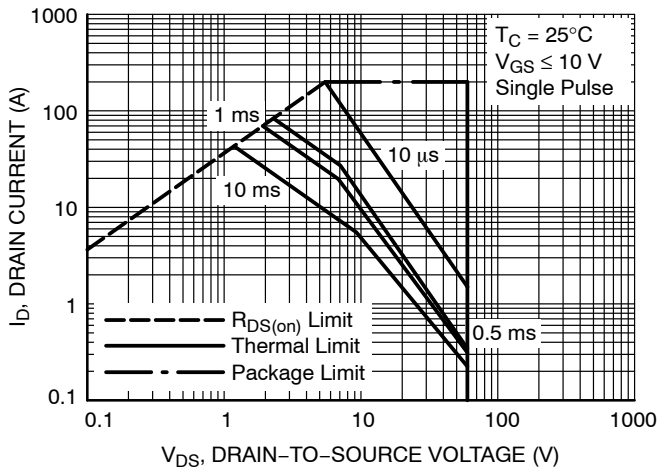
Figure 11. Maximum Rated Forward Biased Safe Operating Area
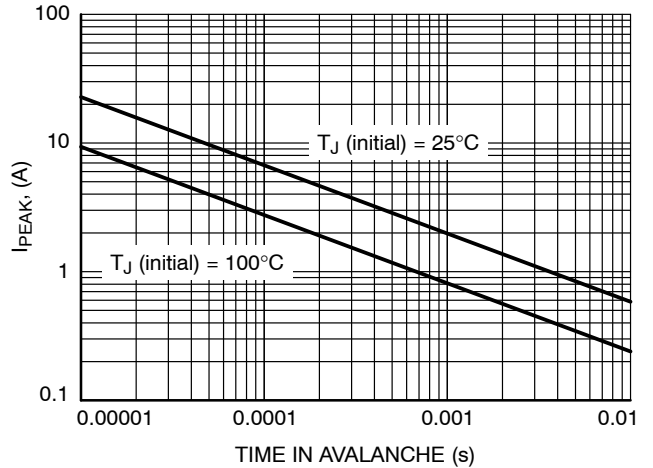
Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS
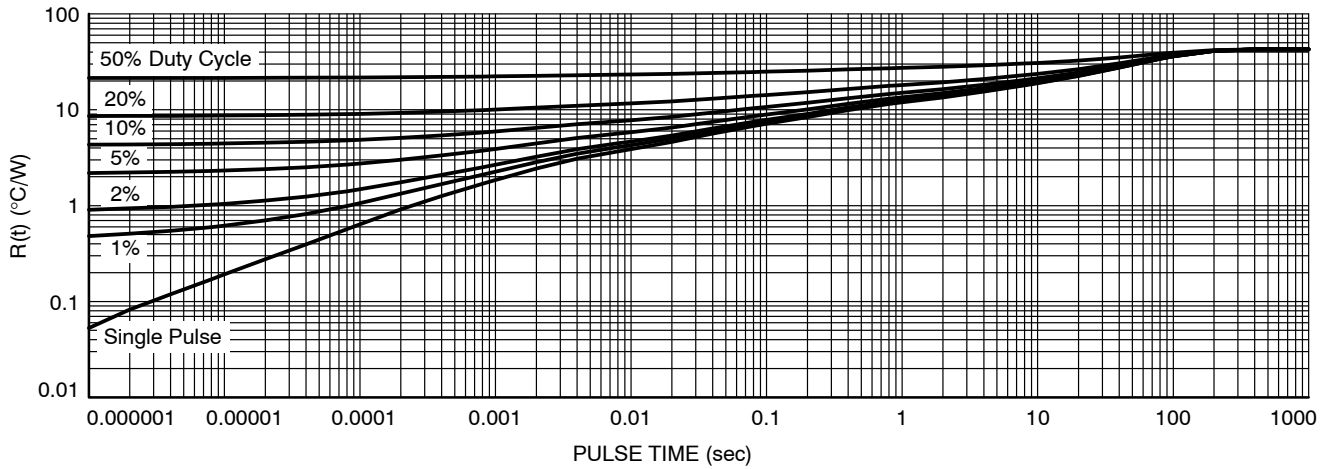
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping[†]
NVMFS5C677NLT1G	5C677L	DFN5 (Pb−Free)	1500 / Tape & Reel
NVMFS5C677NLWFT1G	677LWF	DFN5 (Pb−Free, Wettable Flanks)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

onsemi
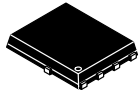
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

SCALE 2:1

DATE 25 JUN 2018

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

TOP VIEW

DETAIL A

SEATING PLANE

SIDE VIEW

DETAIL A

BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	---	12 °

GENERIC MARKING DIAGRAM*

XXXXXX
AYWZZ

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.
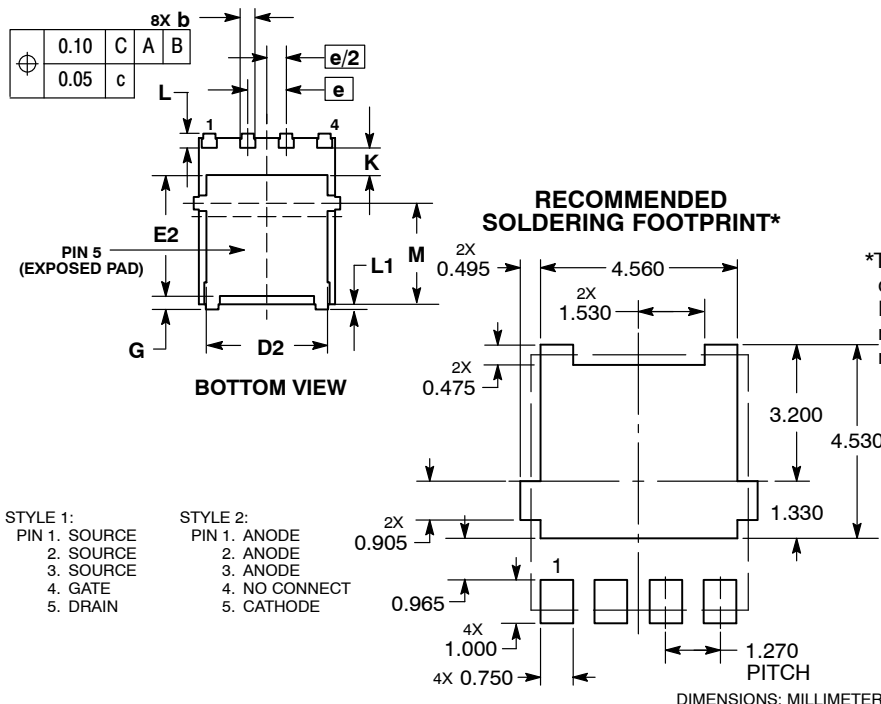
STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON14036D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**DFN5 5x6, 1.27P (SO−8FL)**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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