CA3142

TV Sync Processor

For Color and Monochrome Receivers

Features:

- *Internal impulse noise processing*
- *Sync separator - low impedance, dual polarity*
- *Strobed AGC system*
- *IF AGC output*
- *Delayed outputs for forward or reverse AGC tuners*
- *Automatic noise threshold and AGC detector level control*
- *High-impedance video input*
- *Low-impedance video output*
- *Choice of external time constants for sync separator*
- *Negative power supply not required*
- *RF AGC delay externally controlled*

The RCA-CA3142 is a monolithic silicon integrated circuit TV signal processor for use in color or monochrome receivers. These circuits provide low-impedance video output signals, stripped synchronization signals in both polarities, and AGC output signals for IF (reverse) and tuner (forward and/or reverse).

The circuit design of the CA3142 features impulse noise inversion, delay techniques to reduce the deleterious effects of impulse noise in the receiver AGC and sync circuits. In addition, they incorporate standard AGC strobing techniques.

The CA3142 is supplied in a 16-lead dual-in-line plastic package (E suffix).

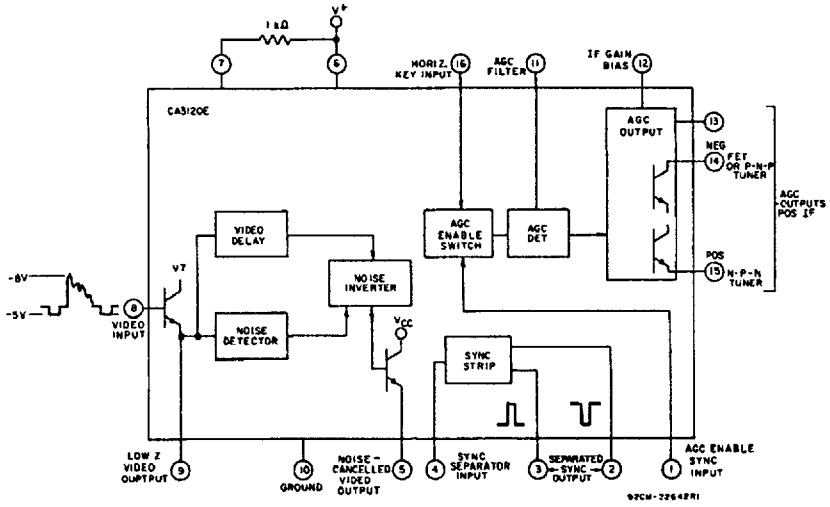

Fig. 1 - Simplified block diagram of the CA3142.

File Number **907**

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ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, Supply Voltage (V^+) = 24 V and Referenced to Test Circuits and Test Conditions (Figs. 6, 7, and 8).

CHARACTERISTICS	TERMINAL MEASURED AND SYMBOL	CA3142 LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current (Pulse Test)	I_{T24}	20	–	40	mA
AGC Threshold (Sync Tip Level at Video Input)	V_{TH}	4.5	–	5.5	V
Video Input Amplitude (White Positive)	V_8	–	3	–	Vp-p
Video Output Amplitude (Low Impedance)	V_9	–	3	–	Vp-p
Noise Cancelled Video Output at V_{TH} (Black Positive, Gain ≅ 2)	V_5	3.6	–	9.2	V
AGC to Noise Separation	$V_{TH\ (SEP)}$	1.1	–	2.2	V
Sync Input Current for Full Amplitude Outputs	$I_{4\ (ON)}$	–	–	100	μA
Maximum Leakage Current at Terminal 4	$I_{4\ (OFF)}$	–	–	±6	μA
Sync Outputs:					
Negative Sync Low	$V_{2(L)}$	0	–	2.6	V
Negative Sync High	$V_{2(H)}$	23.8	–	24	V
Positive Sync Low	$V_{3(L)}$	0	–	0.2	V
Positive Sync High	$V_{3(H)}$	20.1	–	24	V
AGC Filter:					
Charge Current (Pulse Test)	$I_{11(CH)}$	12	–	36	mA
Discharge Current	$I_{11(DISCH)}$	1.1	–	2.6	mA
Leakage Current	$I_{11(LEAK)}$	–	–	±6	μA
AGC Enable:					
Horizontal Keying	$V_{16\ (ON)}$	3	–	6	V
Negative Sync Input Current	$I_{1\ (ON)}$	–	1	–	mA
Maximum IF Gain-Clamp Voltage	V_{11}	4.8	–	5.7	V
Maximum IF Gain Bias	V_{12}	4.2	–	5.2	V
IF AGC Voltage:					
Low	$V_{13\ (LOW)}$	0	–	3.3	V
High	$V_{13(HIGH)}$	5.7	–	6	V
Tuner Currents:					
Reverse AGC (FET) OFF Current	$I_{14\ (OFF)}$	–	–	±6	μA
Reverse AGC (FET) ON Current	$I_{14\ (ON)}$	1.8	–	5.5	mA
Forward AGC (n-p-n) OFF Current	$I_{15\ (OFF)}$	–	–	±6	μA
Reverse AGC (n-p-n) ON Current	$I_{15\ (ON)}$	4.5	–	15	mA

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C*

DC SUPPLY VOLTAGE ..... 30 V

DEVICE DISSIPATION:

Up to T_A = 55°C ..... 750 mW

Above T_A = 55°C ..... Derate linearly at 7.9 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... -40 to +85°C

Storage ..... -65 to +150°C

LEAD TEMPERATURE (During Soldering):

At a distance not less than 1/32 in. (0.79 mm) from case for 10 s max. ..... +265°C

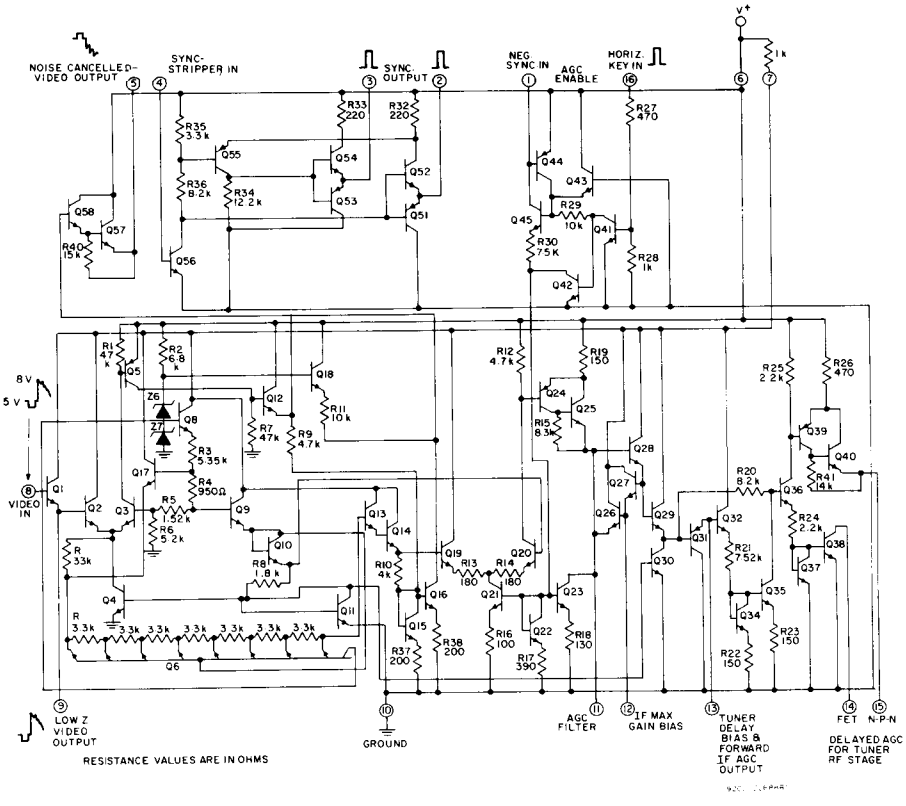

Fig. 2 - Schematic diagram of the CA3142.

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Circuit Description*

An AGC sample-and hold system generates control voltages proportional to the video level. The sync-tip voltage is compared to an internal reference voltage during the horizontal synchronization (retrace) interval. The control voltages (AGC outputs) are supplied to the tuner's RF stage and the IF amplifier to maintain the video level at a constant value.

The composite positive and negative output sync signals are developed across a low impedance source (totem-pole circuit) at an amplitude of approximately 20 volts peak-to-peak.

Video Chain and Impulse Noise Inverter — The input video signal applied at Terminal 8 is white "positive" with a required amplitude in the range of 2 to 4 volts. The DC level of the sync peaks, AGC threshold voltage (V_{TH}) is approximately 5 volts. The level is maintained at 5 volts by the AGC loop in the circuit, comprised of the CA3142 and the TV receiver RF and IF amplifiers. A low source impedance video signal is available from the emitter of Q1 (Terminal 9 in Fig. 2). The external resistor (R_{X1} in Fig. 9) reduces the dissipation of Q1. The emitter-follower output of Q1 is directly coupled to a differential comparator stage (Q2, Q3). Unless a negative-going pulse is present, Q2 functions as an emitter follower and also cuts off transistors Q3, Q5, and Q12.

The output of Q2 is applied through a signal delay network, consisting of transistor Q60 and associated resistors, to the Darlington followers (Q13 and Q14). The delayed video signal at Q14 is fed via its emitter to an AGC comparator Q19 and to the junction of a noise-cancelling amplifier stage (Q16). The noise-cancelled video signal is inverted and amplified by Q16 and then connected to a Darlington emitter-follower output stage (Q57, Q58).

If impulse noise is present on the video signal, Q3 conducts and turns on transistors Q5 and Q12. Q5 inverts and "stretches" the noise pulse width. The output of Q5 is applied to an emitter follower stage (Q12). The signal from Q12, in turn, is applied to the summing junction to the noise-cancelling amplifier Q16. The noise pulse, which has now been amplified, inverted and stretched, is added to the delayed video signal from the emitter of Q14.

Because the video signal has been delayed approximately 300 nanoseconds and the noise pulse has been widened ("stretched") approximately 500 nanoseconds, the output of the combined signal no longer contains impulse noise signals. The derived noise-gating pulse "surrounds" and effectively eliminates the effects of the impulse noise.

The noise-cancelled video signal, amplified and buffered, is available at Terminal 5 for use in the sync-separator stage. The peak-to-peak amplitude of the noise-cancelled output signal is approximately twice the amplitude of the input video signal at Terminal 8.

Sync Separator (See Fig. 3) — The sync separator stage (Q56) clamps the detected sync tips to a fixed reference voltage (≅0.7 V) across its base-emitter junction, and amplifies a portion of the sync signal to provide dual polarity sync-signal outputs at Terminals 2 (negative) and 3 (positive). The output signals are derived from low-impedance complementary emitter-follower stages; a base current of 100 microamperes into Terminal 4 is sufficient to generate full-amplitude sync signals.

The choice of coupling the noise-cancelled video-signal from the emitter-follower (Terminal 5) to the sync separator (Terminal 4) is a user option. Fig. 4 shows three typical coupling networks.

Fig. 5 illustrates the operation of the AGC circuits. An input ramp signal, simulating the potential to which the AGC filter capacitor may be charged, is applied to Terminal 11. The forward IF AGC output voltage appears at Terminal 13. Under low-signal level conditions (represented by A to B in Fig. 5) the output level is approximately 1.4 volts less than the voltage applied to Terminal 12.

The circuit designer should select the voltage at Terminal 12 to provide the maximum IF gain required for the system. At intermediate signal level conditions (represented by B to C in Fig. 5), the IF AGC signal follows the AGC filter potential. The tuner(s) will operate at maximum gain for good signal-to-noise ratios at these equivalent input signal levels. Point C is a turnover point determined by the open-circuit potential of the tuner-delay bias potentiometer. At this potential, further change in the IF AGC output is inhibited (for good dynamic range) and the tuner AGC potentials are activated (represented by C to D).

The output at Terminal 14 with suitable level shifting is used for tuners requiring reverse AGC, such as MOSFET or electron-tube types. The output at Terminal 15 is used for tuners requiring forward AGC, such as tuners utilizing n-p-n bipolar transistors.

*For additional information refer to the IEEE "Transactions on Broadcast and TV Receivers," August 1970, pp 185-195, Vol. BTR No. 3. Also refer to ICAN-6302.

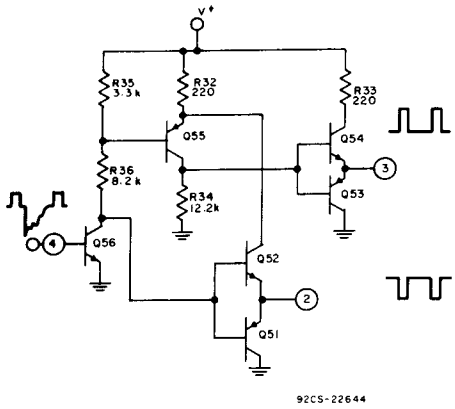

Fig. 3 - Sync separator stage.

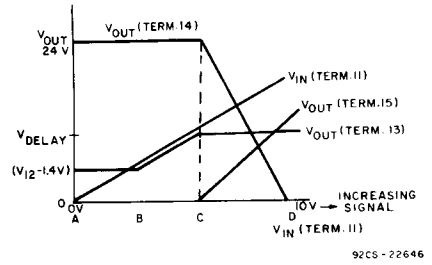

Fig. 5 - Typical operation of the AGC circuits using the CA3142.

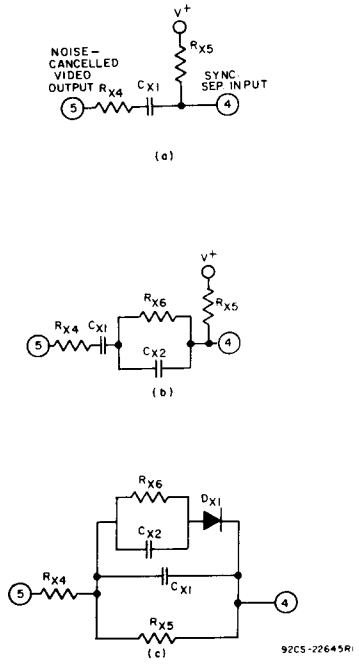

Fig. 4 - Typical coupling networks (Term. 5 to Term. 4).

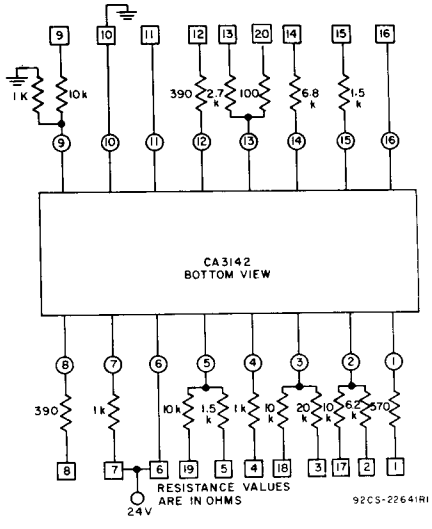

Fig. 6 - Test circuit for measuring electrical characteristics of the CA3142. Refer to Figs. 7 and 8 for switch selector positions.

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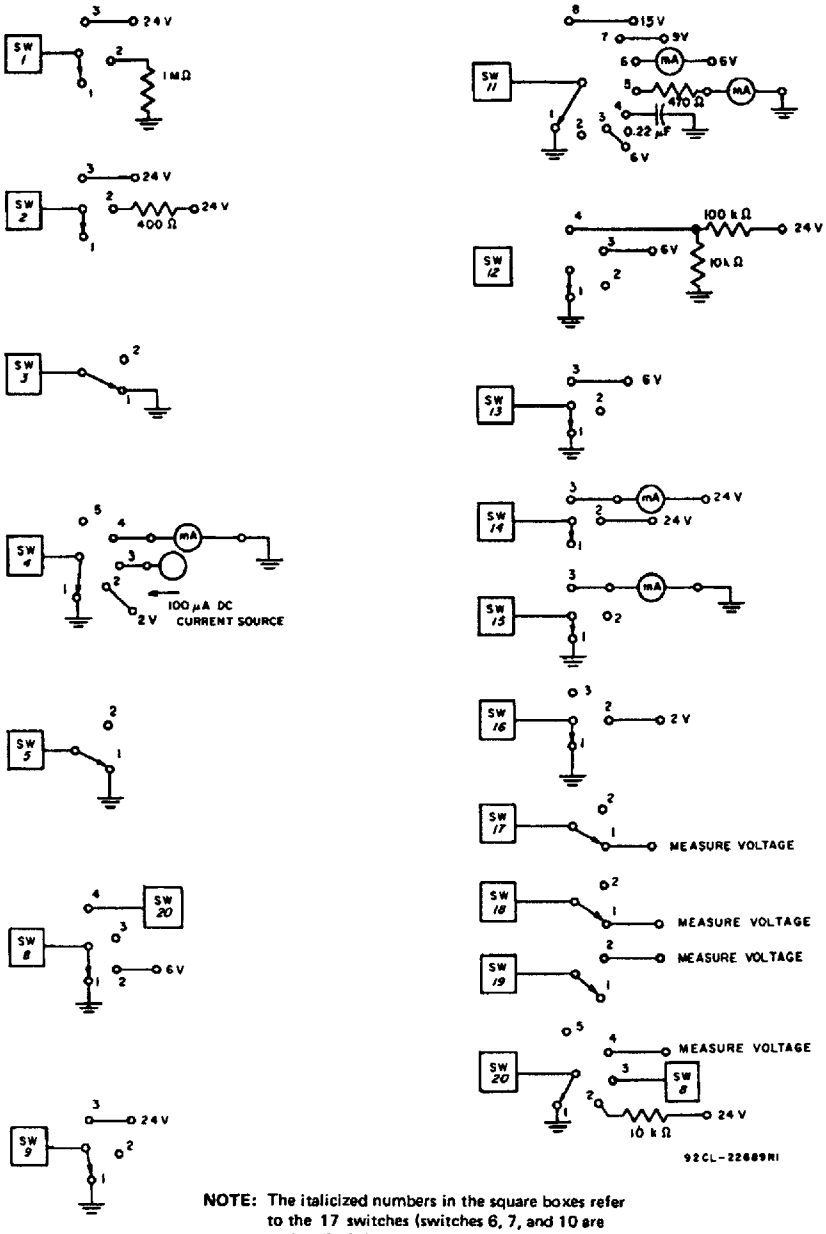

NOTE: The italicized numbers in the square boxes refer to the 17 switches (switches 6, 7, and 10 are omitted) of the test circuit and correspond to those given in Figs. 6 and 8.

CAUTION: Remove power before selecting or adjusting switches

Fig. 7 - Test condition selector switch arrangement for measuring the electrical characteristics of the CA3142.

CHARACTERISTIC	TEST CONDITIONS — SWITCH NUMBERS / SWITCH POSITION																	TERMINAL MEASURED
	1	*2*	*3*	*4*	*5*	*8*	*9*	*11*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*19*	*20*	
I_{T24}	2	3	1	2	1	2	3	1	1	3	2	1	2	2	2	1	5	*2 6 7 9 14*
V_{TH}	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	1	3	*8*
V_5	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	2	3	*19*
$V_{TH(SEP)}$	3	1	2	1	1	*	3	3	4	1	1	2	1	2	2	2	1	*
$I_{4(OFF)}$	3	1	2	4	2	1	1	1	1	1	1	2	1	2	2	1	1	I_4
V_{2L}	1	2	2	3	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{2H}	3	3	1	1	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{3L}	3	3	1	1	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
V_{3H}	3	3	1	3	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
$I_{11(CH)}$	2	1	2	5	2	1	1	5	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(DISCH)}$	2	1	2	5	1	2	3	6	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(LEAK)}$	2	1	2	5	2	1	1	6	4	3	2	2	1	2	2	1	5	I_{11}
V_{11}	2	1	2	5	1	2	3	2	3	3	1	2	2	2	2	1	5	V_{11}
V_{12}	3	1	2	5	2	1	1	3	4	3	1	2	1	2	2	1	5	V_{12}
$V_{13(LOW)}$	3	1	2	5	2	2	3	1	1	2	1	2	1	2	2	1	2	V_{13}
$V_{13(HIGH)}$	3	1	2	5	2	2	3	7	4	3	2	1	1	2	2	1	4	V_{20}
$I_{14(OFF)}$	3	1	2	5	2	2	3	3	4	3	3	1	1	2	2	1	5	I_{14}
$I_{14(ON)}$	3	1	2	5	2	2	3	8	4	3	3	1	1	2	2	1	5	I_{14}
$I_{15(OFF)}$	3	1	2	5	2	2	3	3	4	3	2	3	1	2	2	1	5	I_{15}
$I_{15(ON)}$	3	1	2	5	2	2	3	8	4	3	2	3	1	2	2	1	5	I_{15}

CAUTION: Remove power before selecting or adjusting switches.

* Reduce voltage at Terminal 8 until V_{19} decreases. $V_{TH(SEP)} = V_{TH} - V_8$.

NOTE: Switch numbers in italics correspond to numbers in square boxes in Figs. 6 and 7.

Fig. 8 - Test condition values for associated switches 1 through 20 (switches 6, 7, and 10 are omitted). Refer to Figs. 6 and 7 for test circuit and test-condition selector-switch arrangements.

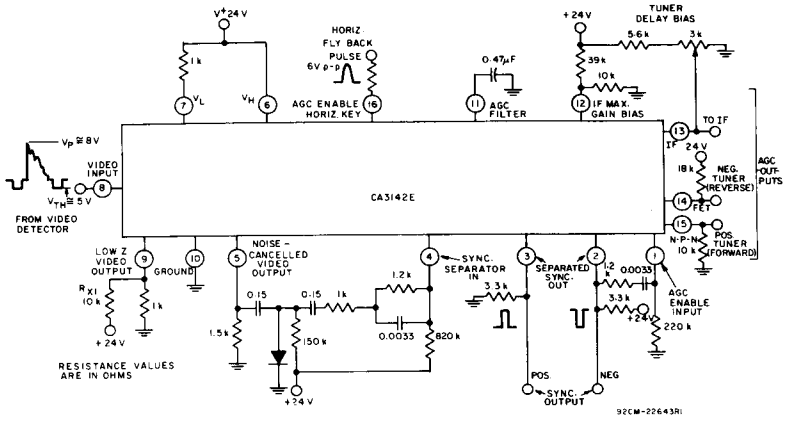

Fig. 9 - Typical application using the CA3142.