High Performance 100 V Bridge Power Stage Module

FDMF8811

PQFN36 6 x 7.5, 0.5P
CASE 483BB

The 100 V Bridge Power Stage (BPS) Module is a fully optimized, compact, integrated MOSFET plus driver power stage solutions for high current DC−DC switching applications. The FDMF8811 integrates a driver IC, two power MOSFETs and a bootstrap diode into a thermally enhanced, compact 6.0 mm x 7.5 mm PQFN package. The PQFN packaging ensures low package resistance improving the current handling capability and performance of the part.

With an integrated approach, the complete switching power stage is optimized with regards to driver and MOSFET dynamic performance, system parasitic inductance, and Power MOSFET $R_{DS(ON)}$. The FDMF8811 uses high performance POWERTRENCH® MOSFET technology, which reduces switch ringing in converter applications. The driver IC features low delay time and matched PWM input propagation delays, which further enhance the performance of the part.

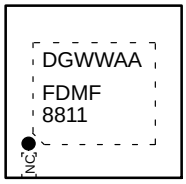
Features

- Compact Size − 6.0 mm x7.5 mm PQFN
- High Current Handling: 20 A
- >97% System Efficiency at 600 W Full Bridge Applications PSRR Value
- Wide Driver Power Supply Range: 8 V to 14 V
- Internal Pull−down Resistors for PWM Inputs (HI,LI)
- 3.3 V/TTL Compatible Input Thresholds
- Short PWM Propagation Delays
- Drive Power Supply Under−voltage Lockout (UVLO)
- Integrated 100 V Half−Bridge Gate Driver with 1 Ohm Bootstrap Diode
- Low Inductance and Low Resistance Packaging for Minimal Operating Lower Losses
- 100 V POWERTRENCH MOSFETs for Clean Switching Waveforms

Typical Applications

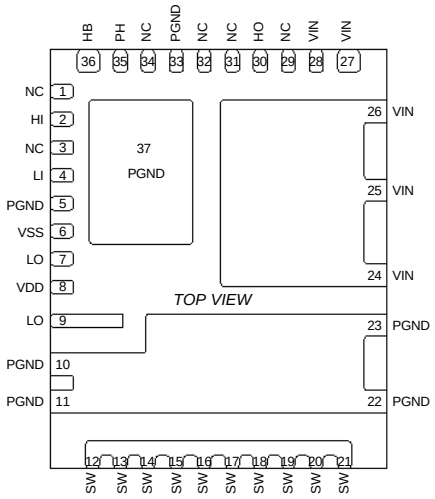
- Telecom Half / Full − Bridge DC−DC Converters
- Two−Switch Forward Converters
- Intermediate Bus Converters
- Brick Converters
- High−current DC−DC Point of Load (POL) Converters

MARKING DIAGRAM



D	= Assembly Plant Code
G	= Year Code
WW	= Work Week
AA	= Lot Code
FDMF8811	= Specific Device Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

Typical Applications

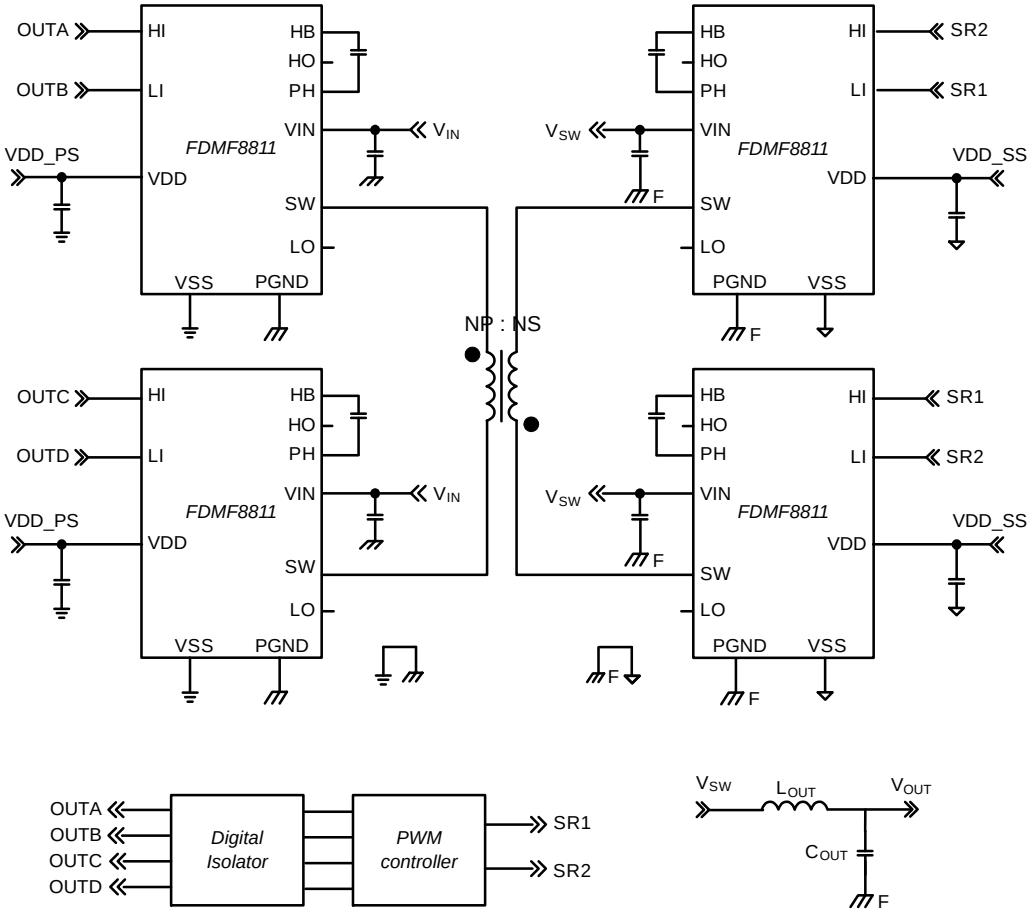


Figure 1. Full−Bridge Isolated DC−DC Converter

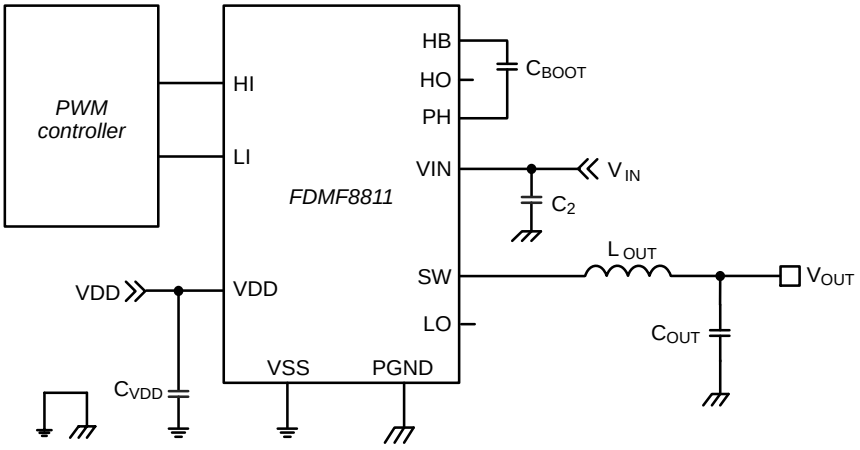


Figure 2. Typical Applications in Buck DC−DC Converter

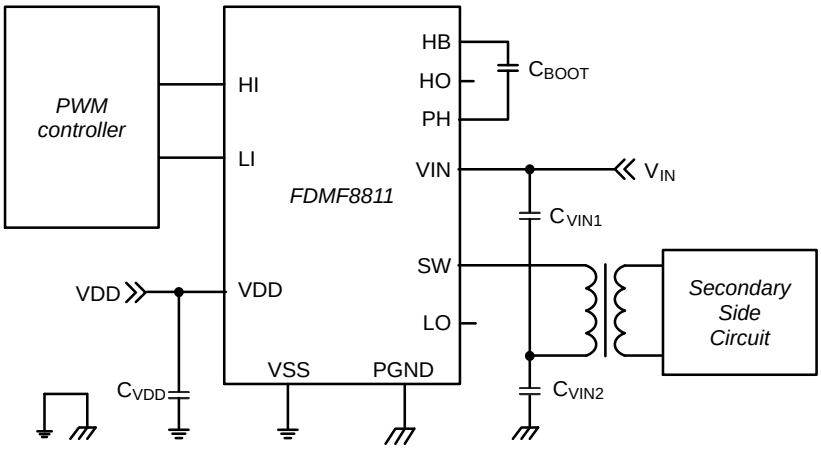


Figure 3. Half−Bridge Isolated DC−DC Converter

Block Diagram

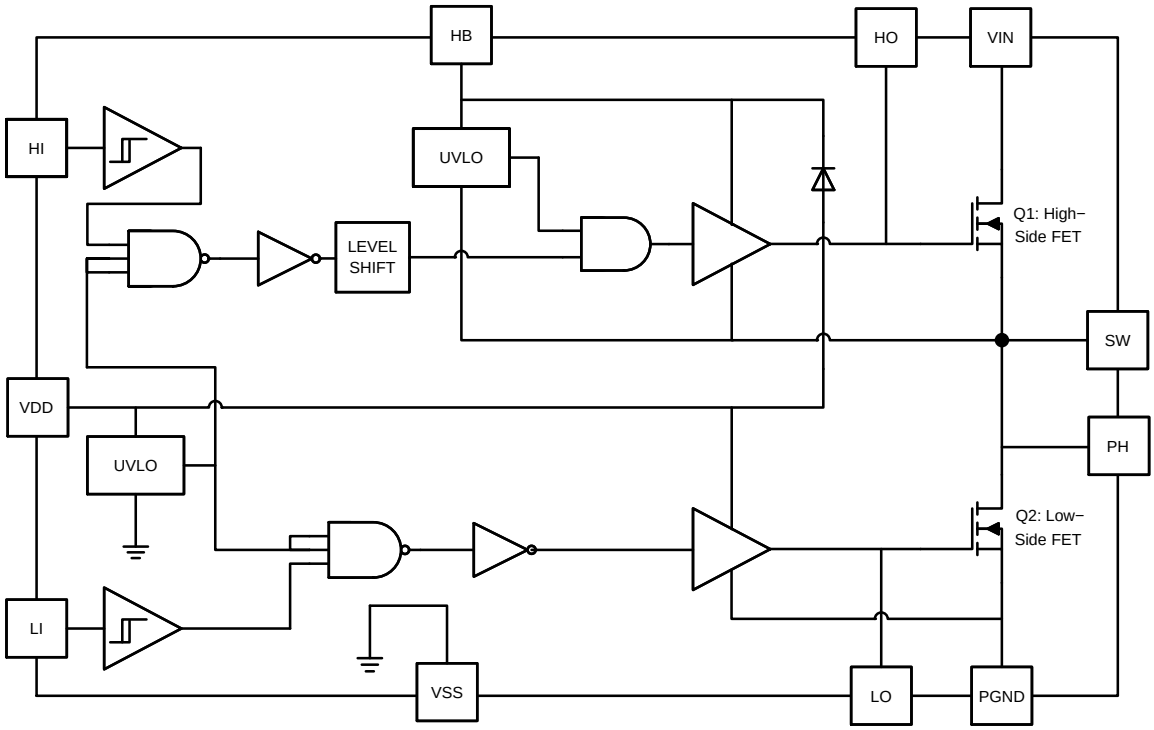


Figure 4. Simplified Block Diagram

PIN CONNECTIONS

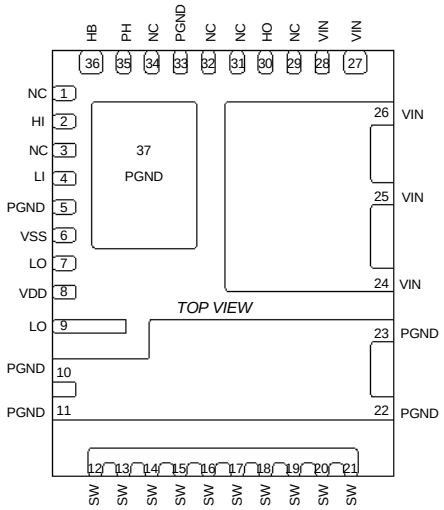


Figure 5. Pin Connections (Top View)

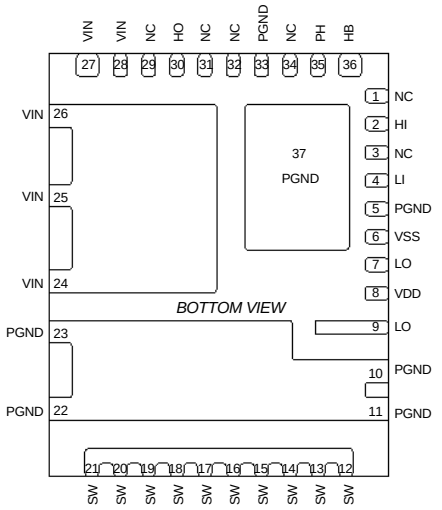


Figure 6. Pin Connections (Bottom View)

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1, 3, 29, 31−32, 34	NC	No connect
2	HI	High−side PWM input.
4	LI	Low−side PWM input.
5, 10, 11, 22, 23, 33, 37	PGND	Power return for the power stage.
6	VSS	Analog ground for driver IC analog circuits.
7, 9	LO	Low−side gate drive output.
8	VDD	Power supply input for low−side gate drive and bootstrap diode. Bypass this pin to PGND with a low impedance capacitor.
12−21	SW	Switching node junction between high−side and Low−side MOSFETs.
24−28	VIN	Power input for the power stage. Bypass this pin to PGND with low impedance capacitor.
35	PH	High−side source connection (SW node) for the bootstrap capacitor.
30	HO	High−side gate drive output.
36	HB	Bootstrap supply for high−side driver. Bypass this pin to PH with low impedance capacitor.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Drive Power Supply Pin to PGND Pin Voltage		$V_{DD} - V_{GND}$	−0.3 to 16	V
Input Power Supply Pin to PGND Pin Voltage		$V_{IN} - V_{GND}$	−0.3 to 100	V
SW Pin to PGND Pin Voltage	DC	$V_{SW} - V_{GND}$	−1 to 100	V
	Repetitive pulse (<100 ns)		−18 to 100	
PH Pin to PGND Pin Voltage	DC	$V_{PH} - V_{GND}$	−1 to 100	V
	Repetitive pulse (<100 ns)		−18 to 100	
LO Pin to VSS Pin Voltage		$V_{LO} - V_{GND}$	−0.3 to V_{DD} + 0.3	V
HO Pin to VSS Pin Voltage		$V_{HO} - V_{GND}$	V_{PH} − 0.3 to V_{HB} + 0.3	V
PWM Input LI and HI Pin to VSS Pin Voltage		$V_{LI} - V_{GND}$, $V_{HI} - V_{GND}$	−0.3 to V_{DD} + 0.3	V
Operating and Storage Temperature Range		T_J, T_{STG}	−65 to 150	V
HB Pin to PH Pin Voltage		$V_{HB} - V_{PH}$	−0.3 to 16	V
HB Pin to PGND Pin Voltage		$V_{HB} - V_{GND}$	−0.3 to 118	V
Lead Temperature Soldering Reflow (SMD Styles Only)		T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics			°C/W
Thermal Resistance, Junction−to−Air (Note 1)	$R_{\theta JA}$	10	
Thermal Reference, Junction−to−case (Note 1)	$R_{\psi JL}$	2.24	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 In^2 pad 2 OZ copper pad on a 1.5 x 1.5 In. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design and operating conditions.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Input Power Voltage	VIN	20	75	V
Driver Supply Voltage DC Level	VDD	8	14	V
Switching Frequency	F_{SW}	20	410	kHz
Input PWM Signal Logic High Level (3.3 V/TTL Compatible Input Thresholds)	LI, HI	3	11	V
Operating Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical value is under VIN = 48 V, VDD = 12 V and $T_A = T_J$ = +25°C unless otherwise noted.
Min. and Max. values are under VIN = 48 V, VCC = PVCC = 12 V ±10% and $T_J = T_A$ = −40°C to +125°C unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
BASIC OPERATION						
V_{DD} Quiescent Current	V_{HI} = 0 V; V_{LI} = 0 V	I_{DD}	−	0.17	0.3	mA
V_{DD} operating Current	Fsw = 97.5 kHz	I_{DDO}	−	6.8	−	mA
HB Quiescent Current	V_{HI} = 0 V; V_{LI} = 0 V	I_{HB}	−	0.1	0.2	mA
V_{DD} UVLO Threshold	V_{DD} Rising	V_{DDR}	6.8	7.6	8.4	V
V_{DD} UVLO Hysteresis		V_{DDH}	−	0.6	−	V

ELECTRICAL CHARACTERISTICS (continued)
(Typical value is under VIN = 48 V, VDD = 12 V and $T_A = T_J$ = +25°C unless otherwise noted.
Min. and Max. values are under VIN = 48 V, VCC = PVCC = 12 V ±10% and $T_J = T_A$ = −40°C to +125°C unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
BASIC OPERATION						
HB UVLO Threshold	HB Rising	V_{HBR}	6.0	7.1	8.1	V
HB UVLO Hysteresis		V_{HBH}	−	0.4	−	V
PWM INPUT						
High Level Input Voltage Threshold		V_{IH}	1.8	2.2	2.5	V
Low Level Input Voltage Threshold		V_{IL}	1.3	1.7	2.0	V
Input Logic Voltage Hysteresis		V_{IHYS}	−	0.5	−	V
Input Pull−down Resistance		R_{IN}	−	100	−	kΩ
BOOTSTRAP DIODE						
Forward Voltage @ Low Current	I_{VDD-HB} = 100 μA	V_{FL}	−	0.55	0.8	V
Forward Voltage @ High Current	I_{VDD-HB} = 100 mA	V_{FH}	−	0.8	1	V
Dynamic Resistance	I_{VDD-HB} = 100 mA	R_D	−	0.7	1.7	Ω
Diode Turn−on or Turn−off Time	I_F = 20 mA, I_{REV} = 0.5 A	t_{BS}	−	20	−	ns
LOW SIDE DRIVER, LO						
Low Level Output Voltage	I_{LO} = 100 mA	V_{OLL}	−	0.1	0.25	V
High Level Output Voltage	I_{LO} = −100 mA, $V_{OHL} = V_{DD} - V_{LO}$	V_{OHL}	−	0.16	0.3	V
Peak Pull−up Current (Note 2)	V_{LO} = 0 V	I_{OHL}	−	3	−	A
Peak Pull−down Current (Note 2)	V_{LO} = 12 V	I_{OLL}	−	4	−	A
LO Rise Time	10% to 90%	t_{R_LO}	−	16.9	−	ns
LO Fall Time	90% to 10%	t_{F_LO}	−	15.8	−	ns
LI=Low Propagation Delay	V_{LI} falling at 1.6 V to V_{LO} falling at 3.0 V	t_{LPHL}	−	36	−	ns
LI=High Propagation Delay	V_{LI} rising at 2.2 V to V_{LO} rising at 3.0 V	t_{LPLH}	−	35	−	ns
HIGH SIDE DRIVER, HO						
Low Level Output Voltage	I_{HO} = 100 mA	V_{OLH}	−	0.1	0.25	V
High Level Output Voltage	I_{HO} = −100 mA, $V_{OHH} = V_{HB} - V_{HO}$	V_{OHH}	−	0.16	0.3	V
Peak Pull−up Current (Note 3)	V_{HO} = 0 V	I_{OHH}	−	3	−	A
Peak Pull−down Current (Note 3)	V_{HO} = 12 V	I_{OLH}	−	4	−	A
HO Rise Time	10% to 90%	t_{R_HO}	−	23.4	−	ns
HO Fall Time	90% to 10%	t_{F_HO}	−	17.7	−	ns
HI = Low Propagation Delay	V_{HI} falling at 1.6 V to V_{HO} falling at 3.0 V	t_{HPHL}	−	39	−	ns
HI = High Propagation Delay	V_{HI} rising at 2.2 V to V_{HO} rising at 3.0 V	t_{HPLH}	−	37	−	ns
DELAY MATCHING						
HO Turn−OFF to LO Turn−ON to		T_{MON}	−	3.0	10	ns
LO Turn−OFF to HO Turn−ON		T_{MOFF}	−	2.4	10	ns
MINIMUM PULSE WIDTH						
Minimum Pulse Width for HI and LI (Note 2)		t_{PW}	−	−	50	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. These parameters are guaranteed by design.

TYPICAL CHARACTERISTICS

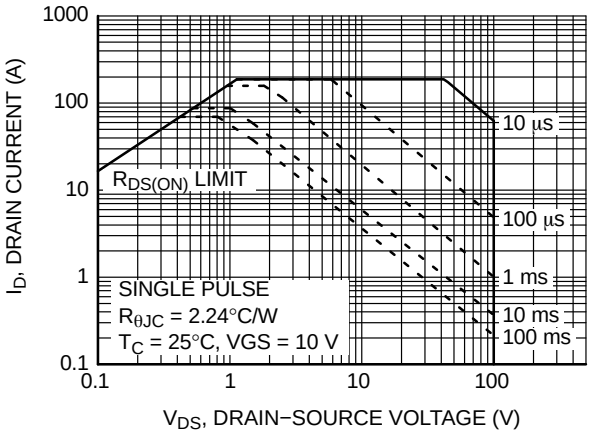


Figure 7. Forward Bias Safe Operating Area

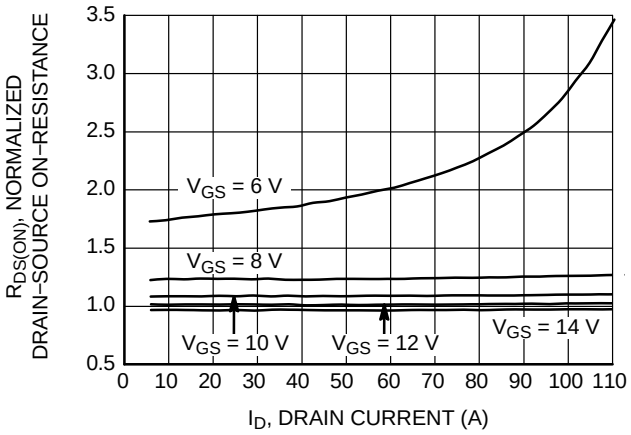


Figure 8. Normalized On Resistance vs. Drain Current and Gate Voltage

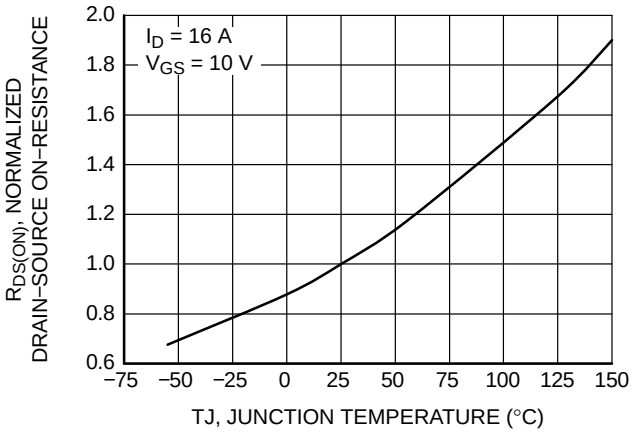


Figure 9. Normalized On Resistance vs. Temperature

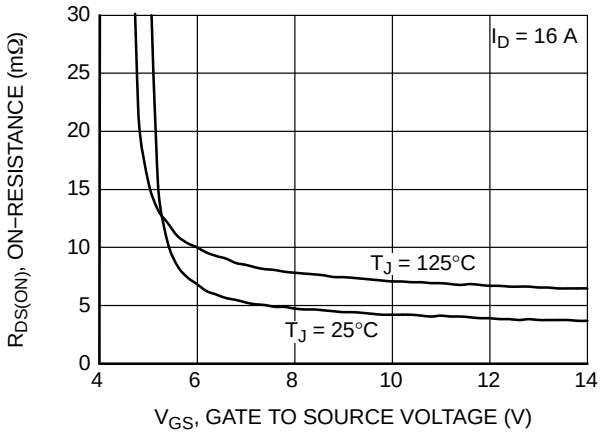


Figure 10. On Resistance vs. Gate to Source Voltage

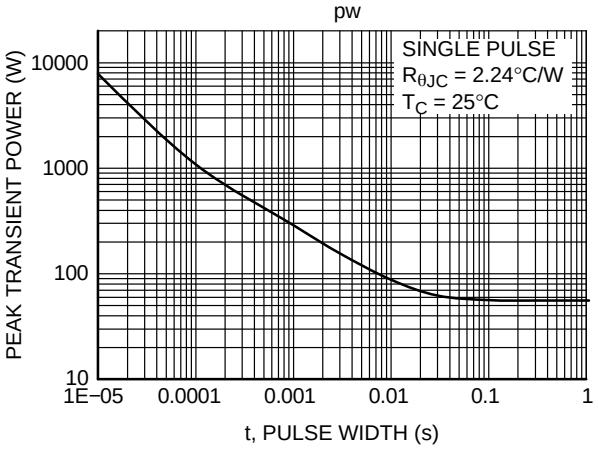


Figure 11. Single Pulse Maximum Power Dissipation

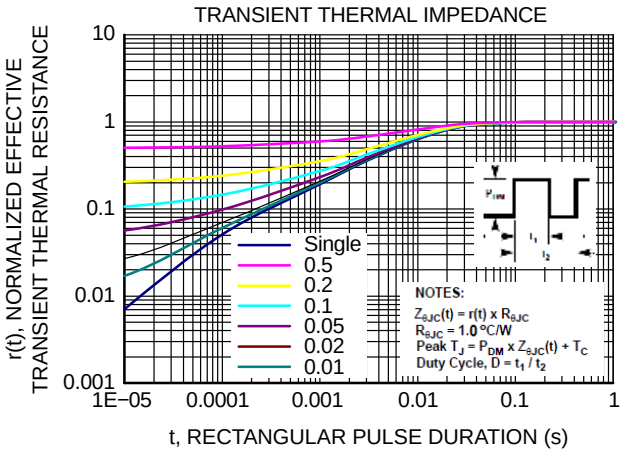


Figure 12. Junction to Ambient Transient Thermal

TYPICAL CHARACTERISTICS (Continued)

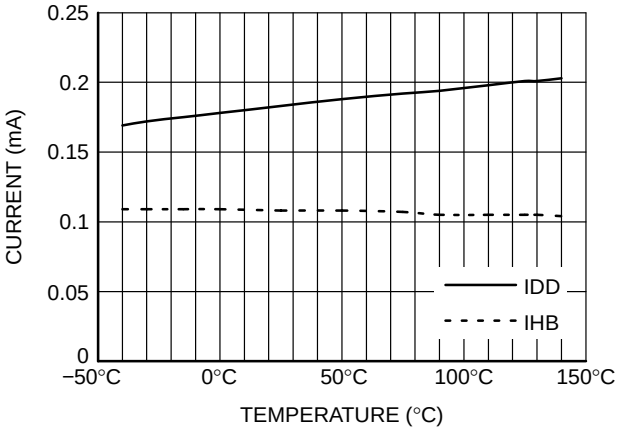


Figure 13. Driver Quiescent Current vs. Temperature

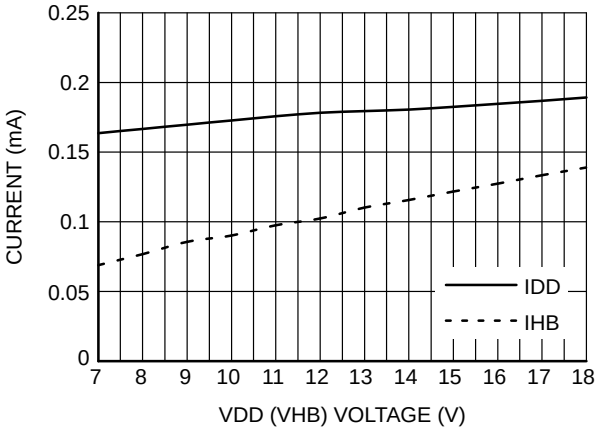


Figure 14. Driver Quiescent Current vs. V_{DD} (V_{HB})

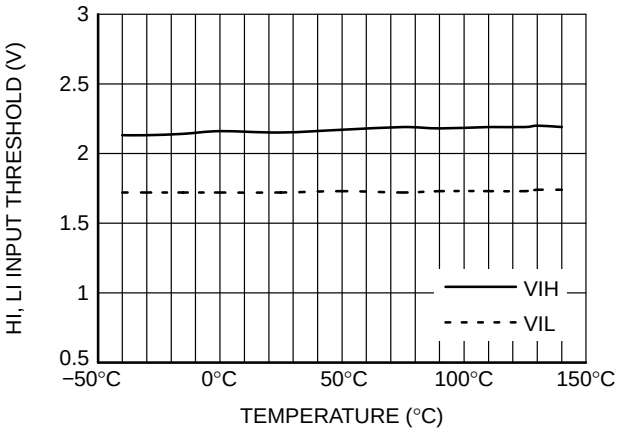


Figure 15. Input Threshold vs. Temperature

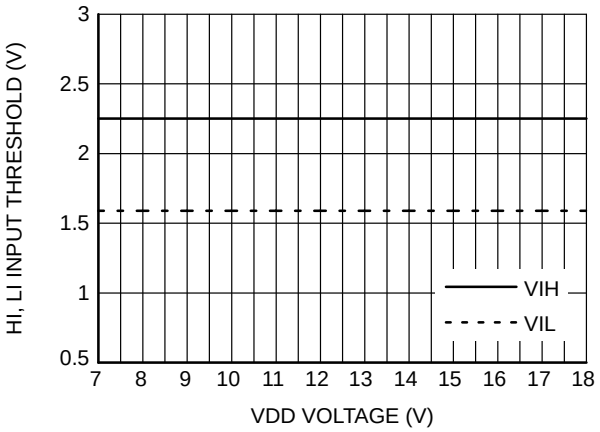


Figure 16. Input Threshold vs. V_{DD}

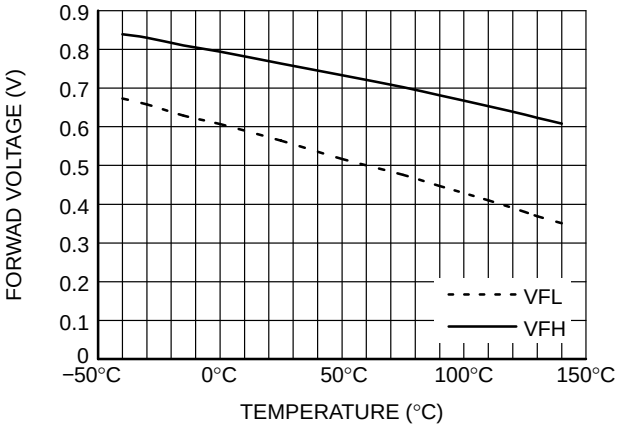


Figure 17. Boost Strop Diode V_F vs. Temperature

Switching Time Definitions

Figure 18 shows the switching time waveforms definitions of the turn on and off propagation delay times.

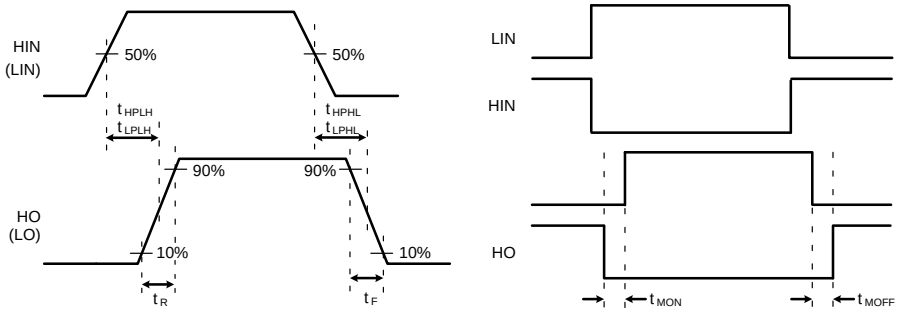


Figure 18. Timing Diagrams

Input to Output Definitions

Figure 19 shows an input to output timing diagram for overall operation.

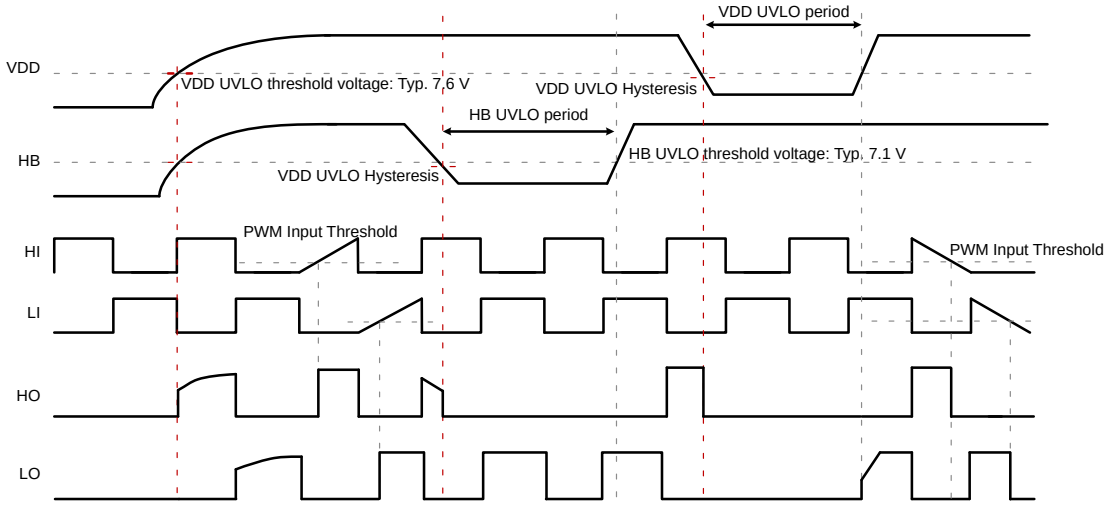


Figure 19. Overall Operation Timing Diagram

APPLICATIONS INFORMATION

The FDMF8811 co−packages one driver IC with integrated bootstrap diode, one low side 100 V power MOSFET and one high side 100 V power MOSFET in a thermally enhanced, compact 6.0 mm x 7.5 mm PQFN package. To perform the half bridge power module function, two 3.3 V/TTL compatible PWM input signals are connected to the FDMF8811's LI and HI pins. The inside driver IC will converter the two input PWM signals into driver signals LO and HO for both low side and high side power MOSFET. A bootstrap capacitor recommended value being 100 nF is required to be connected between HB and PH pin to provide floated driver signal for high side power MOSFET.

Driver Power Supply

Driver power supply quality is very important in DC−DC power applications. First, voltage level of the driver power supply determines pull up/pull down strength of the driver's output signals, switching speed and power conversion efficiency. The higher the DC level of driver power supply is, the higher the pull up and pull down strength is. Second, the DC level of drive power supply determines the operation mode of power MOSFET conducting large current. If the level is low, the power MOSFET safe operation area (SOA) as specified in the power device characteristics will become smaller and its current conduction ability is degraded. If the level is too low, the power MOSFET might even work in saturation region in some cases to cause device damage. Third, the DC level of driver power supply affects the propagation delay inside the drivers and the drain to source voltage stress on the power MOSFET. In high performance power applications, the above factors need to be well controlled by designing a high quality driver power supply circuit to ensure consistent switching performance and best power conversion efficiency. As the FDMF8811 is optimized to operate in VDD = 10 V, our recommended driver power supply is 10 V DC level with less than 100 mV peak to peak ripple.

When customer consider upgrading their nowadays components with FDMF8811, they need to be aware that the load current of the driver power supply might be significantly decreased in comparison with their nowadays solutions with discrete MOSFETs or other companies' components. The reason is that applies the most advanced device technology FDMF8811, so the gate charging current is significantly less and the customer is expected to see around 6.8 mA load current when driving one FDMF8811 with 10 V VDD and 97.5 kHz switching frequency.

We notice that some Flyback based VDD power supply circuit might present oscillation when load current becomes less than 10 mA, so recommends customer to first evaluate and improve their nowadays driver power supply circuit, then power up the whole DC−DC system with the FDMF8811s.

For the convenience of customer to design their VDD power supply system, Figure 20 and Figure 21 provides typical VDD power supply load current of the FDMF8811 and its relationship with VDD level and switching frequency.

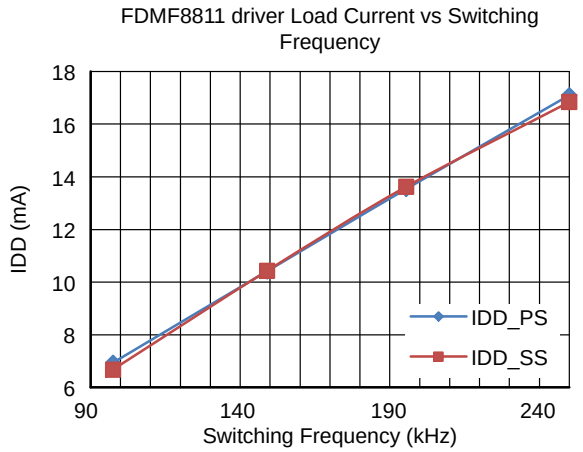


Figure 20. Driver Current per FDMF8811 vs. Switching Frequency

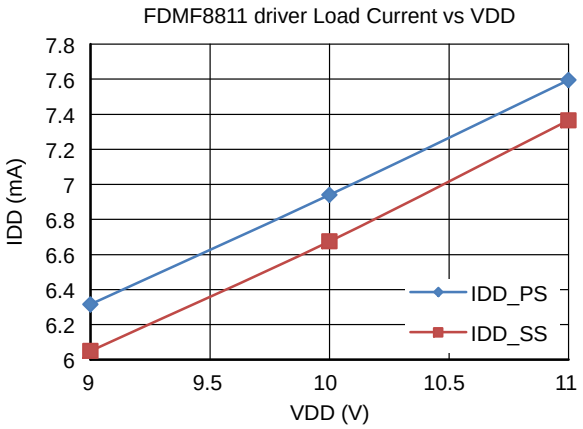


Figure 21. Driver Current per FDMF8811 vs. VDD

Start Up / Shut Down Sequence

When powering up a DC−DC conversion system or recovering the system from fault conditions, a correct start up timing sequence is highly recommended to avoid overstress or even damage of the components in the system. It is highly recommended to configure the power system to have more than 5 milliseconds time margin between the event that the driver power supplies are turned on and the event the system sends out CTRL signal to activate the controller PWM, so that PWM signals are ensured not presenting in the PWM forbidden zone illustrated in Figure 22. "VDD_PS" in Figure 22 refers to VDD power supply at primary side and "VDD_SS" refers to VDD power supply at secondary side.

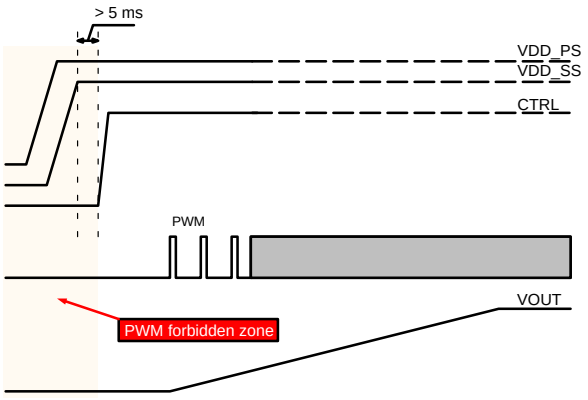


Figure 22. VDD Power Supply Timing Sequence During Start Up

A correct timing sequence is also required when powering down a DC−DC conversion system to avoid overstress or even damage of the components in the system. It is highly recommended to configure the power system to have more than 5 milliseconds time margin between the event that the controller pulls down PWM signals and the event the driver power supplies are turn off. The PWM forbidden region illustrated in Figure 23 suggests no PWM signal 5 milliseconds before VDD power supplies starts to lose regulation.

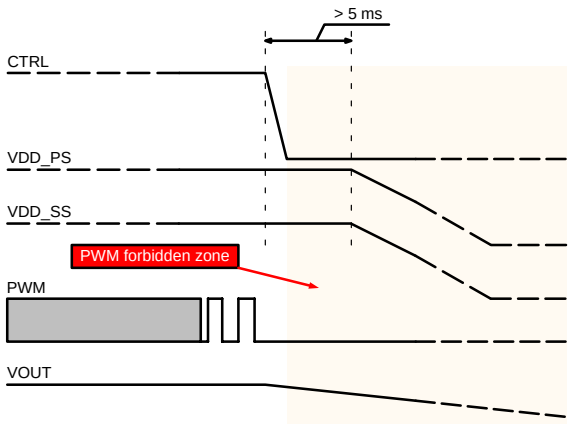


Figure 23. VDD Power Supply Timing Sequence During Power Down

PCB Layout Guideline

There are several loops with the high frequency pulsing current, including the input voltage loop and two gate driver loops. It is critical to keep the loop impedance as low as possible. All of the high current paths, such as VIN, SW and PGND, should be short and wide for low parasitic inductance and resistance. This helps achieve a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Input ceramic bypass capacitors must be close to the VIN and PGND pins. This reduces the high−current power loop inductance and the input current ripple induced by the power MOSFET switching operation.

The SW copper trace serves two purposes. In addition to being the high−frequency current path from the FDMF8811 package to the output inductor, it serves as a heat sink for the low−side MOSFET in the FDMF8811 package. The trace should be short and wide enough to present a low−impedance path for the high−frequency, high−current flow between the FDMF8811 and inductor. The short and wide trace minimizes electrical losses as well as the FDMF8811 temperature rises.

Note that the SW node is a high−voltage and high−frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace acts as a heat sink for the low−side MOSFET, balance using the largest area possible to improve FDMF8811 cooling while maintaining acceptable noise emission.

An output inductor should be located close to the FDMF8811 to minimize the power loss due to the SW copper trace. Care should also be taken so the inductor dissipation does not heat the FDMF8811.

POWERTRENCH MOSFETs are used in the output stage and are effective at minimizing ringing due to fast switching. In most cases, no R&C snubber on SW node is required. If a snubber is used, it should be placed close to the SW and PGND pins.

The board layout should include a placeholder for small−value series boot resistor in series to the BOOT capacitor. The boot−loop size, including series RBOOT and CBOOT, should be as small as possible.

The boot resistor may be required when there is large ringing at SW pin, and it is effective to control the high−side MOSFET turn−on slew rate and SW voltage overshoot. RBOOT can improve noise operating margin if there is large switching noise due to ground bounce or high positive and negative SW ringing. Inserting a boot resistance lowers the FDMF8811 module efficiency. Efficiency versus switching noise trade−offs must be considered.

The VIN and PGND pins handle large current transients with frequency components greater than 100 MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is not recommended since this adds extra parasitic inductance to the power path. This added inductance in series with either the VIN or PGND pin degrades system noise immunity by increasing positive and negative SW ringing.

PGND pad and pins should be connected to the GND copper plane with multiple vias for stable grounding. Poor grounding can create a noise transient offset voltage level between PGND and VSS. This could lead to faulty operation of gate driver and MOSFETs.

Ringing at the BT pin is most effectively controlled by close placement of the boot capacitor. Do not add any additional capacitors between BT to PGND. This may lead to excess current flow through the BT diode, causing high power dissipation.

Put multiple vias on the VIN and VOUT copper areas to interconnect top, inner, and bottom layers to evenly distribute current flow and heat conduction. Do not put too many vias on the SW copper to avoid extra parasitic inductance and noise on the switching waveform. As long as efficiency and thermal performance are acceptable, place only one SW node copper on the top layer and put no vias on the SW copper to minimize switch node parasitic noise. Vias should be relatively large and of reasonably low inductance. Critical high−frequency components, such as RBOOT, CBOOT, R&C snubber, and bypass capacitors should be located as close to the respective FDMF8811 module pins as possible on the top layer of the PCB. If this is not feasible, they can be placed on board bottom side and their pins can be connected from bottom to top through a network of low−inductance vias..

Figure 24 and Figure 25 show example top layer layout of the FDMF8811s Full Bridge application on primary side and secondary side.

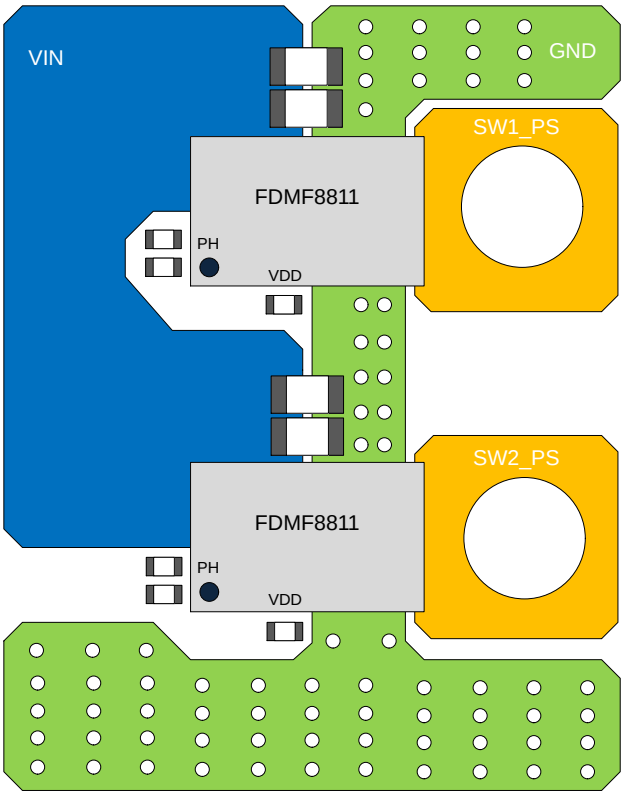


Figure 24. Example Layout of FDMF8811 Full Bridge Primary Side

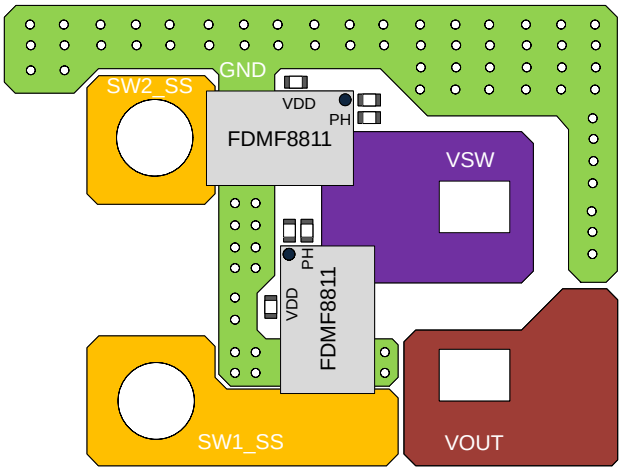


Figure 25. Example Layout of FDMF8811 Full Bridge Secondary

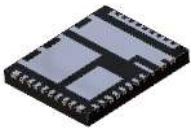
ORDERING INFORMATION

Device	Output Configuration	Marking	Package	Shipping†
FDMF8811	High−Side and Low−Side	FDMF8811	PQFN36 6 x 7.5, 0.5P	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

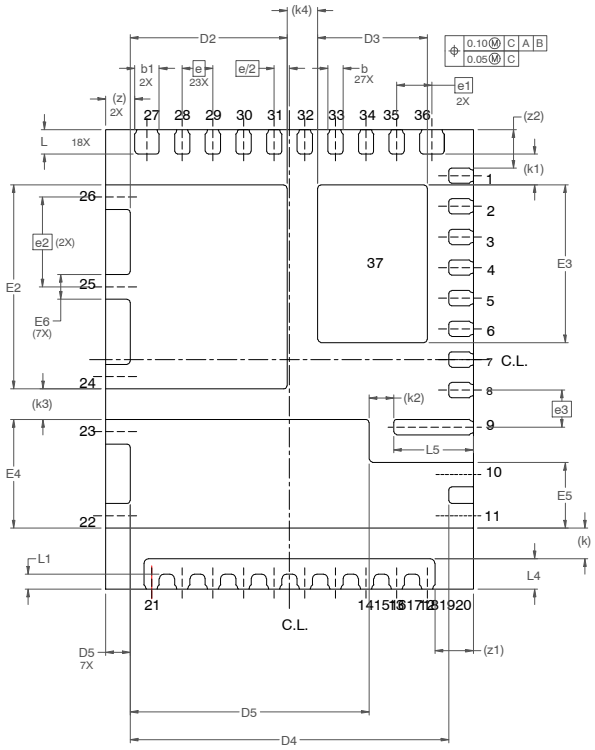
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

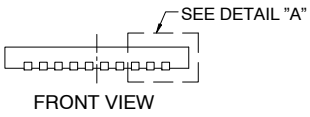


PQFN36 6X7.5, 0.5P
CASE 483BB
ISSUE A

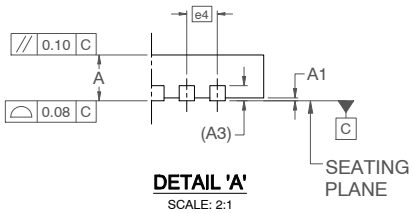
DATE 07 JUN 2021



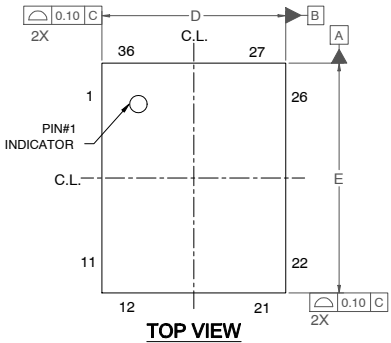
BOTTOM VIEW
SCALE: 2:1



FRONT VIEW



DETAIL 'A'
SCALE: 2:1



TOP VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
b1	0.20	0.40	0.30
D	5.90	6.00	6.10
D2	2.46	2.56	2.66
D3	1.69	1.79	1.89
D4	5.10	5.20	5.30
D5	3.80	3.90	4.00
D6	0.30	0.40	0.50
E	7.40	7.50	7.60
E2	3.22	3.32	3.42
E3	2.47	2.57	2.67
E4	1.67	1.77	1.87
E5	0.97	1.07	1.17
E6	0.35	0.40	0.45
e		0.50 BSC	
e/2		0.25 BSC	
e1		0.575 BSC	
e2		1.464 BSC	
e3		0.60 BSC	
k		0.50 REF	
k1		0.50 REF	
k2		0.40 REF	
k3		0.50 REF	
k4		0.50 REF	
L	0.30	0.40	0.50
L1	0.14	0.24	0.34
L4	0.40	0.50	0.60
L5	1.20	1.30	1.40
z		0.475 REF	
z1		0.625 REF	
z2		0.625 REF	

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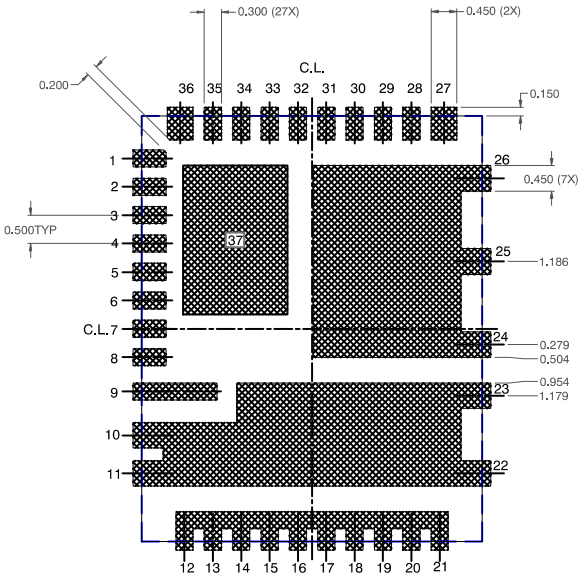
DESCRIPTION:	PQFN36 6X7.5, 0.5P	PAGE 1 OF 2

PQFN36 6X7.5, 0.5P
CASE 483BB
ISSUE A

DATE 07 JUN 202



LAND PATTERN RECOMMENDATION
SCALE 2:1

***FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.**

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC MO-220, ISSUE K.01, DATED AUG 2011.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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