



# STL60N32N3LL

Dual N-channel 30 V, 0.005  $\Omega$ , 15 A PowerFLAT™ 5x6 asymmetrical double island, STripFET™ Power MOSFET

## Features

Order code		V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STL60N32N3LL	Q <sub>1</sub>	30 V	< 0.0092 $\Omega$	13.6 A
	Q <sub>2</sub>	30 V	< 0.0055 $\Omega$	15 A

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

## Application

- Switching applications

## Description

This device is a dual N-channel Power MOSFET which utilizes the latest generation of design rules for ST's proprietary STripFET™ V and STripFET™ VI DeepGATE™ technology. The lowest available RDS(on)\* Qg in this chip scale package renders the device suitable for the most demanding DC-DC converter applications, where high power density is required.

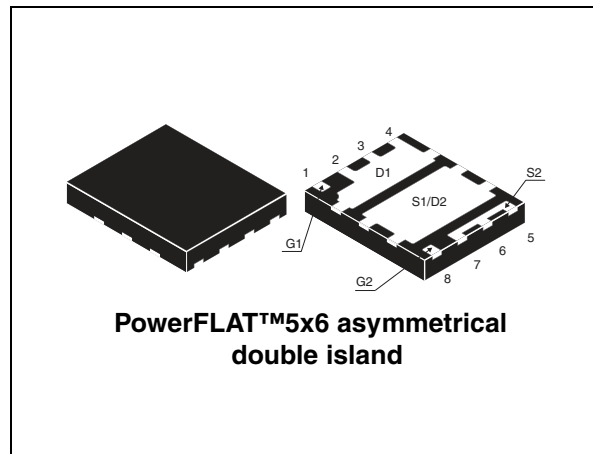


Figure 1. Internal schematic diagram

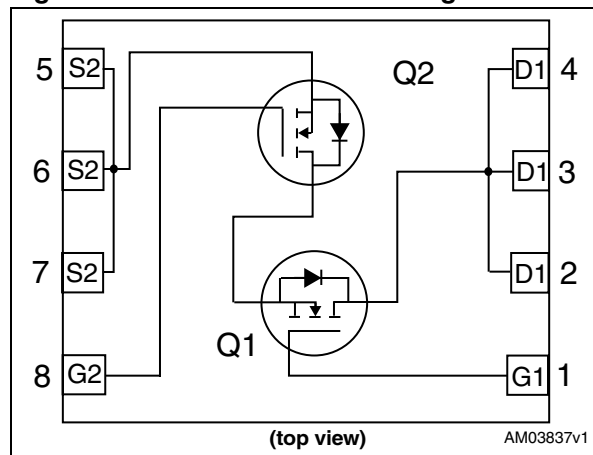


Table 1. Device summary

Order code	Marking	Package	Packaging
STL60N32N3LL	60N32N3LL	PowerFLAT™5x6 asymmetrical double island	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Type	Value	Unit
$V_{DS}$	Drain-source voltage	Q <sub>1</sub>	30	V
		Q <sub>2</sub>	30	V
$V_{GS}$	Gate- source voltage	Q <sub>1</sub>	± 20	V
		Q <sub>2</sub>	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	Q <sub>1</sub>	32	A
		Q <sub>2</sub>	60	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	Q <sub>1</sub>	23	A
		Q <sub>2</sub>	37	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	Q <sub>1</sub>	13.6	A
		Q <sub>2</sub>	15	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	Q <sub>1</sub>	8.5	A
		Q <sub>2</sub>	9.3	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	Q <sub>1</sub>	54.4	A
		Q <sub>2</sub>	60	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ °C}$	Q <sub>1</sub>	23	W
		Q <sub>2</sub>	50	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ °C}$	Q <sub>1</sub>	3.12	W
		Q <sub>2</sub>	3.12	W
$T_j$	Operating junction temperature		-55 to 150	°C
$T_{stg}$	Storage temperature			

1. This value is according to  $R_{thj-c}$
2. This value is according to  $R_{thj-pcb}$
3. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Type	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max		40	°C/W
$R_{thj-c}$	Thermal resistance junction-case	Q <sub>1</sub>	5.5	°C/W
		Q <sub>2</sub>	2.5	

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	Q <sub>1</sub>	30			V
			Q <sub>2</sub>	30			V
$I_{DSS}$	Zero gate voltage Drain current ( $V_{GS} = 0$ )	$V_{DS} = 30 V$	Q <sub>1</sub>			1	$\mu A$
			Q <sub>2</sub>			1	$\mu A$
$I_{DSS}$	Zero gate voltage Drain current ( $V_{GS} = 0$ )	$V_{DS} = 30 V, T_C = 125^{\circ}C$	Q <sub>1</sub>			10	$\mu A$
			Q <sub>2</sub>			10	$\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$	Q <sub>1</sub>			$\pm 100$	nA
			Q <sub>2</sub>			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	Q <sub>1</sub>	1			V
			Q <sub>2</sub>	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 6.8 A$ $V_{GS} = 10 V, I_D = 7.5 A$	Q <sub>1</sub>		0.0085	0.0092	$\Omega$
			Q <sub>2</sub>		0.005	0.0055	$\Omega$
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5 V, I_D = 6.8 A$ $V_{GS} = 4.5 V, I_D = 7.5 A$	Q <sub>1</sub>		0.0109	0.012	$\Omega$
			Q <sub>2</sub>		0.0065	0.0073	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$C_{ISS}$	Input capacitance	$V_{DS} = 25 V, f = 1 MHz,$ $V_{GS} = 0$	Q <sub>1</sub>	-	950	-	pF
			Q <sub>2</sub>	-	1690	-	pF
$C_{OSS}$	Output capacitance		Q <sub>1</sub>	-	193	-	pF
			Q <sub>2</sub>	-	291	-	pF
$C_{RSS}$	Reverse transfer capacitance		Q <sub>1</sub>	-	27.6	-	pF
			Q <sub>2</sub>	-	176	-	pF
$Q_g$	Total gate charge	$V_{DD} = 15 V, I_D = 15 A,$ $V_{GS} = 4.5 V$ <i>(see Figure 25)</i>	Q <sub>1</sub>	-	6.6	-	nC
$Q_{gs}$	Gate-source charge		Q <sub>1</sub>	-	3.3	-	nC
			Q <sub>2</sub>	-	8	-	nC
$Q_{gd}$	Gate-drain charge		Q <sub>1</sub>	-	2.4	-	nC
			Q <sub>2</sub>	-	6	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=7.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=4.5\text{ V}$ (see Figure 29)	$Q_1$	-	10.8	-	ns
$t_r$	Rise time		$Q_2$		9.5		ns
			$Q_1$		15.6		ns
			$Q_2$		30		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD}=15\text{ V}$ , $I_D=7.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=4.5\text{ V}$ (see Figure 29)	$Q_1$	-	14.2	-	ns
$t_f$	Fall time		$Q_2$		37		ns
			$Q_1$		6		ns
			$Q_2$		12		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current	$V_{DD}=15\text{ V}$ , $I_D=7.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=4.5\text{ V}$	$Q_1$	-		13.6	A
			$Q_2$			15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)	$V_{DD}=15\text{ V}$ , $I_D=7.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=4.5\text{ V}$	$Q_1$	-		54.4	A
			$Q_2$			60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=15\text{ A}$ , $V_{GS}=0$	$Q_1$	-		1.1	V
			$Q_2$			1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD}=15\text{ A}$ , $V_{DD}=15\text{ V}$ , $di/dt=100\text{ A}/\mu\text{s}$ , $T_j=150^\circ\text{C}$ (see Figure 29)	$Q_1$	-		20	ns
$Q_{rr}$	Reverse recovery charge		$Q_2$			24	ns
			$Q_1$			10	nC
			$Q_2$			16.8	nC
$I_{RRM}$	Reverse recovery current		$Q_1$			1	A
		$Q_2$	1.4	A			

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

### 2.1.1 Graphs for Q1

Figure 2. Safe operating area

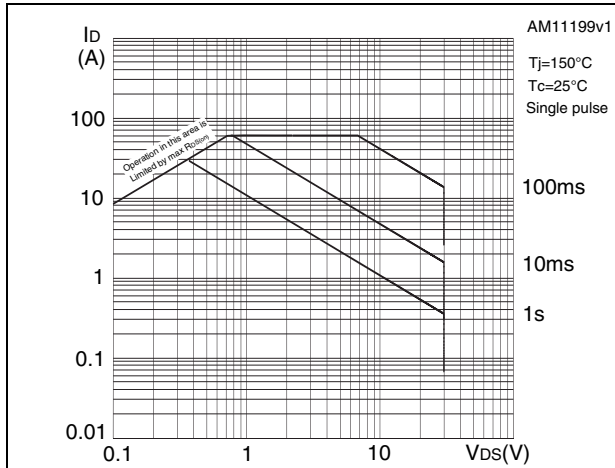


Figure 3. Thermal impedance

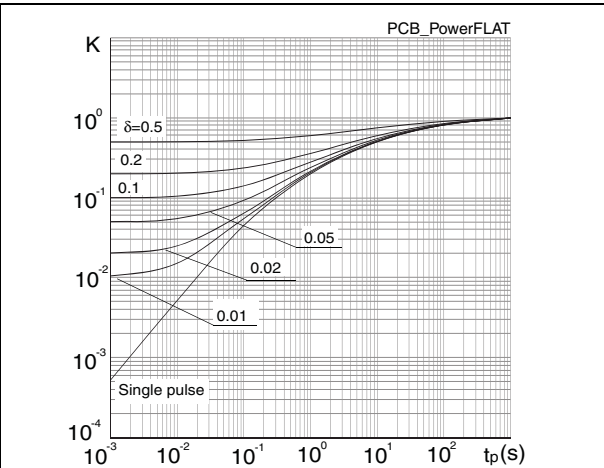


Figure 4. Output characteristics

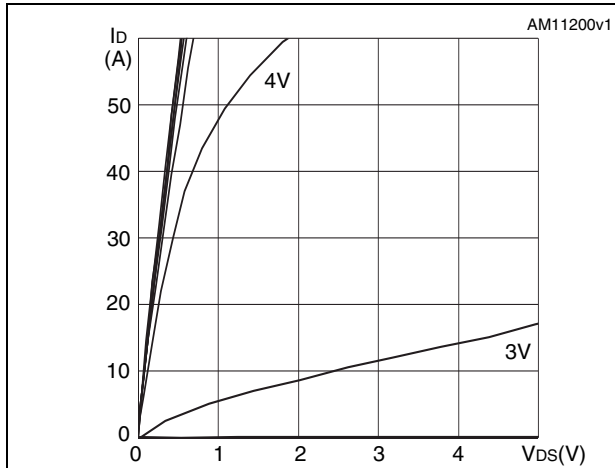


Figure 5. Transfer characteristics

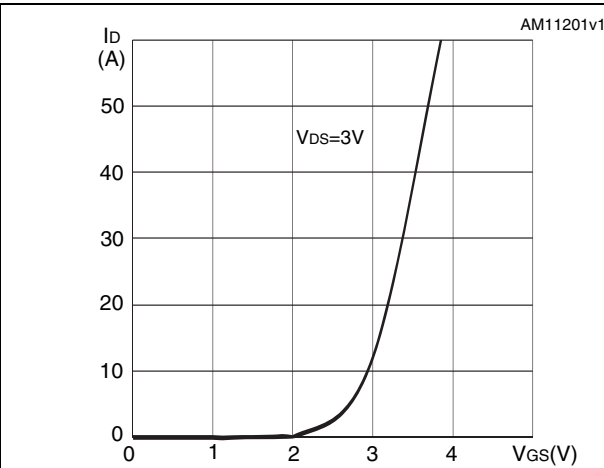


Figure 6. Normalized B<sub>VDS</sub> vs temperature

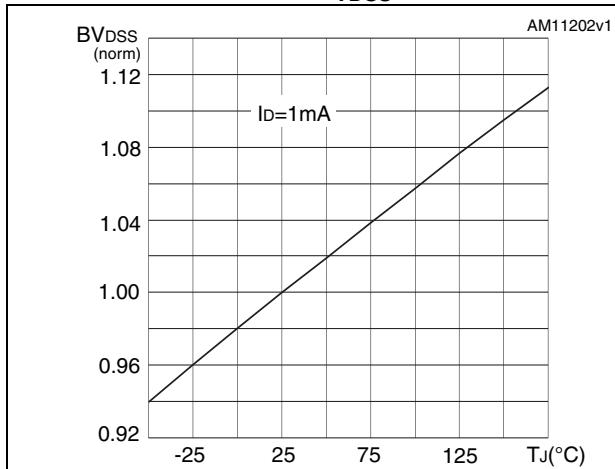
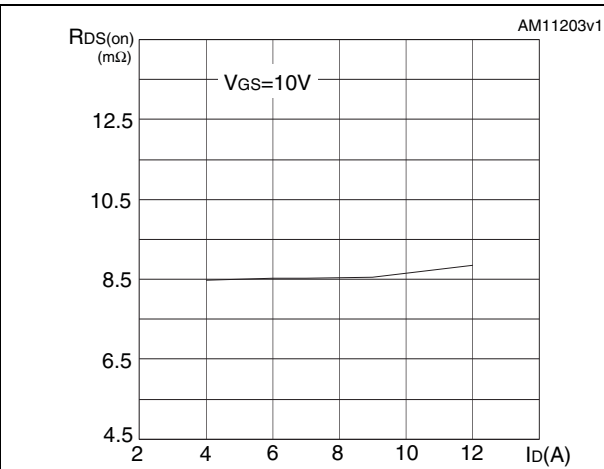
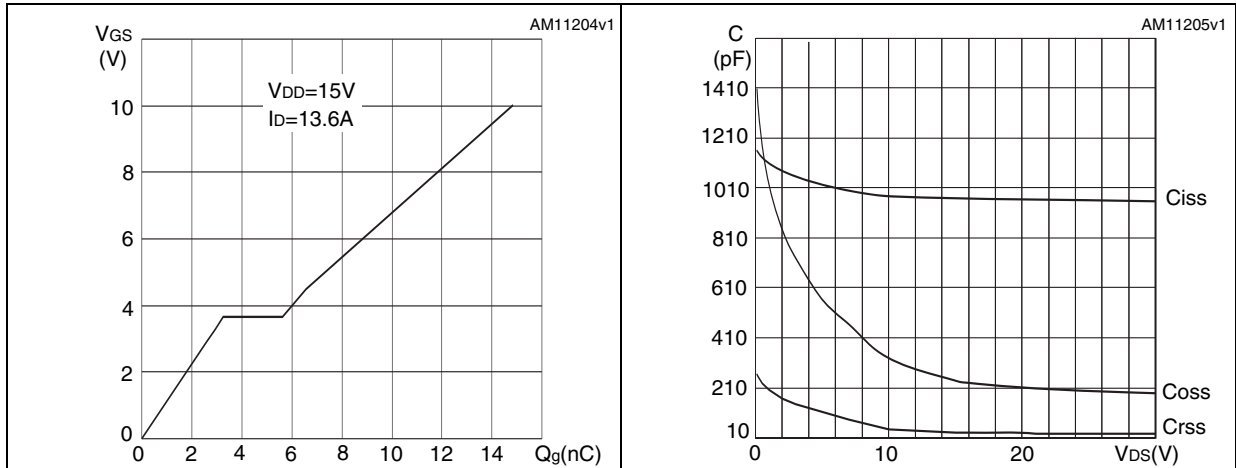


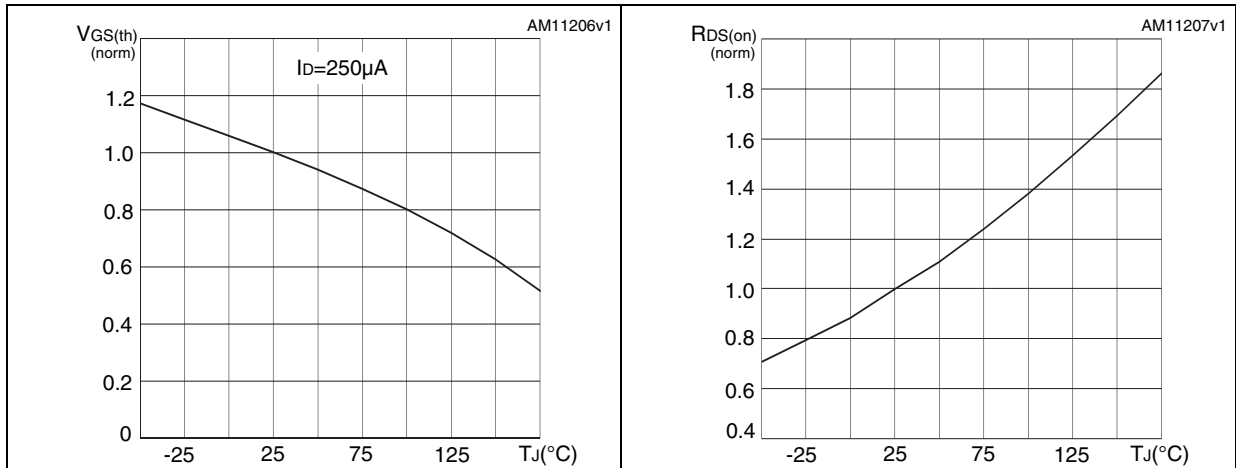
Figure 7. Static drain-source on resistance



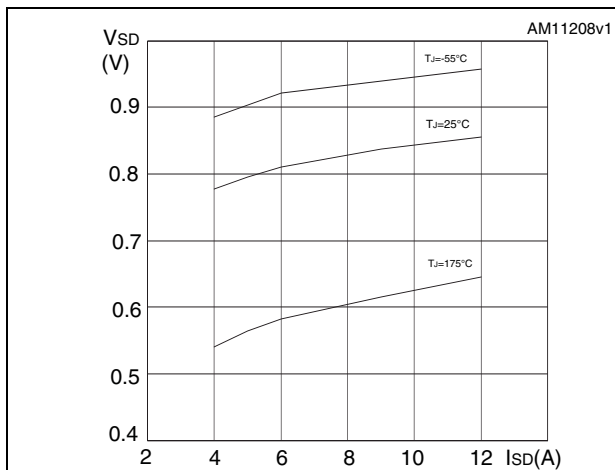
**Figure 8. Gate charge vs gate-source voltage** **Figure 9. Capacitance variations**



**Figure 10. Normalized gate threshold voltage vs temperature** **Figure 11. Normalized on resistance vs temperature**



**Figure 12. Source-drain diode forward characteristics**



2.1.2 Graphs for Q2

Figure 13. Safe operating area

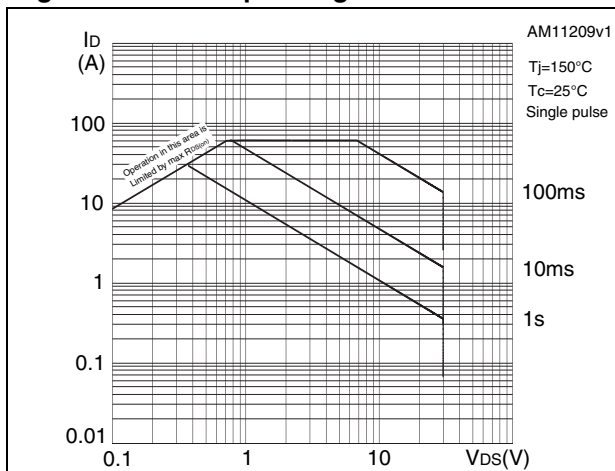


Figure 14. Thermal impedance

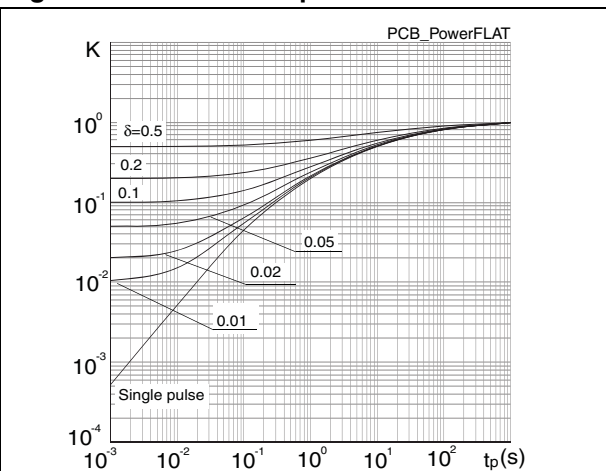


Figure 15. Output characteristics

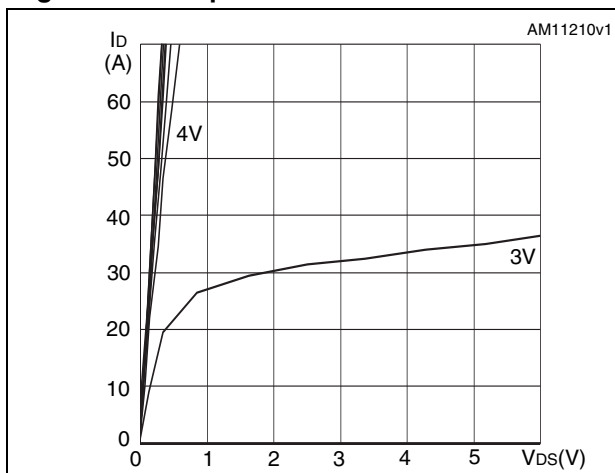


Figure 16. Transfer characteristics

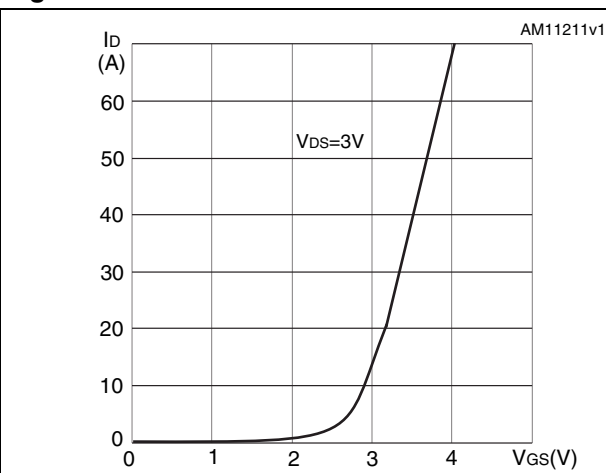


Figure 17. Normalized BV<sub>DSS</sub> vs temperature

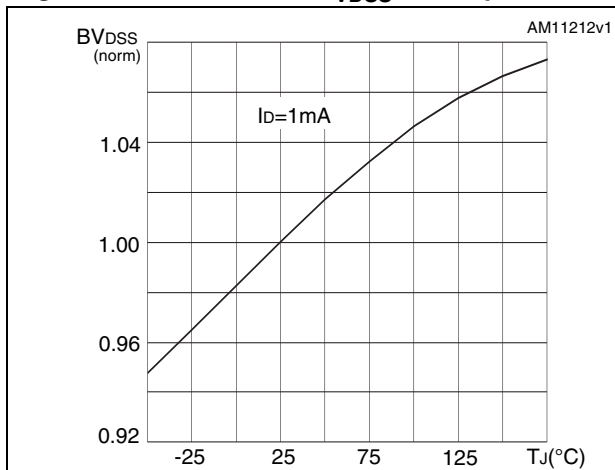


Figure 18. Static drain-source on resistance

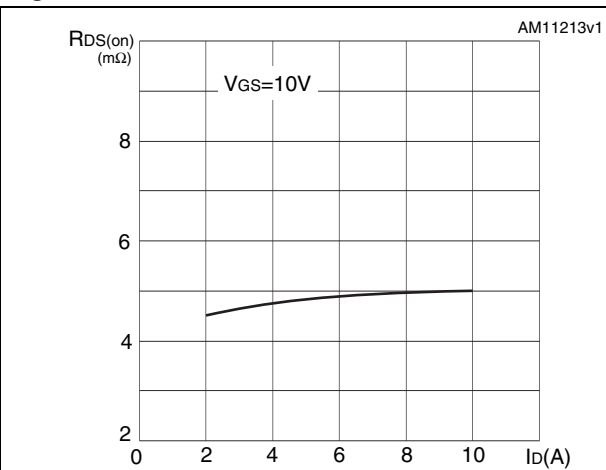




Figure 19. Gate charge vs gate-source voltage Figure 20. Capacitance variations

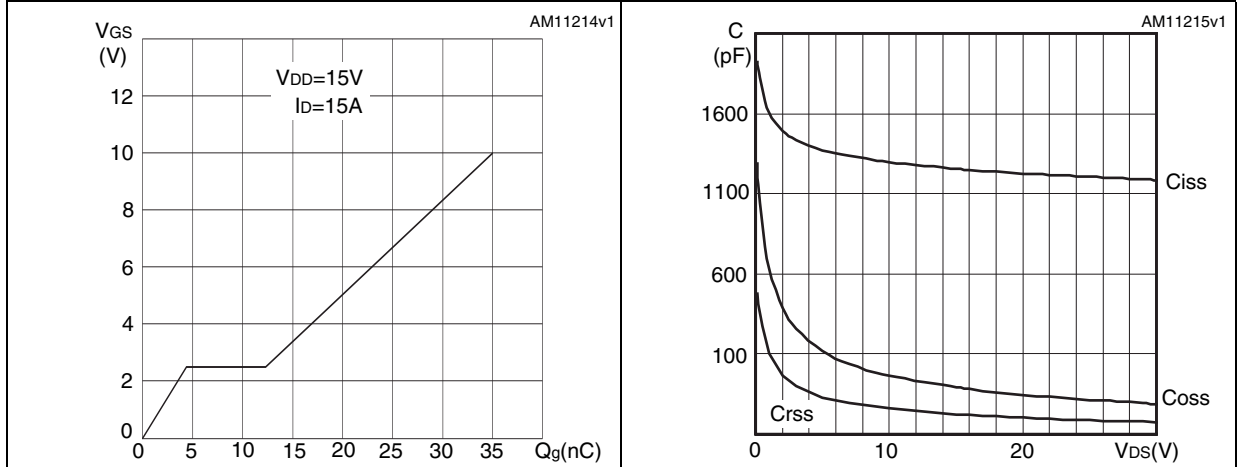


Figure 21. Normalized gate threshold voltage vs temperature Figure 22. Normalized on resistance vs temperature

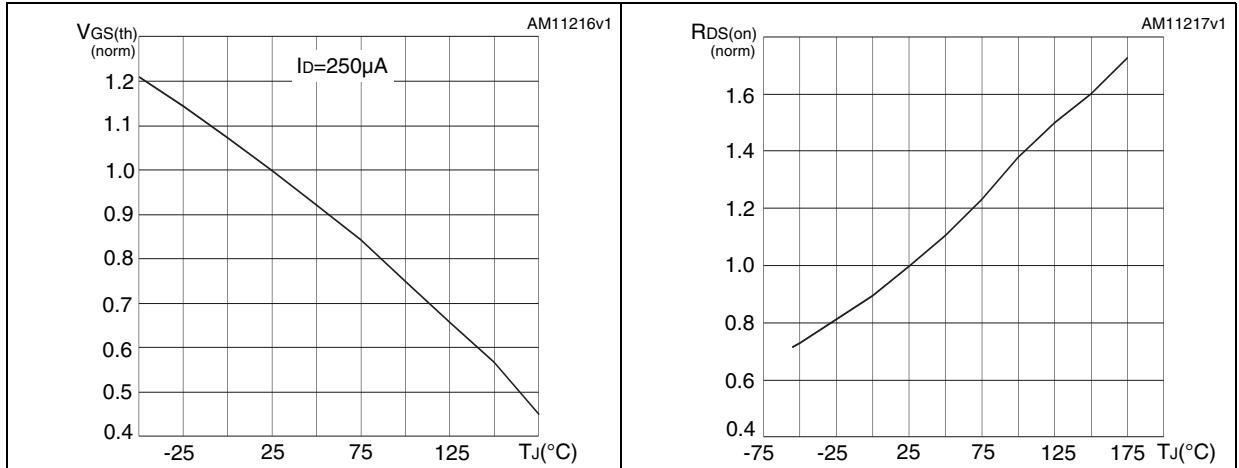
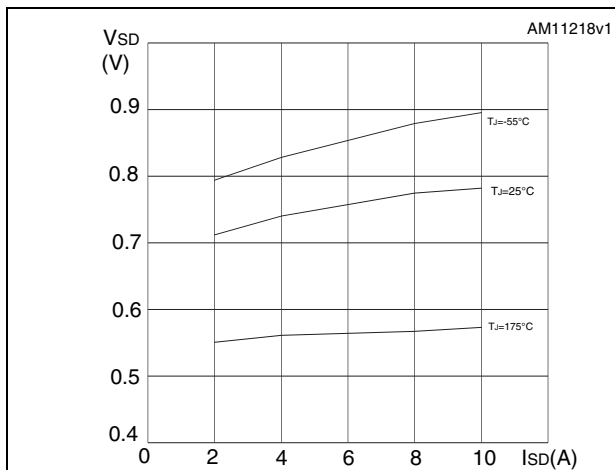
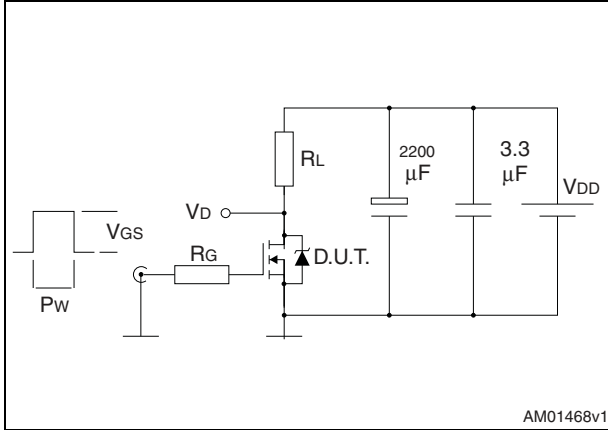


Figure 23. Source-drain diode forward characteristics



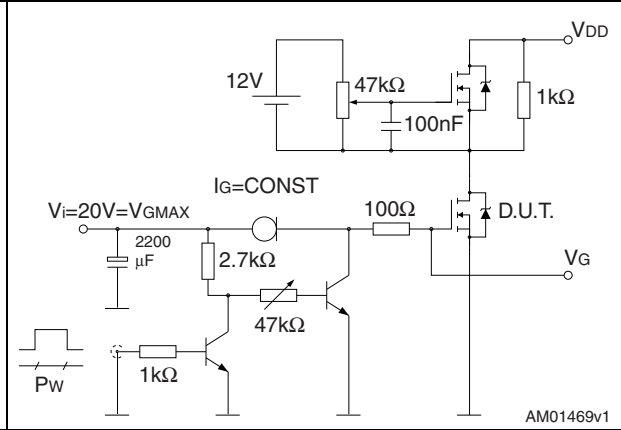
### 3 Test circuits

**Figure 24. Switching times test circuit for resistive load**



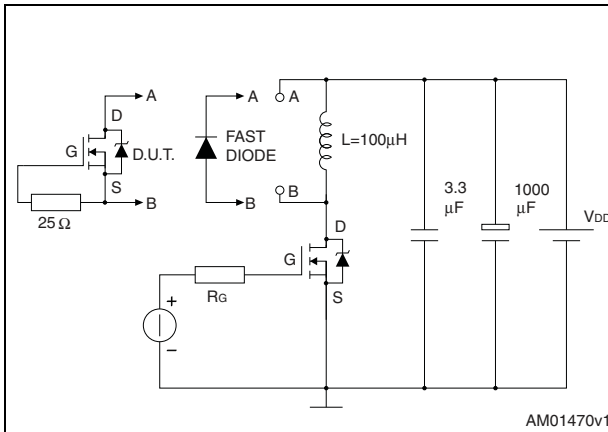
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**Figure 25. Gate charge test circuit**



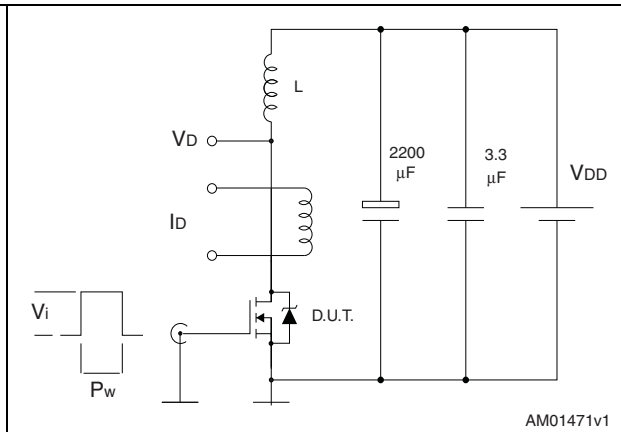
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**Figure 26. Test circuit for inductive load switching and diode recovery times**



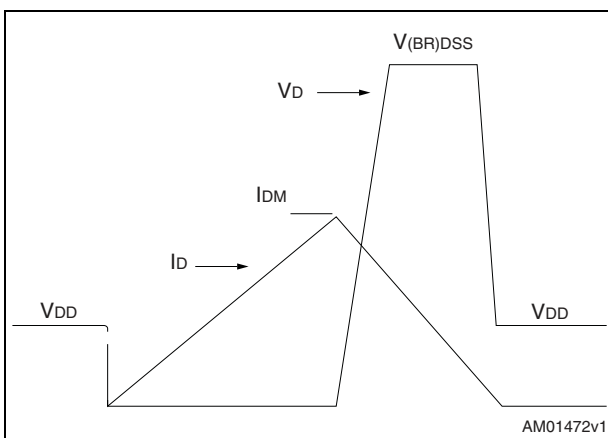
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**Figure 27. Unclamped inductive load test circuit**



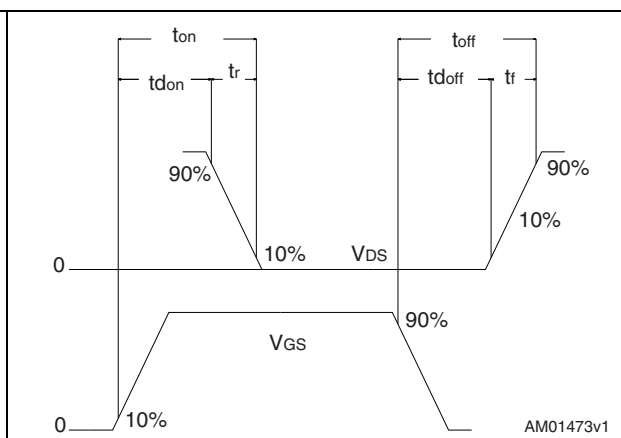
AM01471v1

**Figure 28. Unclamped inductive waveform**



AM01472v1

**Figure 29. Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 8. PowerFLAT™ 5x6 asymmetrical double island dimensions**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1			0.05
b	0.45		0.55
D	4.90	5.00	5.10
E	5.90	6.00	6.10
e		1.27	
L	0.40		0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 30. Package drawing

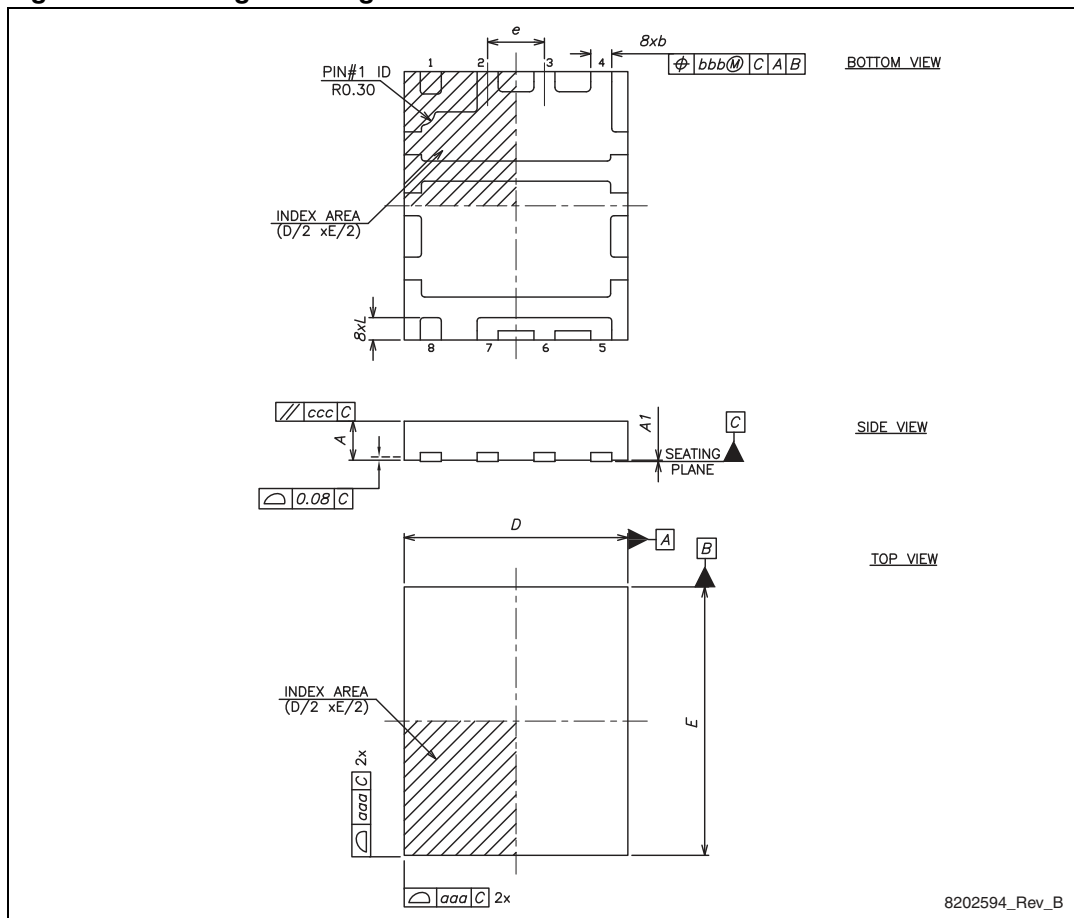
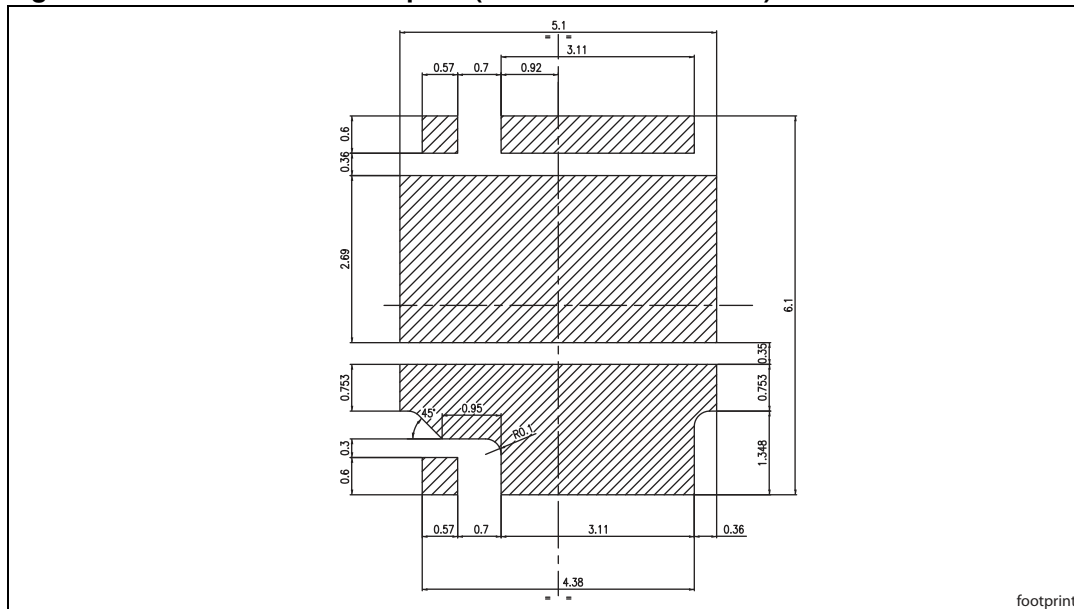


Figure 31. Recommended footprint (dimensions are in mm)



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
15-Mar-2010	1	First release
07-Feb-2011	2	Document status promoted from target specification to preliminary data.
21-Feb-2012	3	Document status promoted from preliminary data to datasheet. <i>Section 2.1: Electrical characteristics (curves)</i> has been added. <i>Section 4: Package mechanical data</i> has been updated. Minor text changes.

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