*Preliminary Information*

# MC68360 New Features on REV B

**February 1, 1994**

Some new features have been added to the XC68360 Revision B device. The uses of these new features are not required with an exception of hardware device errata fixes. The main purpose of the revision B device is to fix the errata items that is described on the QUICC Device Errata as "will be fixed on rev B".

Revision B device is visually marked with mask number C69T. The RISC revision number in the XC68360 at address (MiscBase+$00) has the value $0002. Revision A0 device has a mask number 0C63T, and revision A1 has a mask number 1C63T. Both revisions A0 and A1 have microcode revision number of $0001.

**NOTE**

The following information is not described in the MC68360 User's Manual (MC68360UM/AD). The use of this document along with QUICC Device Errata, QUICC Users Manual Errata and the User's Manual and Centronics Specification will fully describe revision B device operation.

## SCC

### HDLC BUS

HDLC MODE REGISTER (PSMR)

The HDLC mode register (PSMR) have two additional defined bits. The width and the location of the register has not changed. The definition of the two new bits are as follows.

Bit 2 BPM (HDLC BUS Priority Mode)

This bit determines the number of idle bits needed to be counted prior to a frame transmission after a successful transmission.

0 = 10 bits
1 = 9 bits

Bit 1 BCM (HDLC BUS Collision Sense Mode)

This bit determines the sample point of collision detection.

0 = collision is sensed after 1/2 bit delay (or at3/4 bit delay if the clock duty cycle is 25%).
1 = collision is sensed after one bit delay

**Ethernet**

1 Heart Beat window

The Heart Beat window was increased from 2µSec to 4µSec. It is measured from Carrier Sense negation. This was changed in order to conform to the 802.3 standard.

2 Ethernet Mode Register (PCMR)

The Ethernet Mode Register (PSMR) have one additional defined bit to support full duplex Ethernet. The width and the location of the register has not changed. The definition of the new bit is as follows.

Bit 0 FDE (Full Duplex Ethernet)

This bit when set enables full duplex Ethernet operation.

0 = Disable full duplex ethernet.
1 = Enable full duplex ethernet.

**NOTE**

When this bit is set to 1 the LPB bit must also be set to 1.

3 Ethernet receive buffer descriptor.

The description of collision bit (CL) in the Ethernet receive buffer descriptor was corrected. The collision bit will be set if the reception was terminated by the negation of RENA. This may not be a late collision and the frame could be longer than 64 bytes.

## SMC

GCI has a new spec - Please see QUICC User's Manual Errata.

## PIP

Centronics support

Centronics feature is now supported in hardware. For more detail, please see the centronics specifications.

## IDMA

Channel status register (CSR)

IDMA channel status register (CSR) was changed that a clear of Normal channel transfer done (DONE), Bus Error Source (BDS) or Bus Error Destination (BED) event is no longer required prior to a new transfer. These bits should be clead depending on the channel mask register (CMR) setting to avoid any unnecessary interrupt generation.

## SIGNAL DESCRIPTION

TRIS Pin

On Revision A, assertion of TRIS* pin did not tristate clock out pins (CLKO1 and CLKO2). On revision B hardware fix was implemented so both clock out pins will be tristated with assertion of TRIS* pin.

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