PCK940L

Low voltage 1 : 18 clock distribution chip

Rev. 01 — 4 April 2006 | Product data sheet

1. General description

The PCK940L is a 1 : 18 low voltage clock distribution chip with 2.5 V or 3.3 V LVCMOS output capabilities. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 18 outputs are 2.5 V or 3.3 V LVCMOS compatible and feature the drive strength to drive 50 Ω series or parallel terminated transmission lines. With output-to-output skews of 150 ps, the PCK940L is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5 V outputs also make the device ideal for supplying clocks for a high performance microprocessor based design.

With a low output impedance of approximately 20 Ω, in both the HIGH and LOW logic states, the output buffers of the PCK940L are ideal for driving series terminated transmission lines. With an output impedance of 20 Ω, the PCK940L has the capability of driving two series terminated transmission lines from each output. This gives the PCK940L an effective fan-out of 1 : 36. If a lower output impedance is desired, please see the PCK942C data sheet.

The differential LVPECL inputs of the PCK940L allow the device to interface directly with a LVPECL fan-out buffer like the PCKEP111 to build very wide clock fan-out trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLKSEL pin will select the LVCMOS level clock input. All inputs of the PCK940L have internal pull-up/pull-down resistors so they can be left open if unused.

The PCK940L is a single or dual supply device. The device power supply offers a high degree of flexibility. The device can operate with a 3.3 V core and 3.3 V output, a 3.3 V core and 2.5 V outputs, as well as a 2.5 V core and 2.5 V outputs. The 32-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead LQFP package has a 7 mm × 7 mm body size with a conservative 0.8 mm pin spacing.

2. Features

- LVPECL or LVCMOS clock input
- 2.5 V LVCMOS outputs for Pentium II microprocessor support
- 150 ps maximum output-to-output skew
- Maximum output frequency of 250 MHz at 3.3 V V_{CC}
- 32-lead LQFP packaging

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- Dual or single supply voltage:
  - Dual V_{CC} supply voltage, 3.3 V core and 2.5 V output
  - Single 3.3 V V_{CC} supply voltage for 3.3 V outputs
  - Single 2.5 V V_{CC} supply voltage for 2.5 V I/O

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCK940LBD	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

4. Functional diagram

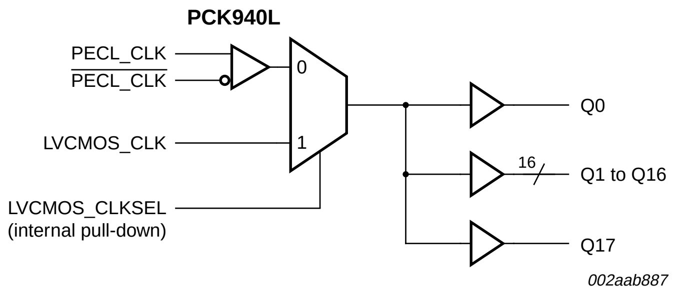

Fig 1. Functional diagram of PCK940L

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5. Pinning information

5.1 Pinning

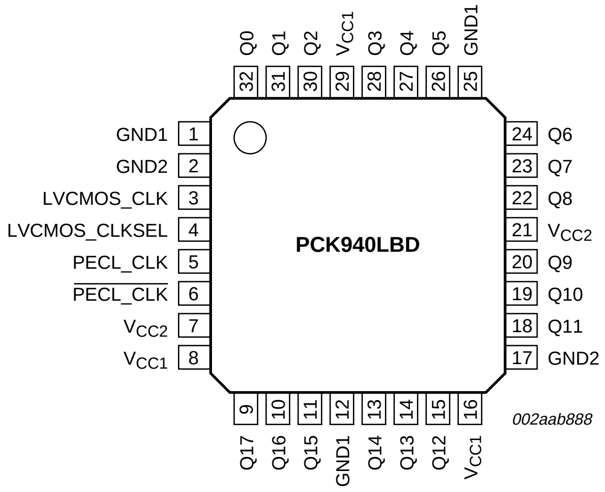

Fig 2. Pin configuration for LQFP32

5.2 Pin description

Table 2. Pin description

Symbol	Pin	I/O	Type	Description
PECL_CLK	5	input	LVPECL	reference clock input
$\overline{\text{PECL\_CLK}}$	6	input	LVPECL	reference clock input (active LOW)
LVCMOS_CLK	3	input	LVCMOS	alternative reference clock input
LVCMOS_CLKSEL	4	input	LVCMOS	clock source select
Q0 to Q17	32, 31, 30, 28, 27, 26, 24, 23, 22, 20, 19, 18, 15, 14, 11, 10, 9	output	LVCMOS	clock outputs
GND1	1, 12, 25	-	supply	output negative power supply
GND2	2, 17	-	supply	core negative power supply
V_{CC1}	8, 16, 29	-	supply	output positive power supply
V_{CC2}	7, 21	-	supply	core positive power supply

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6. Functional description

Refer to Figure 1 “Functional diagram of PCK940L”.

6.1 Function table

Table 3. Function table

LVCMOS_CLKSEL	Input
0	PECL_CLK
1	LVCMOS_CLK

Table 4. Power supply voltage

Supply pin	Voltage level
V_{CC2}	2.5 V or 3.3 V ± 5 %
V_{CC1}	2.5 V or 3.3 V ± 5 %

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+3.6	V
V_I	input voltage		–0.3	V_{DD} + 0.3	V
I_I	input current		-	±20	mA
T_{stg}	storage temperature		–40	+125	°C

8. Static characteristics

Table 6. Static characteristics (3.3 V V_{CC}, 3.3 V outputs)

T_{amb} = 0 °C to 70 °C; V_{CC2} = 3.3 V ± 5 %; V_{CC1} = 3.3 V ± 5 %

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	LVCMOS_CLK	2.4	-	V_{CC2}	V
V_{IL}	LOW-level input voltage	LVCMOS_CLK	-	-	0.8	V
$V_{i(p-p)}$	peak-to-peak input voltage	PECL_CLK	500	-	1000	mV
V_{ICR}	common mode input voltage range	PECL_CLK	V_{CC} – 1.4	-	V_{CC} – 0.6	V
V_{OH}	HIGH-level output voltage	I_{OH} = –20 mA	2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OH} = 20 mA	-	-	0.5	V
I_I	input current		-	-	±200	µA
C_i	input capacitance		-	4.0	-	pF
C_{PD}	power dissipation capacitance	per output	-	10	-	pF
Z_o	output impedance		18	23	28	Ω
$I_{CC(max)}$	maximum supply current		-	0.5	1.0	mA

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Table 7. Static characteristics (3.3 V V_{CC}, 2.5 V outputs)

T_{amb} = 0 °C to 70 °C; V_{CC2} = 3.3 V ± 5 %; V_{CC1} = 2.5 V ± 5 %

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	LVCMOS_CLK	2.4	-	V_{CC2}	V
V_{IL}	LOW-level input voltage	LVCMOS_CLK	-	-	0.8	V
$V_{i(p-p)}$	peak-to-peak input voltage	PECL_CLK	500	-	1000	mV
V_{ICR}	common mode input voltage range	PECL_CLK	V_{CC} – 1.4	-	V_{CC} – 0.6	V
V_{OH}	HIGH-level output voltage	I_{OH} = –20 mA	1.8	-	-	V
V_{OL}	LOW-level output voltage	I_{OH} = 20 mA	-	-	0.5	V
I_I	input current		-	-	±200	μA
C_i	input capacitance		-	4.0	-	pF
C_{PD}	power dissipation capacitance	per output	-	10	-	pF
Z_o	output impedance		-	23	-	Ω
$I_{CC(max)}$	maximum supply current		-	0.5	1.0	mA

Table 8. Static characteristics (2.5 V V_{CC}, 2.5 V output)

T_{amb} = 0 °C to 70 °C; V_{CC2} = 2.5 V ± 5 %; V_{CC1} = 2.5 V ± 5 %

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	LVCMOS_CLK	2.0	-	V_{CC2}	V
V_{IL}	LOW-level input voltage	LVCMOS_CLK	-	-	0.8	V
$V_{i(p-p)}$	peak-to-peak input voltage	PECL_CLK	500	-	1000	mV
V_{ICR}	common mode input voltage range	PECL_CLK	V_{CC} – 1.0	-	V_{CC} – 0.6	V
V_{OH}	HIGH-level output voltage	I_{OH} = –20 mA	1.8	-	-	V
V_{OL}	LOW-level output voltage	I_{OH} = 20 mA	-	-	0.5	V
I_I	input current		-	-	±200	μA
C_i	input capacitance		-	4.0	-	pF
C_{PD}	power dissipation capacitance	per output	-	10	-	pF
Z_o	output impedance		18	23	28	Ω
$I_{CC(max)}$	maximum supply current		-	0.5	1.0	mA

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9. Dynamic characteristics

Table 9. Dynamic characteristics (3.3 V V_{CC}, 3.3 V output)

T_{amb} = 0 °C to 70 °C; V_{CC2} = 3.3 V ± 5 %; V_{CC1} = 3.3 V ± 5 %

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{oper(max)}$	maximum operating frequency			-	-	250	MHz
t_{PLH}	LOW-to-HIGH propagation delay	PECL_CLK ≤ 150 MHz	[1]	2.0	2.7	3.8	ns
		LVCMOS_CLK ≤ 150 MHz	[1]	1.8	2.5	3.0	ns
		PECL_CLK > 150 MHz		2.0	2.9	3.7	ns
		LVCMOS_CLK > 150 MHz		1.8	2.4	3.2	ns
$t_{sk(o)}$	output skew time	output-to-output					
		PECL_CLK	[1]	-	-	200	ps
		LVCMOS_CLK	[1]	-	-	150	ps
$t_{sk(pr)}$	process skew time	part-to-part					
		PECL_CLK < 150 MHz	[1][2]	-	-	1.4	ns
		LVCMOS_CLK < 150 MHz	[1][2]	-	-	1.2	ns
		PECL_CLK > 150 MHz	[1][2]	-	-	1.7	ns
		LVCMOS_CLK > 150 MHz	[1][2]	-	-	1.4	ns
		PECL_CLK	[1][3]	-	-	850	ps
		LVCMOS_CLK	[1][3]	-	-	750	ps
δ_o	output duty cycle	LCVMOS_CLK; input δ = 50 %					
		f_{clk} < 134 MHz		45	50	55	%
		f_{clk} ≤ 250 MHz		40	50	60	%
		PECL_CLK; input δ = 50 %					
		f_{clk} < 134 MHz		35	50	65	%
		f_{clk} ≤ 250 MHz		40	50	60	%
t_r	rise time	output; from 0.5 V to 2.4 V		0.3	-	1.1	ns
t_f	fall time	output; from 2.4 V to 0.5 V		0.3	-	1.1	ns

[1] Tested using standard input levels, production tested at 150 MHz.

[2] Across temperature and voltage ranges, includes output skew.

[3] For a specific temperature and voltage, includes output skew.

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Table 10. Dynamic characteristics (3.3 V V_{CC}, 2.5 V output)

T_{amb} = 0 °C to 70 °C; V_{CC2} = 3.3 V ± 5 %; V_{CC1} = 2.5 V ± 5 %

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{oper(max)}$	maximum operating frequency			-	-	250	MHz
t_{PLH}	LOW-to-HIGH propagation delay	PECL_CLK ≤ 150 MHz	[1]	2.0	2.8	4.0	ns
		LVCMOS_CLK ≤ 150 MHz	[1]	1.7	2.5	3.0	ns
		PECL_CLK > 150 MHz		2.0	2.9	4.0	ns
		LVCMOS_CLK > 150 MHz		1.8	2.5	3.3	ns
$t_{sk(o)}$	output skew time	output-to-output					
		PECL_CLK	[1]	-	-	300	ps
		LVCMOS_CLK	[1]	-	-	150	ps
$t_{sk(pr)}$	process skew time	part-to-part					
		PECL_CLK < 150 MHz	[1][2]	-	-	1.5	ns
		LVCMOS_CLK < 150 MHz	[1][2]	-	-	1.3	ns
		PECL_CLK > 150 MHz	[1][2]	-	-	1.8	ns
		LVCMOS_CLK > 150 MHz	[1][2]	-	-	1.5	ns
		PECL_CLK	[1][3]	-	-	850	ps
		LVCMOS_CLK	[1][3]	-	-	750	ps
δ_o	output duty cycle	LCVMOS_CLK; input δ = 50 %					
		f_{clk} < 134 MHz		45	50	55	%
		f_{clk} ≤ 250 MHz		40	50	60	%
		PECL_CLK; input δ = 50 %					
		f_{clk} < 134 MHz		35	50	65	%
		f_{clk} ≤ 250 MHz		40	50	60	%
t_r	rise time	output; from 0.5 V to 1.8 V		0.3	-	1.2	ns
t_f	fall time	output; from 1.8 V to 0.5 V		0.3	-	1.2	ns

[1] Tested using standard input levels, production tested at 150 MHz.

[2] Across temperature and voltage ranges, includes output skew.

[3] For a specific temperature and voltage, includes output skew.

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Table 11. Dynamic characteristics (2.5 V V_{CC}, 2.5 V output)
T_{amb} = 0 °C to 70 °C; V_{CC2} = 2.5 V ± 5 %; V_{CC1} = 2.5 V ± 5 %

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{oper(max)}$	maximum operating frequency			-	-	200	MHz
t_{PLH}	LOW-to-HIGH propagation delay	PECL_CLK ≤ 150 MHz	[1]	2.6	4.0	5.2	ns
		LVCMOS_CLK ≤ 150 MHz	[1]	2.3	3.1	4.0	ns
		PECL_CLK > 150 MHz		2.8	3.8	5.0	ns
		LVCMOS_CLK > 150 MHz		2.3	3.1	4.0	ns
$t_{sk(o)}$	output skew time	output-to-output					
		PECL_CLK	[1]	-	-	300	ps
		LVCMOS_CLK	[1]	-	-	200	ps
$t_{sk(pr)}$	process skew time	part-to-part					
		PECL_CLK < 150 MHz	[1][2]	-	-	2.6	ns
		LVCMOS_CLK < 150 MHz	[1][2]	-	-	1.7	ns
		PECL_CLK > 150 MHz	[1][2]	-	-	2.2	ns
		LVCMOS_CLK > 150 MHz	[1][2]	-	-	1.7	ns
		PECL_CLK	[1][3]	-	-	1.2	ns
		LVCMOS_CLK	[1][3]	-	-	1.0	ns
δ_o	output duty cycle	LCVMOS_CLK; input δ = 50 %					
		f_{clk} < 134 MHz		45	50	55	%
		f_{clk} ≤ 250 MHz		40	50	60	%
		PECL_CLK; input δ = 50 %					
		f_{clk} < 134 MHz		35	50	65	%
		f_{clk} ≤ 250 MHz		40	50	60	%
t_r	rise time	output; from 0.5 V to 1.8 V		0.3	-	1.2	ns
t_f	fall time	output; from 1.8 V to 0.5 V		0.3	-	1.2	ns

[1] Tested using standard input levels, production tested at 150 MHz.

[2] Across temperature and voltage ranges, includes output skew.

[3] For a specific temperature and voltage, includes output skew.

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9.1 Timing diagrams

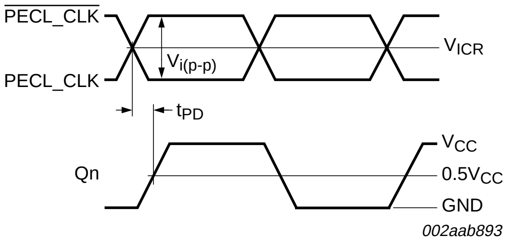


Fig 3. Propagation delay (t_{PD}) test reference

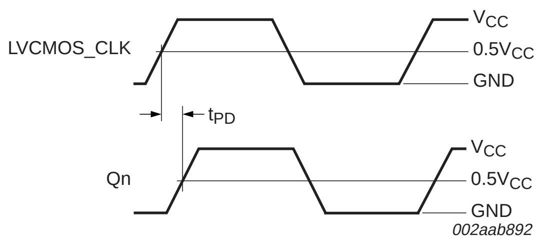
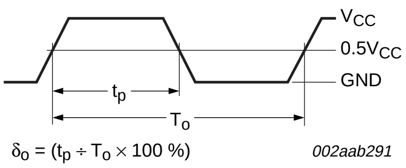
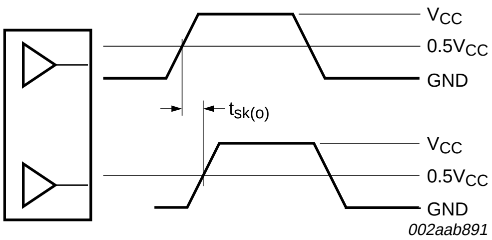


Fig 4. LVCMOS_CLK propagation delay (t_{PD}) test reference



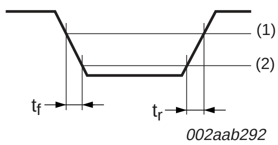
The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Fig 5. Output duty cycle



The pin-to-pin skew is defined as the worst-case difference in propagation delay between any two similar delay paths within a single device.

Fig 6. Output-to-output skew



(1) output 2.4 V; input 2.0 V (V_{CC} = 3.3 V)
output 1.8 V; input 1.7 V (V_{CC} = 2.5 V)

(2) output 0.55 V; input 0.8 V (V_{CC} = 3.3 V)
output 0.6 V; input 0.7 V (V_{CC} = 2.5 V)

Fig 7. Transition time test reference

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10. Test information

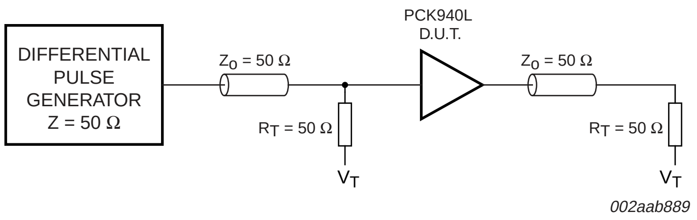

Fig 8. LVCMOS_CLK PCK940L AC test reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

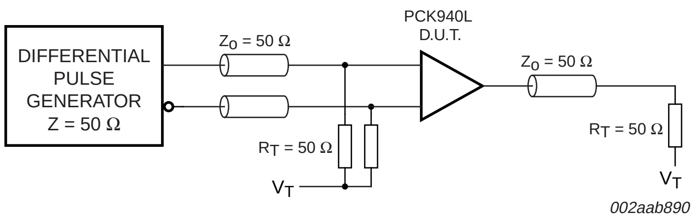

Fig 9. PECL_CLK PCK940L AC test reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

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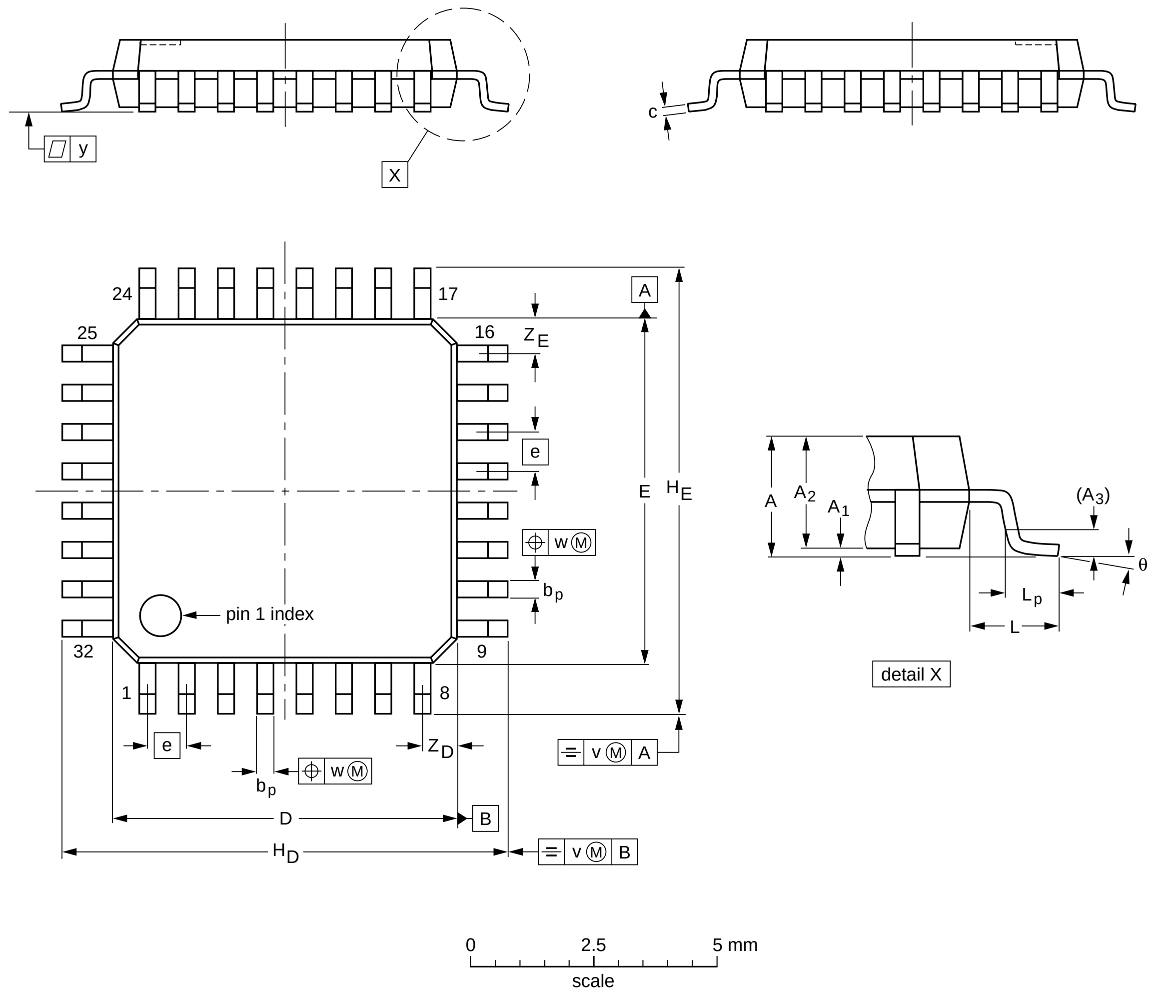
11. Package outline

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~03-02-25~~ 05-11-09

Fig 10. Package outline SOT358-1 (LQFP32)

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12. Soldering

12.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

12.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 260 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

12.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

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– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

12.5 Package related soldering information

Table 12. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

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[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVPECL	Low Voltage Positive Emitter Coupled Logic
PLL	Phase-Locked Loop

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCK940L_1	20060404	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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