AMC1035 Delta-Sigma Modulator With Bipolar Input of ±1 V and Reference Output of 2.5 V

1 Features

- Delta-sigma modulator optimized for voltage and temperature sensing:
  - ±1-V input voltage range
  - High differential input resistance: 1.6 GΩ (typ)
  - Integrated 2.5-V, ±5-mA reference for ratiometric measurement
- Excellent DC performance:
  - Offset error: ±0.5 mV (max)
  - Offset drift: ±6 µV/°C (max)
  - Gain error: ±0.25% (max)
  - Gain drift: ±45 ppm/°C (max)
  - Ratiometric gain drift: ±15 ppm/°C (max)
- Selectable manchester encoded or uncoded bitstream output
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- AC voltage and temperature sensing in industrial applications:
  - Motor drives
  - Photovoltaic inverters
  - Uninterruptible power supplies
  - Industrial transport systems

3 Description

The AMC1035 is a precision delta-sigma (ΔΣ) modulator that operates from a single 3.0-V to 5.5-V supply and with an externally supplied clock signal in the range of 9 MHz to 21 MHz. In Manchester mode, the specified clock range is 9 MHz to 11 MHz. The differential ±1-V input structure of the device is optimized for high noise environments typical for industrial applications.
Select the output bitstream of the AMC1035 to be Manchester coded to prevent setup and hold time requirement considerations of the receiving device and reduce overall circuit layout efforts. When used with a digital filter (such as integrated in the TMS320F28004x, TMS320F2807x or TMS320F2837x microcontroller families) to decimate the output bitstream, the device can achieve 16 bits of resolution with a dynamic range of 87 dB at a data rate of 82 kSPS.

The internal reference source of the AMC1035 supports ratiometric circuit architecture to minimize the negative impact of the supply voltage variation and temperature drift on the accuracy of the measurement.

The AMC1035 can also be used for AC power line voltage sensing with a digital isolator and isolated power supply.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1035	SOIC (8)	4.9 mm × 3.9 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Example

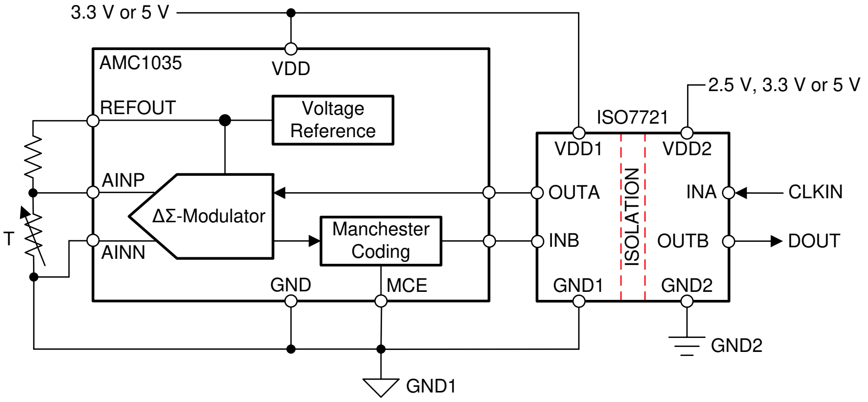


Table of Contents

---

4 Revision History

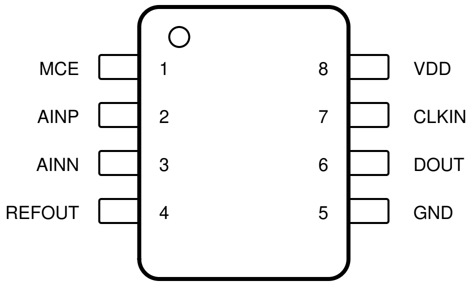
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2018) to Revision B	Page
• Deleted PSRR specification for T_A > 85°C from *Reference Output* section of *Electrical Characteristics* table	6
• Changed SINAD equation	22

Changes from Original (August 2018) to Revision A	Page
• Changed document status from Advance Information to Production Data	1

5 Pin Configuration and Functions

**D Package
8-Pin SOIC
Top View**



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	MCE	I	Manchester coding enabled, active high, with internal pulldown resistor (typical value: 200 kΩ). The polarity of this signal must not be changed when the clock signal is applied.
2	AINP	I	Noninverting analog input.
3	AINN	I	Inverting analog input.
4	REFOUT	O	Reference output: 2.5 V nominal, maximum ±5-mA sink and source capability.
5	GND	—	Ground reference.
6	DOUT	O	Modulator bitstream data output, updated with the rising edge of the clock signal present on CLKIN. This pin is a Manchester coded output if MCE is pulled high. Use the rising edge of the clock to latch the modulator bitstream at the input of the digital filter device.
7	CLKIN	I	Modulator clock input: 9 MHz to 21 MHz with an internal pulldown resistor (typical value: 200 kΩ). The clock signal must be applied continuously for proper device operation; see the *Clock Input* section for additional details.
8	VDD	—	Power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

	MIN	MAX	UNIT
Supply voltage, VDD to GND	–0.3	7	V
Analog input voltage at AINP, AINN	GND – 5	VDD + 0.5	V
Analog output voltage at REFOUT	GND – 0.5	VDD + 0.5	V
Digital input voltage at CLKIN or MCE	GND – 0.5	VDD + 0.5	V
Digital output voltage at DOUT	GND – 0.5	VDD + 0.5	V
Input current to any pin except supply pins	–10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Supply voltage	VDD to GND	3.0	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{AINP} – V_{AINN}$		±1.25		V
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{AINP} – V_{AINN}$	–1		1	V
	Absolute common-mode input voltage (1)	$(V_{AINP} + V_{AINN})$ / 2 to GND	–2		VDD	V
V_{CM}	Operating common-mode input voltage (2)	$(V_{AINP} + V_{AINN})$ / 2 to GND, 3.0 V ≤ VDD < 4 V, $V_{AINP} = V_{AINN}$	–1.4		VDD – 1.4	V
		$(V_{AINP} + V_{AINN})$ / 2 to GND, 3.0 V ≤ VDD < 4.5 V, $\lvert V_{AINP} – V_{AINN}\rvert$ = 1.25 V	–0.8		VDD – 2.4	
		$(V_{AINP} + V_{AINN})$ / 2 to GND, 4 V ≤ VDD ≤ 5.5 V, $V_{AINP} = V_{AINN}$	–1.4		2.7	
		$(V_{AINP} + V_{AINN})$ / 2 to GND, 4.5 V ≤ VDD ≤ 5.5 V, $\lvert V_{AINP} – V_{AINN}\rvert$ = 1.25 V	–0.8		2.1	
DIGITAL INPUT						
	Input voltage	V_{MCE} or V_{CLKIN} to GND	GND		VDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40	25	125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.
(2) See the *Analog Input* section for more details.

6.4 Thermal Information

THERMAL METRIC[1]		AMC1035	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, AINP = –1 V to 1 V, AINN = GND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, and VDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{CMuv} (1)	Negative common-mode undervoltage detection level (2)	$(V_{AINP} + V_{AINN}) / 2$, $V_{AINP} = V_{AINN}$			–1.45	V
		$(V_{AINP} + V_{AINN}) / 2$, $\lvert V_{AINP} – V_{AINN}\rvert$ = 1.25 V			–0.85	
V_{CMov} (1)	Positive common-mode overvoltage detection level (2)	3.0 V ≤ VDD < 4 V, $V_{AINP} = V_{AINN}$			VDD – 1.35	V
		3.0 V ≤ VDD < 4.5 V, $\lvert V_{AINP} – V_{AINN}\rvert$ = 1.25 V			VDD – 2.35	
		4 V ≤ VDD ≤ 5.5 V, $V_{AINP} = V_{AINN}$	2.75			
		4.5 V ≤ VDD ≤ 5.5 V, $\lvert V_{AINP} – V_{AINN}\rvert$ = 1.25 V	2.15			
R_{IN}	Single-ended input resistance	AINN = GND	0.1	0.4		GΩ
R_{IND}	Differential input resistance		0.16	1.6		GΩ
C_{IN}	Single-ended input capacitance	AINN = GND		2		pF
C_{IND}	Differential input capacitance			2		pF
I_{IB}	Input bias current	AINP = AINN = GND, $(I_{AINP} + I_{AINN}) / 2$	–10	±3	10	nA
TCI_{IB}	Input bias current thermal drift	AINP = AINN = GND, $(I_{AINP} + I_{AINN}) / 2$		±5		pA/°C
I_{IO}	Input offset current	$I_{IO} = I_{AINP} – I_{AINN}$	–5	±1	5	nA
CMRR	Common-mode rejection ratio	AINP = AINN, f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–104		dB
		AINP = AINN, f_{IN} from 0.1 Hz to 50 kHz, –0.5 V ≤ V_{IN} ≤ 0.5 V		–88		
DC ACCURACY						
	Resolution (3)		16			Bits
INL	Integral nonlinearity (4)	Resolution: 16 bits	–12	±2	12	LSB
E_O	Offset error	Initial, at T_A = 25°C, AINP = AINN = GND	–0.5	±0.03	0.5	mV
TCE_O	Offset error thermal drift (5)		–6	±0.1	6	µV/°C
E_G	Gain error	Initial, at T_A = 25°C	–0.25%	±0.02%	0.25%	
		Initial, at T_A = 25°C, ratiometric mode	–0.3%	±0.02%	0.3%	
TCE_G	Gain error thermal drift (6)		–45	±20	45	ppm/°C
		Ratiometric mode	–15	±4	15	
PSRR	Power-supply rejection ratio	AINP = AINN = GND, at dc		–90		dB
		AINP = AINN = GND, 10 kHz, 100-mV ripple		–84		

(1) See the *Analog Input* section for more details.
(2) The common-mode overvoltage detection level has a typical hysteresis of 35 mV.
(3) The filter output is truncated to 16 bits. 16 bits of no missing codes is specified by design.
(4) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(5) Offset error drift is calculated using the box method, as described by the following equation: $TCE_O = \dfrac{value_{MAX} - value_{MIN}}{TempRange}$.
(6) Gain error drift is calculated using the box method, as described by the following equation: $TCE_G(ppm) = \left(\dfrac{value_{MAX} - value_{MIN}}{value \times TempRange}\right) \times 10^6$.

Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, AINP = –1 V to 1 V, AINN = GND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, and VDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	81	87		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	77	83		dB
THD	Total harmonic distortion	f_{IN} = 1 kHz		–87	–78	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	78	87		dB
REFERENCE OUTPUT						
V_{REFOUT}	Reference output voltage	Initial, at T_A = 25°C, no load	2.495	2.5	2.505	V
TCV_{REFOUT}	Reference output voltage drift		–50	±20	50	ppm/°C
I_{REFOUT}	Reference output current	C_{LOAD} < 1 nF[7]	–5		5	mA
	Load regulation	Load to GND or VDD		0.15	0.35	mV/mA
I_{SC}	Short-circuit current	REFOUT to GND		23		mA
		REFOUT to VDD		–21		
PSRR	Power-supply rejection ratio		–200	±30	200	µV/V
DIGITAL INPUTS (CMOS Logic With Schmitt-Trigger)						
I_{IN}	Input current	GND ≤ V_{IN} ≤ VDD			35	µA
C_{IN}	Input capacitance			3		pF
V_{IH}	High-level input voltage		0.7 × VDD		VDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × VDD	V
DIGITAL OUTPUT: CMOS						
C_{LOAD}	Output load capacitance	f_{CLKIN} = 21 MHz		15	30	pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	VDD – 0.1			V
		I_{OH} = –4 mA	VDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
POWER SUPPLY						
I_{VDD}	High-side supply current	3.0 V ≤ VDD ≤ 3.6 V, I_{REFOUT} = 0 mA, MCE = 0, C_{LOAD} = 15 pF		5.2	6.8	mA
		3.0 V ≤ VDD ≤ 3.6 V, I_{REFOUT} = 0 mA, MCE = 1, C_{LOAD} = 15 pF[8]		4.6	6.1	
		4.5 V ≤ VDD ≤ 5.5 V, I_{REFOUT} = 0 mA, MCE = 0, C_{LOAD} = 15 pF		6.4	8.3	
		4.5 V ≤ VDD ≤ 5.5 V, I_{REFOUT} = 0 mA, MCE = 1, C_{LOAD} = 15 pF[8]		5.4	7.2	

(7) Capacitive load with a value ≥ 1nF requires series resistor to be connected to the REFOUT pin. See the *Reference Output* section for more details.

(8) Typical value is specified at f_{CLKIN} = 10 MHz, maximum value is specified at f_{CLKIN} = 11 MHz.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLKIN}	CLKIN clock frequency	MCE = 0	9	20	21	MHz
		MCE = 1	9	10	11	
$Duty_{Cycle}$	CLKIN clock duty cycle[1]		40%	50%	60%	
t_{H1}	DOUT hold time after rising edge of CLKIN	MCE = 0, C_{LOAD} = 15 pF	6			ns
t_{H2}	DOUT hold time after rising edge of CLKIN	MCE = 1, C_{LOAD} = 15 pF	6		23	ns
t_{H3}	DOUT hold time after falling edge of CLKIN	MCE = 1, C_{LOAD} = 15 pF	10		26	ns
t_{D1}	Rising edge of CLKIN to DOUT valid delay	MCE = 0, C_{LOAD} = 15 pF			25	ns
t_{D2}	Rising edge of CLKIN to DOUT valid delay	MCE = 1, C_{LOAD} = 15 pF	11		27	ns
t_{D3}	Falling edge of CLKIN to DOUT valid delay	MCE = 1, C_{LOAD} = 15 pF	15		30	ns
t_r	DOUT rise time	10% to 90%, 3.0 V ≤ VDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.5	5	ns
		10% to 90%, 4.5 V ≤ VDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.5	3.5	
t_f	DOUT fall time	90% to 10%, 3.0 V ≤ VDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.5	5.8	ns
		90% to 10%, 4.5 V ≤ VDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.8	4.4	
t_{ASTART}	Analog startup time	VDD step to 3.0 V, 0.1% settling, CLKIN applied		0.25		ms

---

[1] The duty cycle of DOUT equals the clock duty cycle of the applied CLKIN signal.

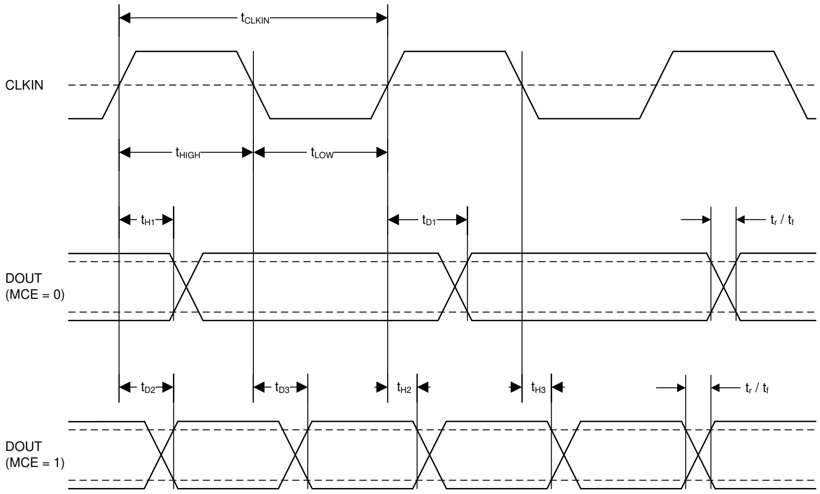


Figure 1. Digital Interface Timing

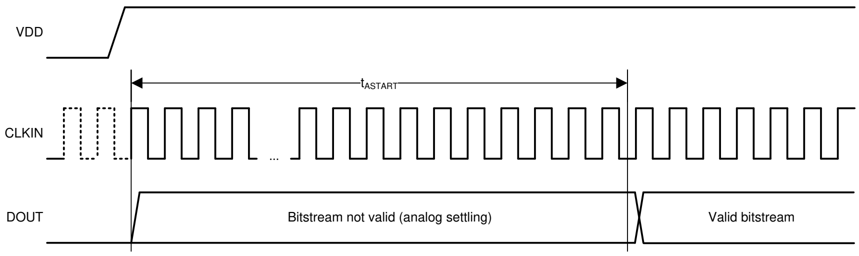
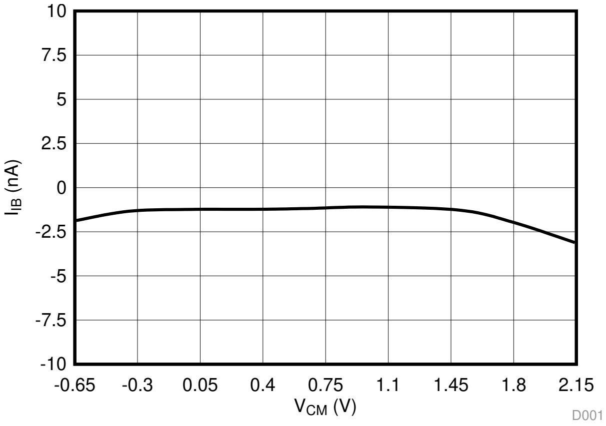


Figure 2. Device Startup Timing

6.7 Typical Characteristics

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)



VDD = 5.5 V

Figure 3. Input Bias Current vs Common-Mode Input Voltage

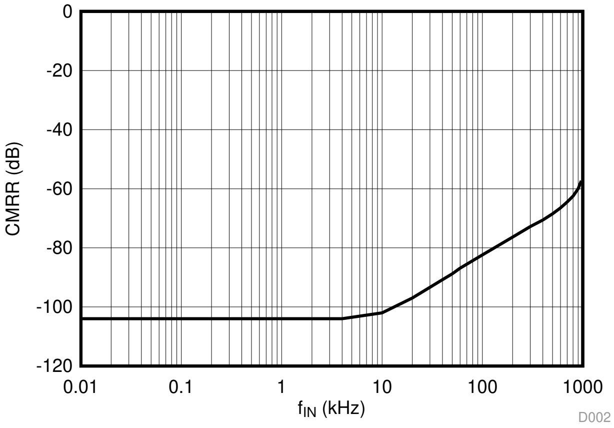


Figure 4. Common-Mode Rejection Ratio vs Input Signal Frequency

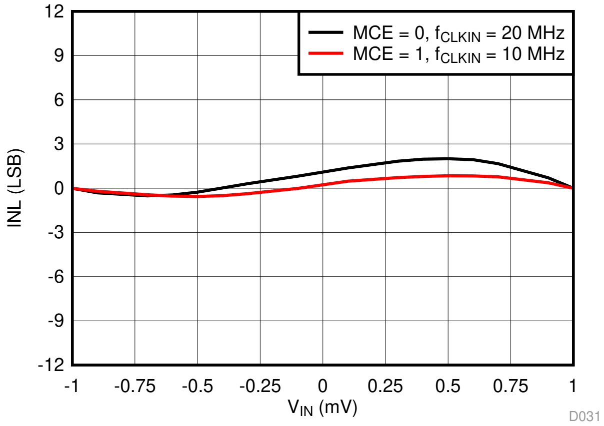


Figure 5. Integral Nonlinearity vs Input Voltage

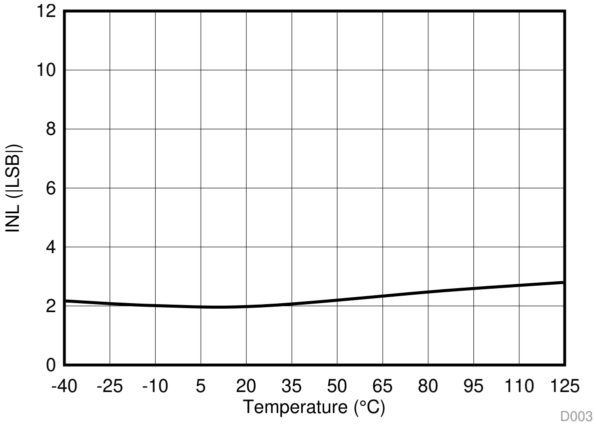


Figure 6. Integral Nonlinearity vs Temperature

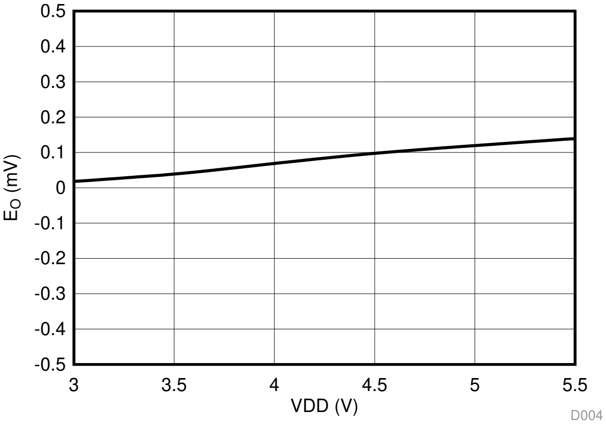


Figure 7. Offset Error vs Supply Voltage

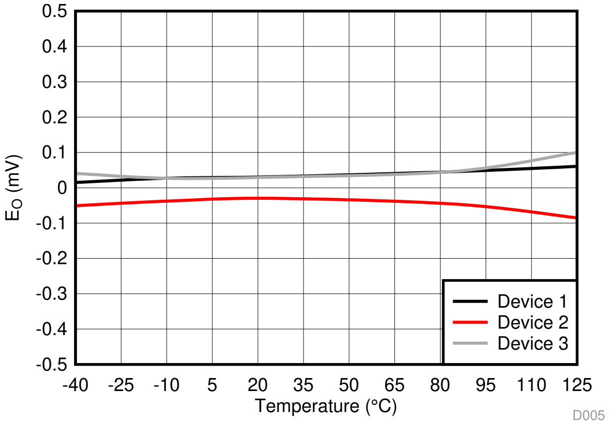


Figure 8. Offset Error vs Temperature

Typical Characteristics (continued)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

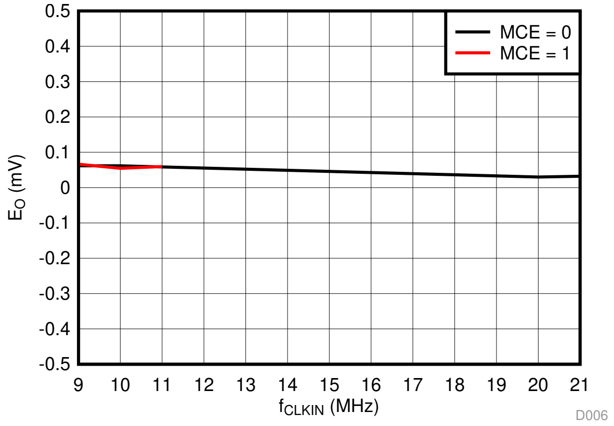


Figure 9. Offset Error vs Clock Frequency

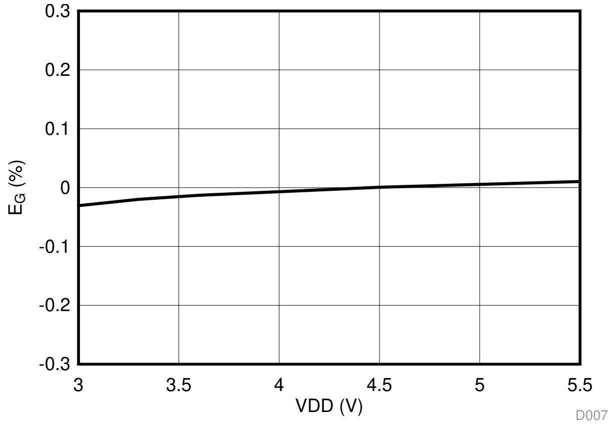


Figure 10. Gain Error vs Supply Voltage

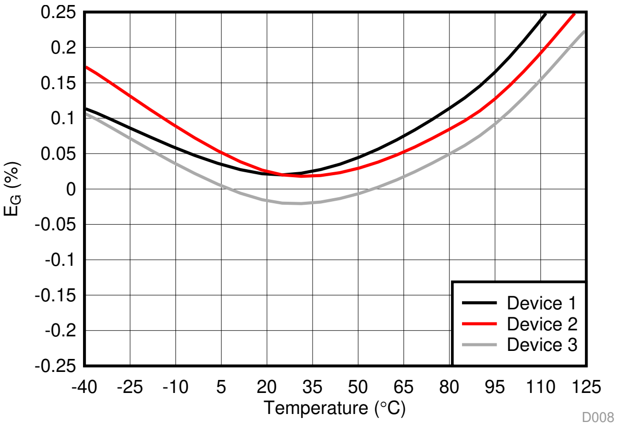


Figure 11. Gain Error vs Temperature

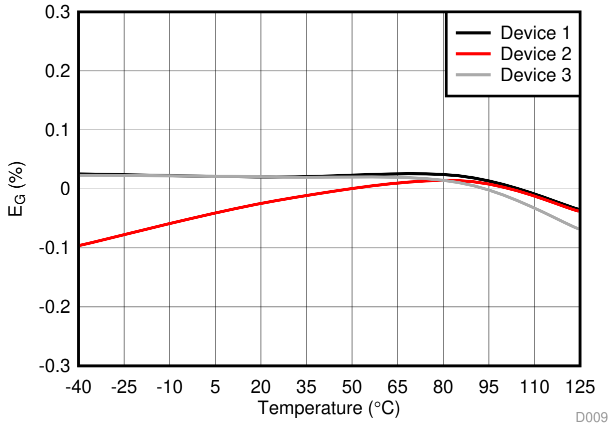


Figure 12. Ratiometric Gain Error vs Temperature

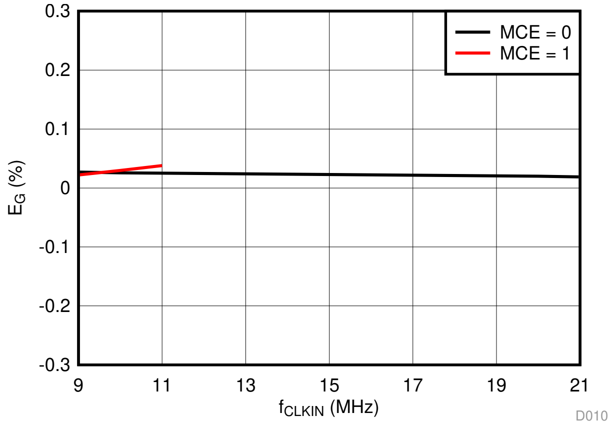


Figure 13. Gain Error vs Clock Frequency

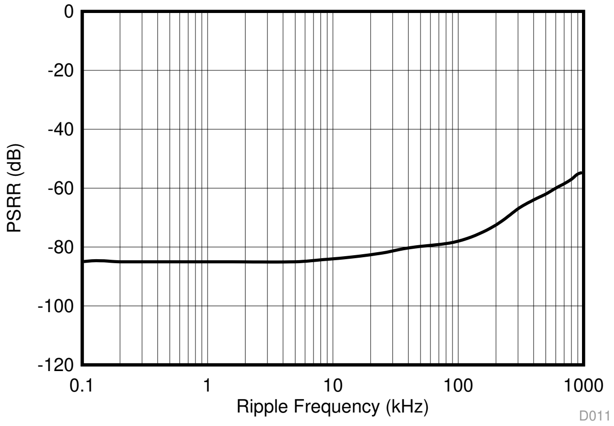


Figure 14. Power-Supply Rejection Ratio vs Ripple Frequency

Typical Characteristics (continued)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

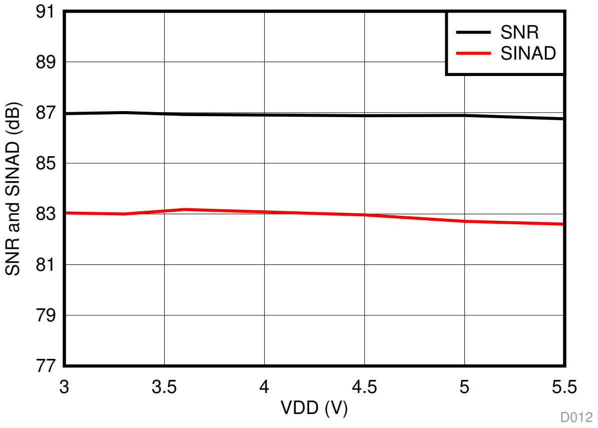


Figure 15. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Supply Voltage

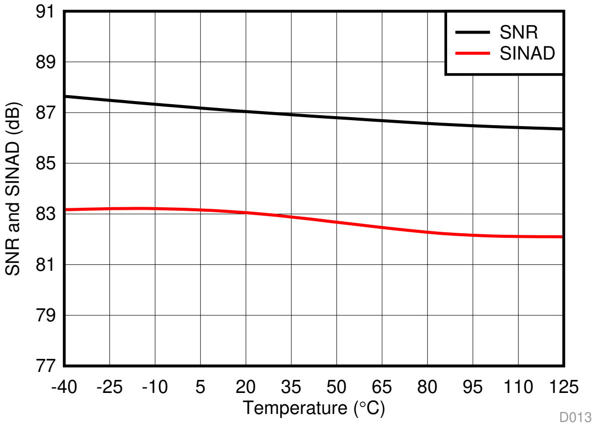


Figure 16. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

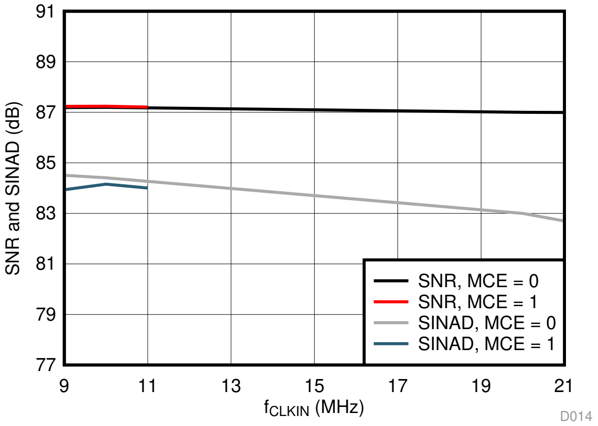


Figure 17. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency

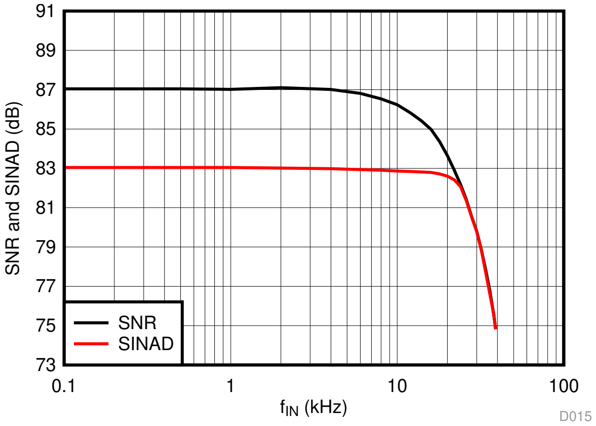


Figure 18. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

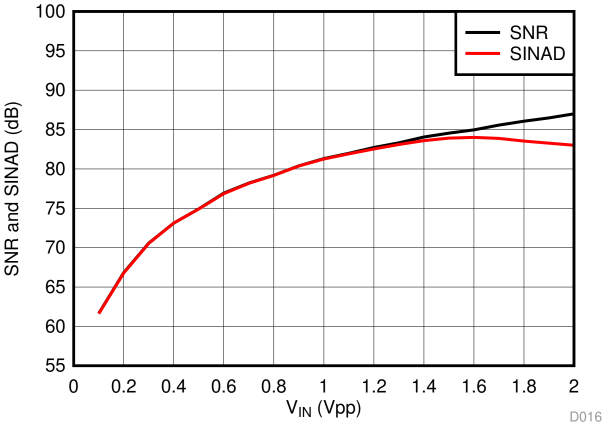


Figure 19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

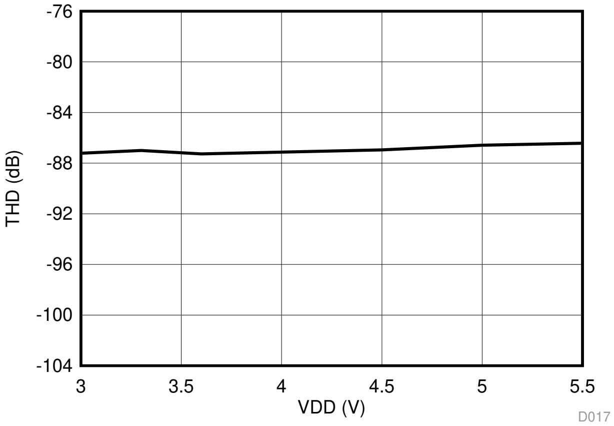


Figure 20. Total Harmonic Distortion vs Supply Voltage

Typical Characteristics (continued)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

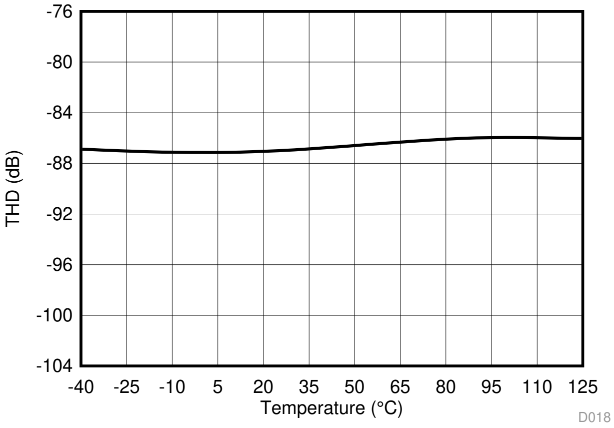


Figure 21. Total Harmonic Distortion vs Temperature

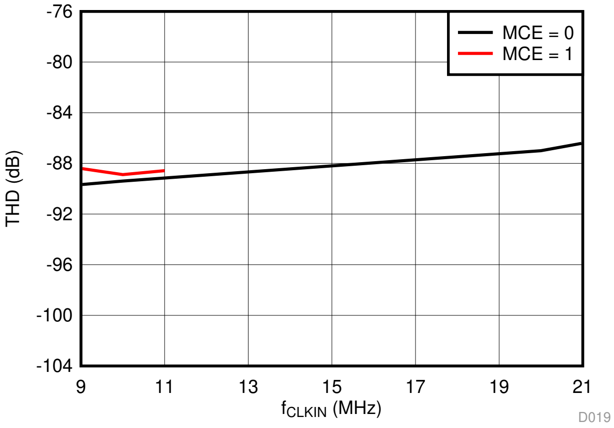


Figure 22. Total Harmonic Distortion vs Clock Frequency

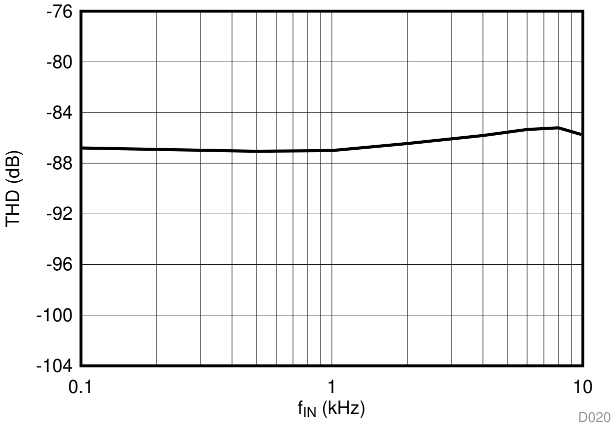


Figure 23. Total Harmonic Distortion vs Input Signal Frequency

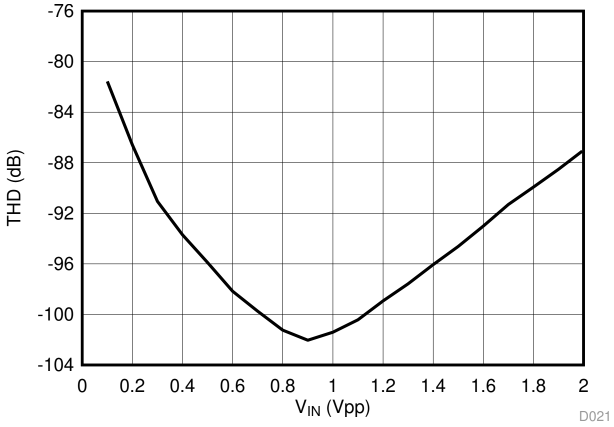


Figure 24. Total Harmonic Distortion vs Input Signal Amplitude

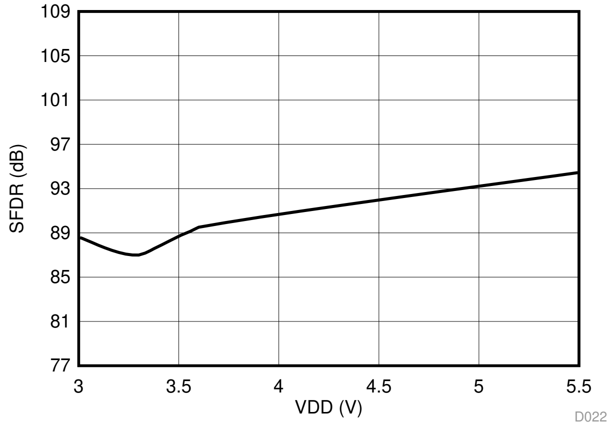


Figure 25. Spurious-Free Dynamic Range vs Supply Voltage

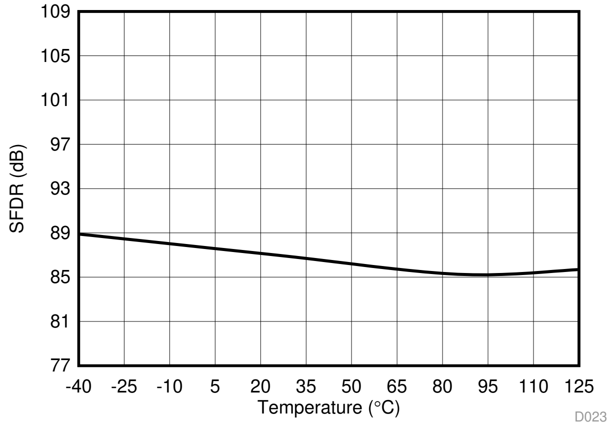


Figure 26. Spurious-Free Dynamic Range vs Temperature

Typical Characteristics (continued)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

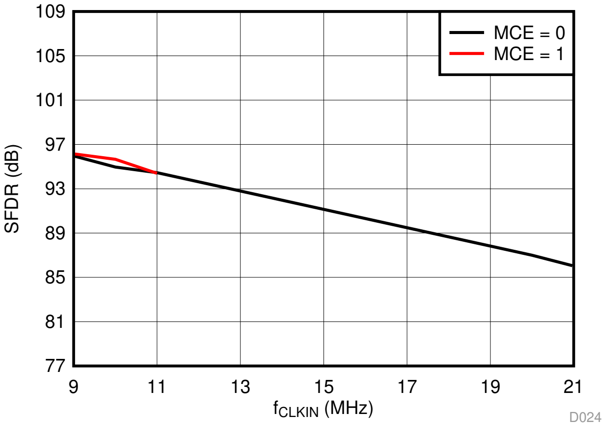


Figure 27. Spurious-Free Dynamic Range vs Clock Frequency

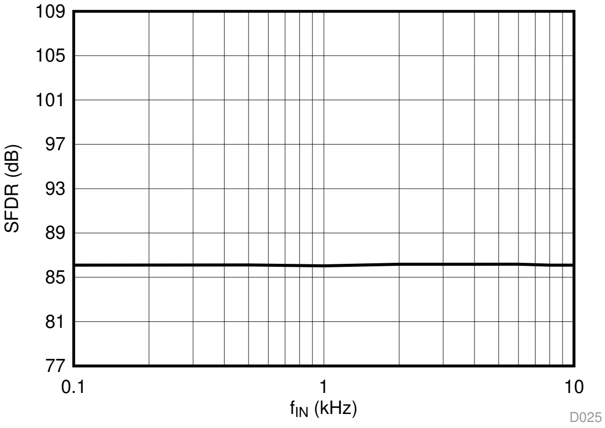


Figure 28. Spurious-Free Dynamic Range vs Input Signal Frequency

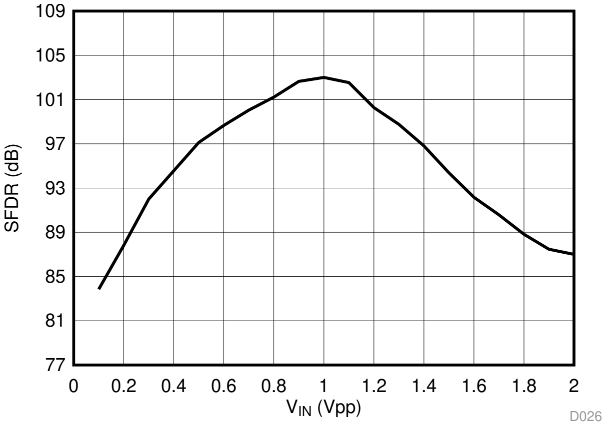
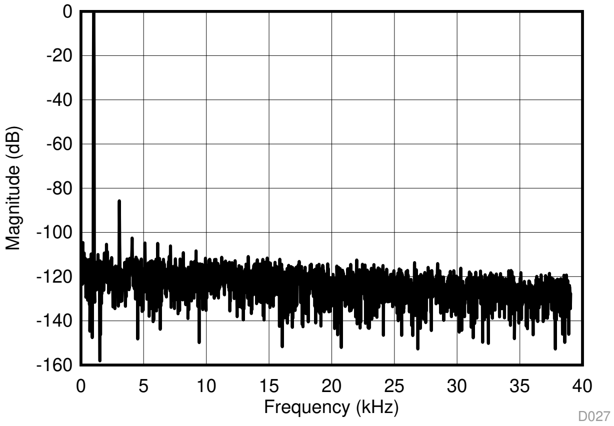
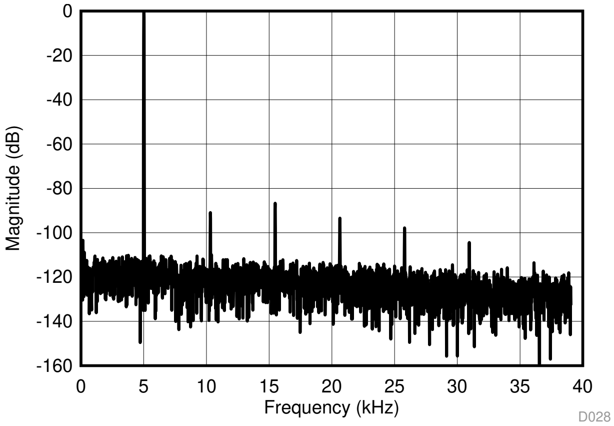


Figure 29. Spurious-Free Dynamic Range vs Input Signal Amplitude



4096-point FFT, V_{IN} = 2 V_{PP}

Figure 30. Frequency Spectrum With 1-kHz Input Signal



4096-point FFT, V_{IN} = 2 V_{PP}

Figure 31. Frequency Spectrum With 5-kHz Input Signal

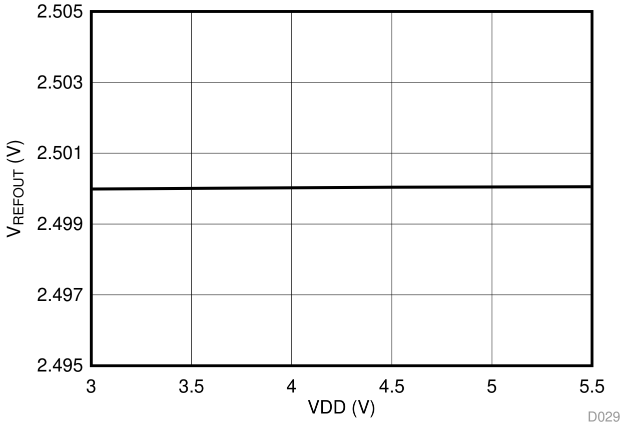


Figure 32. Reference Output Voltage vs Supply Voltage

Typical Characteristics (continued)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

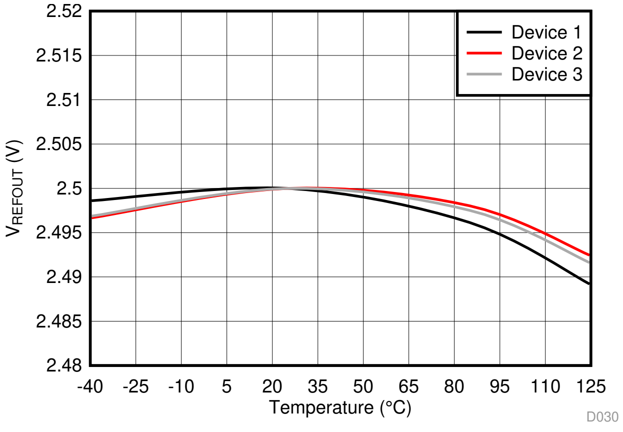


Figure 33. Reference Output Voltage vs Temperature

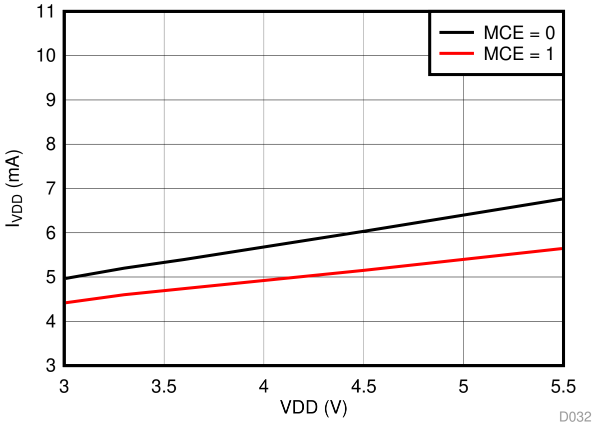


Figure 34. Supply Current vs Supply Voltage

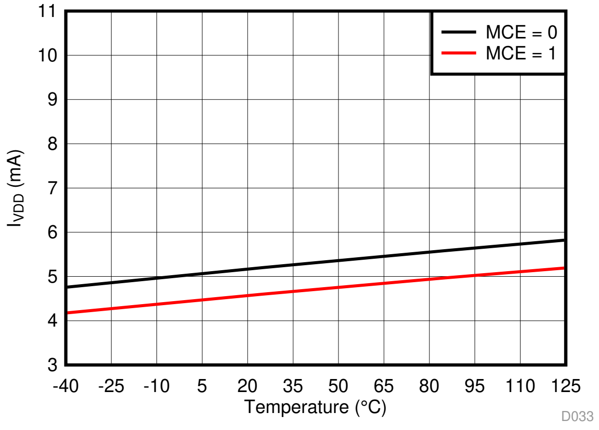


Figure 35. Supply Current vs Temperature

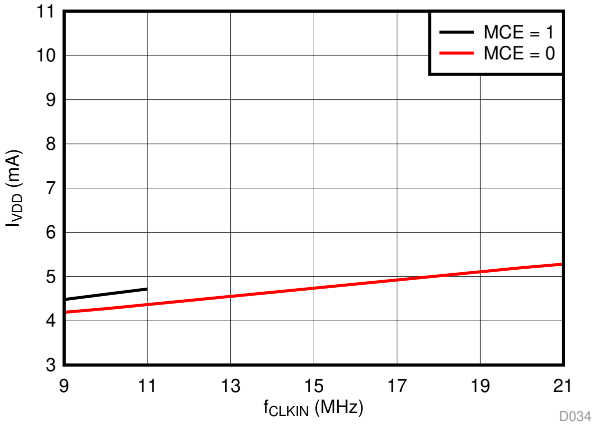


Figure 36. Supply Current vs Clock Frequency

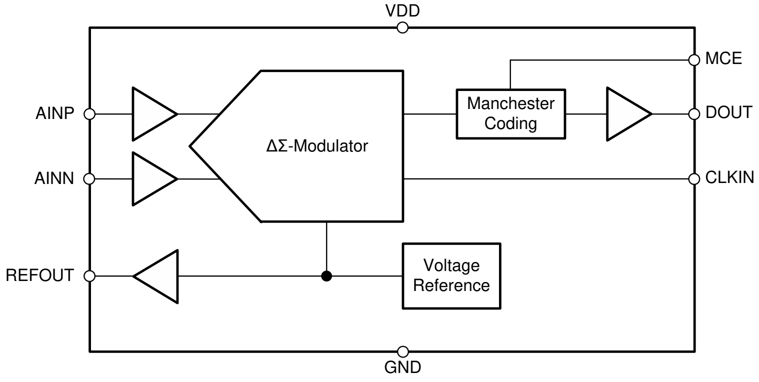
7 Detailed Description

7.1 Overview

The differential analog input (comprised of input signals AINP and AINN) of the AMC1035 is a chopper-stabilized buffer, followed by the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator stage that digitizes the input signal into a 1-bit output stream. The data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the externally-provided clock source at the CLKIN pin with a frequency in the range of 9 MHz to 21 MHz. The time average of this serial bitstream output is proportional to the analog input voltage.

The *Functional Block Diagram* section shows a detailed block diagram of the AMC1035. The 1.6-GΩ differential input resistance of the analog input stage supports low gain-error signal sensing in high-voltage applications using resistive dividers. The external clock input simplifies the synchronization of multiple measurement channels on the system level. The extended frequency range of up to 21 MHz supports higher performance levels compared to the other solutions available on the market.

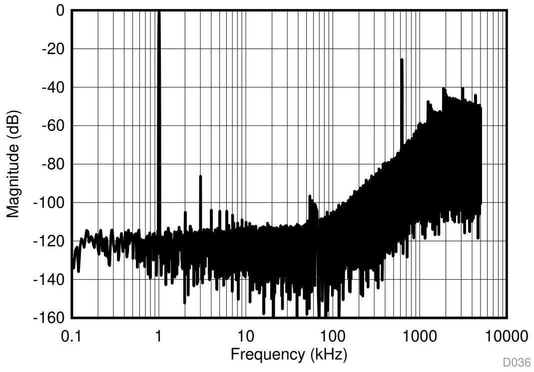
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The AMC1035 incorporates front-end circuitry that contains a buffered sampling stage, followed by a ΔΣ modulator. To support a bipolar input range, the device uses a charge pump that allows single-supply operation to simplify the overall system design and minimize the circuit cost. For reduced offset and offset drift, the input buffer is chopper-stabilized with the switching frequency set at f_{CLKIN} / 32. Figure 37 shows the spur created by the switching frequency.



sinc^3 filter, OSR = 2, f_{CLKIN} = 20 MHz, f_{IN} = 1 kHz

Figure 37. Quantization Noise Shaping

Feature Description (continued)

The linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is ±1 V, and within the specified input common-mode range.

Figure 38 shows the specified common-mode input voltage that applies for the full-scale input voltage range as specified in this document along with the corresponding common-mode undervoltage and overvoltage threshold levels.

If smaller input signals are used, the operational common-mode input voltage range widens. Figure 39 shows the common-mode input voltage that applies with no differential input signal; that is, when the voltage applied on AINP is equal to the voltage applied on AINN. The common-mode input voltage range scales with the actual differential input voltage between this range and the range in Figure 38.

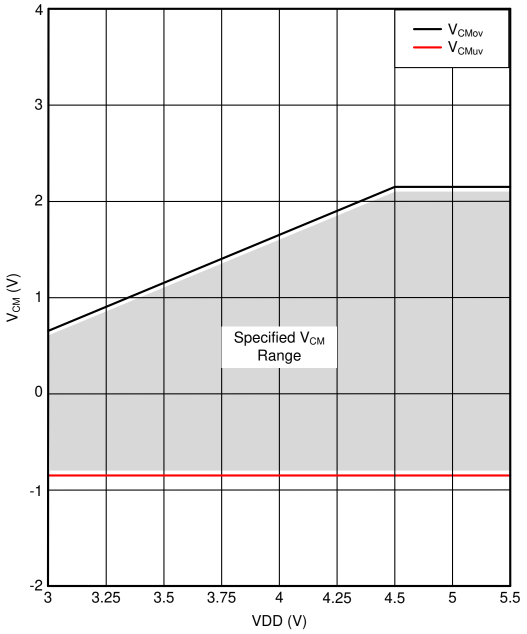


Figure 38. Common-Mode Input Voltage Range With a Full-Scale Differential Input Signal of ±1.25 V

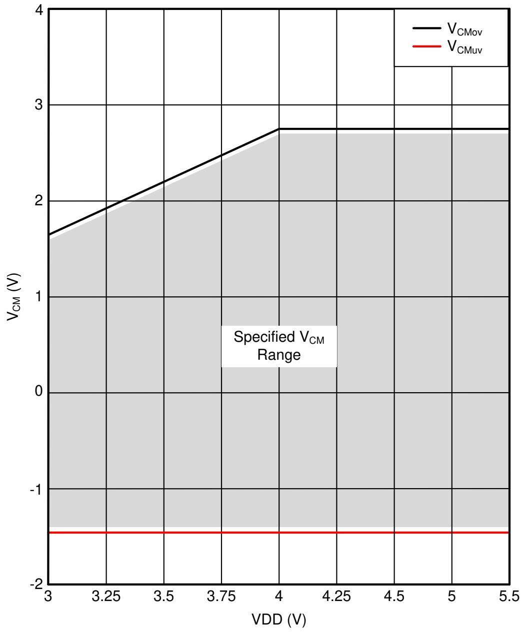


Figure 39. Common-Mode Input Voltage Range With a Zero Differential Input Signal

Feature Description (continued)

7.3.2 Modulator

The modulator implemented in the AMC1035 (such as the one conceptualized in Figure 40) is a second-order, switched-capacitor, feed-forward ΔΣ modulator. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are subtracted, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is summed with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

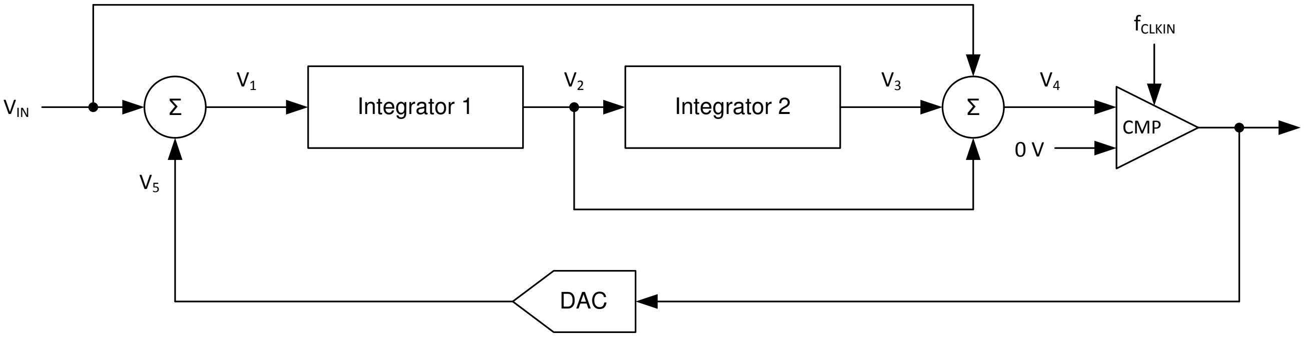


Figure 40. Block Diagram of a Second-Order Modulator

As depicted in Figure 37, the modulator shifts the quantization noise to high frequencies. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller families TMS320F28004x, TMS320F2807x, and TMS320F2837x offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1035. Also, SD24_B converters on the MSP430F677x microcontrollers offer a path to directly access the integrated sinc-filters for a simple system-level solution for multichannel, isolated current sensing. An additional option is to use a suitable application-specific device, such as the AMC1210 (a four-channel digital sinc filter). Alternatively, a field-programmable gate array (FPGA) can be used to implement the filter.

7.3.3 Reference Output

The AMC1035 offers a voltage reference output that can source or sink current to significantly reduce the gain error thermal drift in ratiometric applications as specified in the *Electrical Characteristics* table. The *IGBT Temperature Sensing* section provides an example of a ratiometric use case for the AMC1035.

The reference output can drive capacitive loads less than 1 nF. Use a series resistor to avoid oscillations and degradation of performance for capacitive loads ≥ 1 nF. Table 1 lists the recommended series resistor values for given capacitor value examples. Interpolate for capacitive loads with a value between the given examples.

Table 1. Series Resistor Value for Capacitive Loads ≥ 1 nF on REFOUT Pin

CAPACITIVE LOAD ON REFOUT PIN	1 nF	3.3 nF	10 nF	33 nF	100 nF	330 nF	1 µF	3.3 µF	10 µF
Recommended series resistor	33 Ω	56 Ω	47 Ω	33 Ω	15 Ω	10 Ω	5.6 Ω	3.3 Ω	1.8 Ω

7.3.4 Clock Input

The AMC1035 system clock is provided externally at the CLKIN pin. The clock signal must be applied continuously for proper device operation.

To support the bipolar input voltage range with a single supply, the AMC1035 includes a charge pump. This charge pump stops operating if the clock signal is below the specified frequency range or if the signal is paused or missing. Additionally, the input bias current increases beyond the specified range and significantly reduces the input resistance of the device. When the clock signal is paused or missing, the modulator stops the analog signal conversion and the digital output signal remains frozen in the last logic state. When the clock signal is applied again after a pause, the internal analog circuitry biasing must settle for proper device performance. In this case, consider the t_{ASTART} specification in the *Switching Characteristics* table.

7.3.5 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 1 V produces a stream of ones and zeros that are high 90% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58982 (an unsigned code). A differential input of –1 V produces a stream of ones and zeros that are high 10% of the time and ideally results in code 6553 with 16-bit resolution. These input voltages are also the specified linear range of the AMC1035 with performance as specified in this document. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior when the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to –1.25 V or with a stream of only ones with an input greater than or equal to 1.25 V. In this case, however, the AMC1035 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the *Fail-Safe Output* section for more details). Figure 41 shows the input voltage versus the output modulator signal.

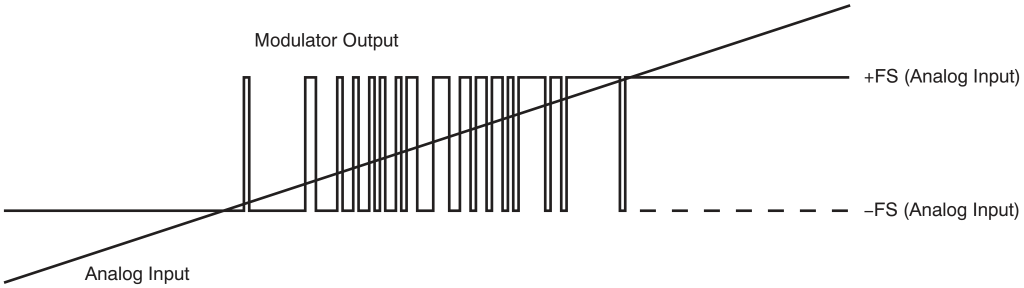


Figure 41. Analog Input versus the AMC1035 Modulator Output

Equation 1 calculates the density of ones in the output bitstream for any input voltage value (with the exception of a full-scale input signal, as described in the *Output Behavior in Case of a Full-Scale Input* section):

$$\frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

The modulator bitstream on the DOUT pin changes with the rising edge of the clock signal applied on the CLKIN pin. Use the rising edge of the clock to latch the modulator bitstream at the input of the digital filter device.

7.3.6 Manchester Coding Feature

The AMC1035 offers the IEEE 802.3-compliant Manchester coding feature that generates at least one transition per bit to support clock signal recovery from the bitstream. The Manchester coding combines the clock and data information using exclusive-OR (XOR) logical operation that results in a bitstream free of DC components. Figure 42 shows the resulting bitstream from this coding. The duty cycle of the Manchester encoded bitstream depends on the duty cycle of the input clock CLKIN. To enable Manchester coding on the AMC1035, pull the input pin MCE high. The DOUT signal is inverted if the MCE status changes when CLKIN is high.

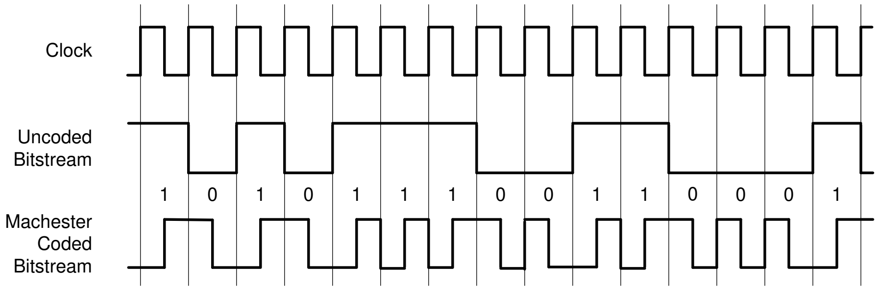


Figure 42. Manchester Coded Output of the AMC1035

7.4 Device Functional Modes

The AMC1035 is operational when the power supply VDD and clock signal CLKIN are applied, as specified in Figure 39 and the *Switching Characteristics* table.

7.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1035 (that is, $|V_{IN}| \geq |V_{Clipping}|$), the device generates a single one or zero every 128 bits at DOUT, as shown in Figure 43, depending on the actual polarity of the signal being sensed. This feature is also supported with Manchester-coded output and allows full-scale and invalid input signals to be identified as described in the *Fail-Safe Output* section and can be used for advanced system-level diagnostics.

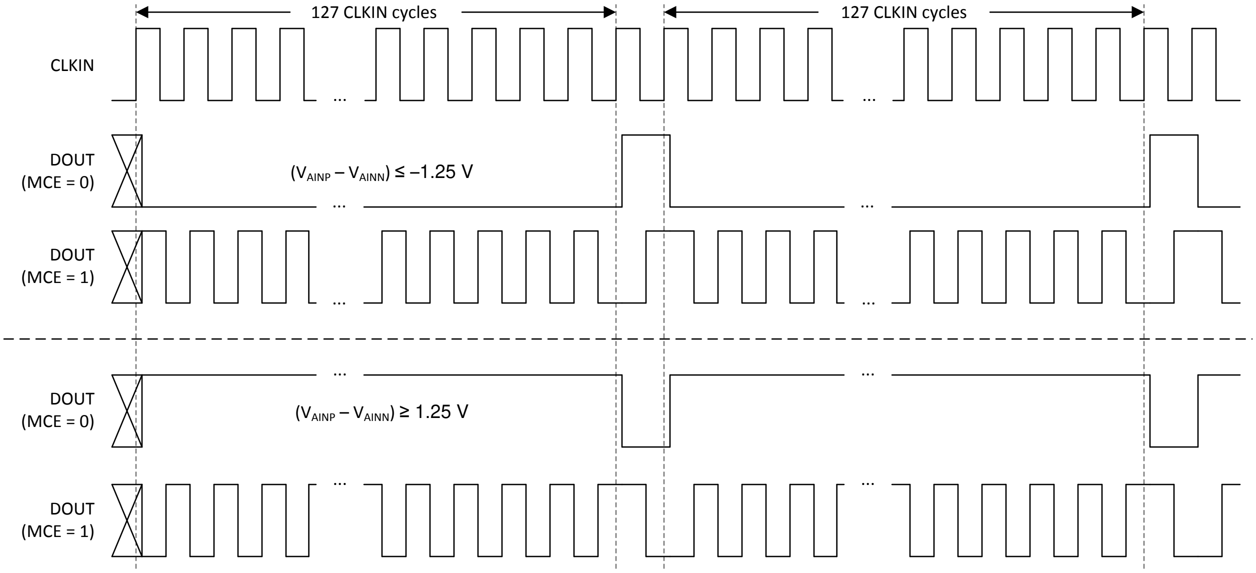


Figure 43. Overrange Output of the AMC1035

Device Functional Modes (continued)

7.4.2 Fail-Safe Output

Figure 44 shows that if the common-mode voltage of the input reaches or exceeds the specified common-mode undervoltage, V_{CMuv}, or overvoltage detection level, V_{CMov} as defined in the *Electrical Characteristics* table, the DOUT of the AMC1035 is held at steady-state high.

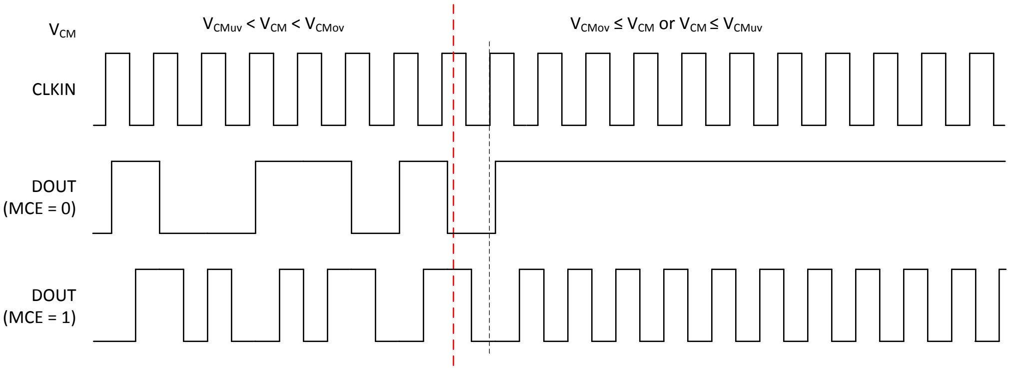


Figure 44. Fail-Safe Output of the AMC1035

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Digital Filter Usage

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). Equation 2 shows a sinc^3-type filter, which is a very simple filter, built with minimal effort and hardware:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \tag{2}$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is also done with a sinc^3 filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

An example code for implementing a sinc^3 filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

8.2 Typical Applications

8.2.1 Voltage Sensing

ΔΣ modulators are widely used in frequency inverter designs because of their high AC and DC performance. Frequency inverters are critical parts of industrial motor drives, photovoltaic inverters (string and central inverters), uninterruptible power supplies (UPS), and other industrial applications.

Figure 45 shows a simplified schematic of a motor drive application with the AMC1035 used for the DC-link and output phase voltage sensing. In this example, all resistive dividers reference to the negative DC-link voltage that is also used as a ground reference point for the microcontroller. An additional fifth AMC1035 can be used for temperature sensing of the insulated-gate bipolar transistor (IGBT) module; see the *IGBT Temperature Sensing* section for more details.

Current feedback is performed with shunt resistors (R_{SHUNT}) and TI's AMC1306M25 isolated modulators. Depending on the system design, either all three or only two motor phase currents are sensed.

Depending on the overall digital processing power requirements and with a total of eight ΔΣ modulator bitstreams to be processed by the MCU, a derivate from either the low-cost single-core TMS320F2807x or the dual-core TMS320F2837x families can be used in this application.

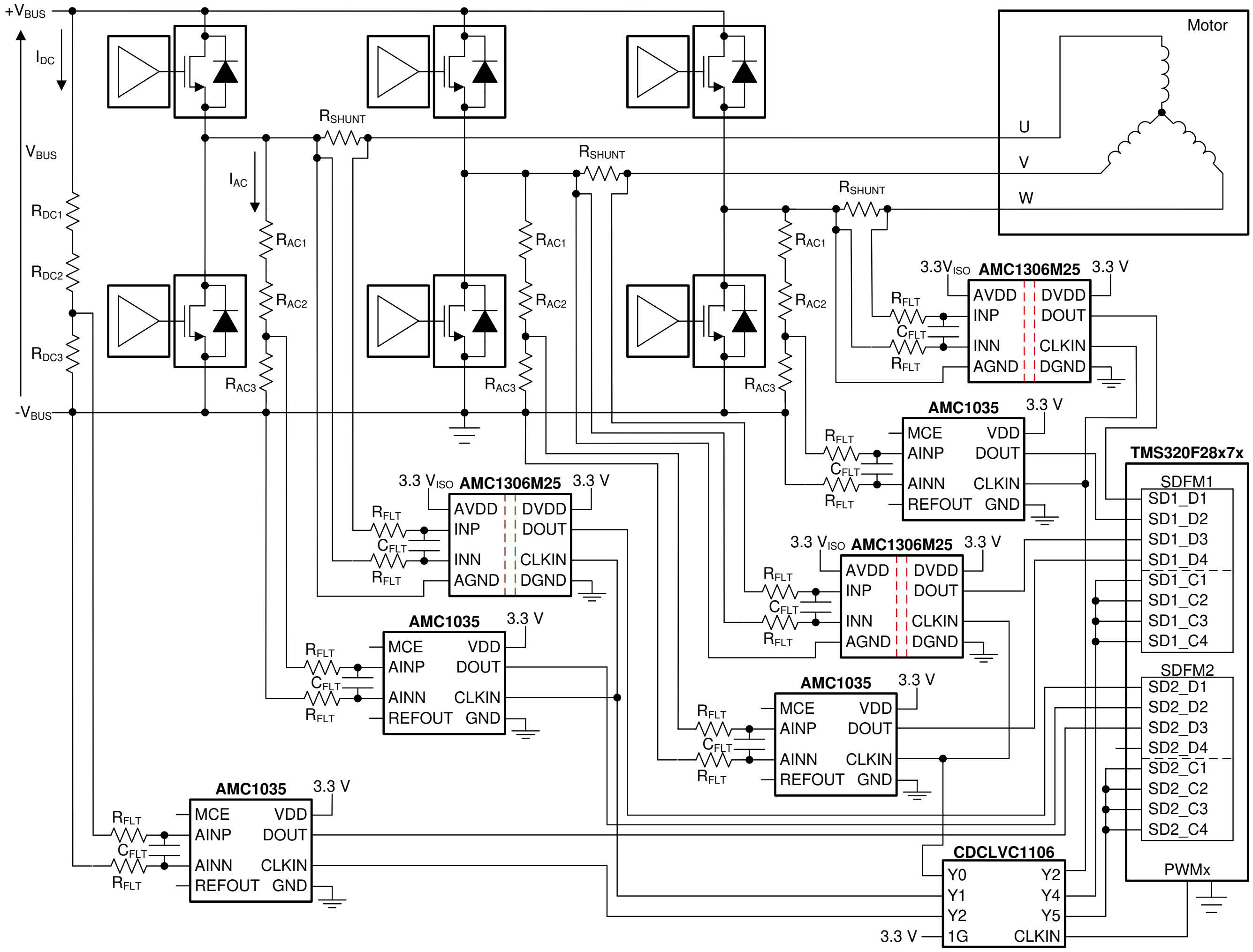


Figure 45. The AMC1035 in a Frequency Inverter Application

Typical Applications (continued)

8.2.1.1 Design Requirements

Table 2 lists the parameters for this typical application.

Table 2. Design Requirements

PARAMETER	VALUE
Supply voltage	3.3 V
Voltage drop across the sensing resistor R_{DC1} for a linear response	1 V (maximum)
Voltage drop across the sensing resistors R_{ACx} for a linear response	±1 V (maximum)
Current through the sensing resistors R_{ACx}	±100 µV (maximum)

8.2.1.2 Detailed Design Procedure

Use Ohm's Law to calculate the minimum total resistance of the resistive dividers to limit the cross current to the desired values:

- For the voltage sensing on the DC bus: $R_{DC1} + R_{DC2} + R_{DC3} = V_{BUS} / I_{DC}$
- For the voltage sensing on the output phases U, V, and W: $R_{AC1} + R_{AC2} + R_{AC3} = V_{PHASE\ (max)} / I_{AC}$

Consider the following two restrictions to choose the proper value of the resistors R_{DC3} and R_{AC3}:

- The voltage drop caused by the nominal voltage range of the system must not exceed the recommended input voltage range of the AMC1035: $V_{xC3} \le V_{FSR}$
- The voltage drop caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output: $V_{xC3} \le V_{Clipping}$

Use similar approach for calculation of the shunt resistor values R_{SHUNT} and see the AMC1306M25 data sheet for further details.

Table 3 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 600 V and 800 V on the DC bus.

Table 3. Resistor Value Examples for DC Bus Sensing

PARAMETER	600-V DC BUS	800-V DC Bus
Resistive divider resistor R_{DC1}	3.01 MΩ	4.22 MΩ
Resistive divider resistor R_{DC2}	3.01 MΩ	4.22 MΩ
Sense resistor R_{DC3}	10 kΩ	10.5 kΩ
Resulting current through resistive divider I_{DC}	99.5 µA	94.7 µA
Resulting voltage drop on sense resistor V_{RDC3}	0.995 V	0.994 V

Table 4 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 230 V and 690 V on the output phases.

Table 4. Resistor Value Examples for Output Phase Voltage Sensing

PARAMETER	±400-V_{AC} PHASE	±690-V_{AC} PHASE
Resistive divider resistor R_{AC1}	2.0 MΩ	3.48 MΩ
Resistive divider resistor R_{AC2}	2.0 MΩ	3.48 MΩ
Sense resistor R_{AC3}	10.0 kΩ	10.0 kΩ
Resulting current through resistive divider I_{AC}	99.8 µA	99.0 µA
Resulting voltage drop on sense resistor V_{RAC3}	±0.998 V	±0.990 V

Use a power supply with a nominal voltage of 3.3 V to directly connect all modulators to the microcontroller.

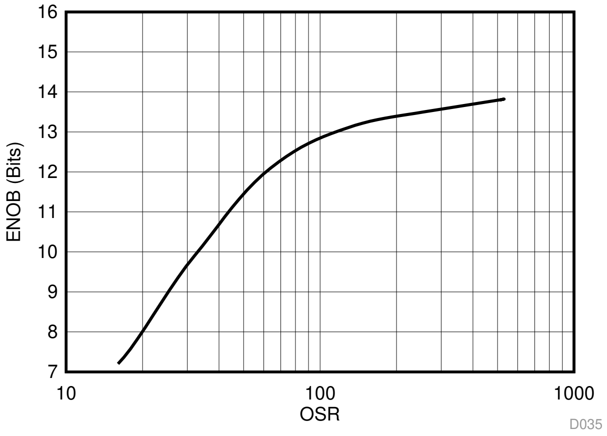
For modulator output bitstream filtering, a device from TI's TMS320F2807x family of low-cost microcontrollers (MCUs) or TMS320F2837x family of dual-core MCUs is recommended. These MCU families support up to eight channels of dedicated hardwired filter structures called sigma-delta filter modules (SDFMs) that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one that offers a fast response path for overcurrent detection. Use one of the pulse-width modulation (PWM) sources inside the MCU to generate the clock for the modulators and for easy synchronization of all feedback signals and the switching control of the gate drivers.

Figure 45 uses a clock buffer to distribute the clock reference signal generated on one of the PWM outputs of the MCU (called PWMx in Figure 45) to all modulators used in the circuit and as a reference for the digital filters in the MCU. In this example, TI's CDCLVC1106 is used for this purpose. Each CDCLVC1106 output can drive a load of 8 pF that is sufficient to drive up to two modulator and up to four SDFM clock inputs.

8.2.1.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 46 shows the ENOB of the AMC1035 with different oversampling ratios on a sinc3 filter. This number is calculated from the SINAD by using Equation 3 in this document.

$$\text{SINAD} = 1.76\text{ dB} + 6.02\text{ dB} \times \text{ENOB} \quad (3)$$



Sinc3 filter

Figure 46. Measured Effective Number of Bits vs Oversampling Ratio

8.2.2 IGBT Temperature Sensing

The high input impedance of the AMC1035 is optimized for usage in voltage-sensing applications. Additionally, the internal voltage reference supports temperature sensing using a positive temperature coefficient (PTC) or a negative temperature coefficient (NTC) sensor often integrated in the IGBT module.

The same reference is internally used by the modulator, resulting in a ratiometric system solution that minimizes the overall temperature drift of the sensing path. Figure 47 shows a simplified schematic of the AMC1035 used for temperature sensing of the IGBT module.

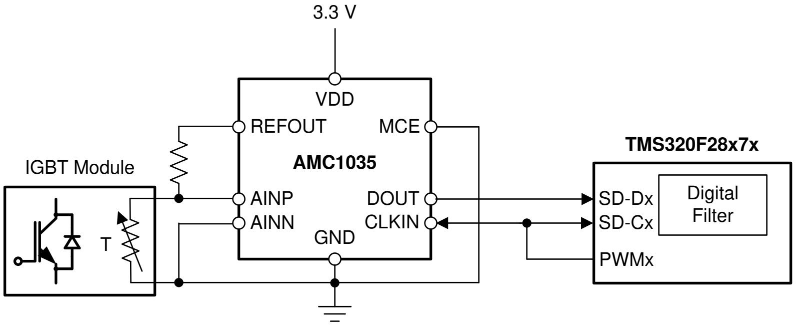


Figure 47. Using the AMC1035 for Temperature Sensing

8.2.3 What to Do and What Not to Do

Do not leave the analog inputs of the AMC1035 unconnected (floating) when the device is powered up. If either modulator input is left floating, the input bias current may drive this input beyond the specified common-mode input voltage range. If both inputs are beyond that range, the gain of the front-end diminishes. In both cases, the modulator outputs a fail-safe bitstream as described in the *Fail-Safe Output* section.

9 Power Supply Recommendations

For decoupling of the power supply, a 0.1-µF capacitor is recommended to be placed as close to the VDD pin of the AMC1035 as possible, as shown in Figure 48, followed by an additional capacitor in the range of 1 µF to 10 µF.

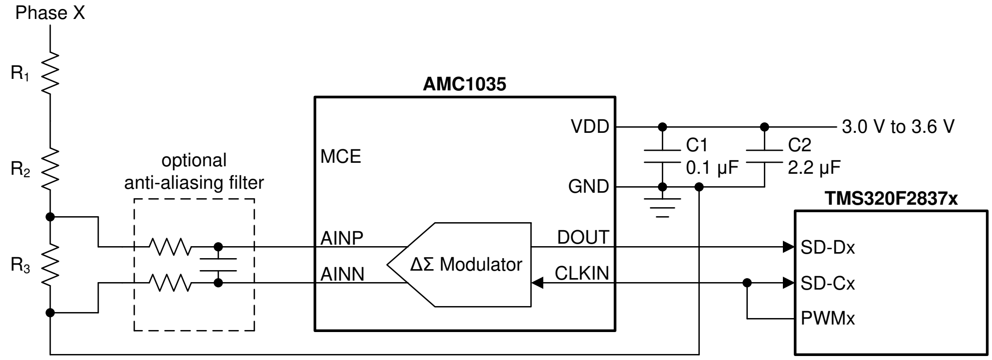


Figure 48. Decoupling the AMC1035

Safety considerations or high common-mode voltage levels may require the AMC1035 to be galvanically isolated from other parts of the system. Figure 49 shows an example of a circuit that uses the ISO7721 to isolate the signal path and the SN6501 and a transformer to generate the required isolated power.

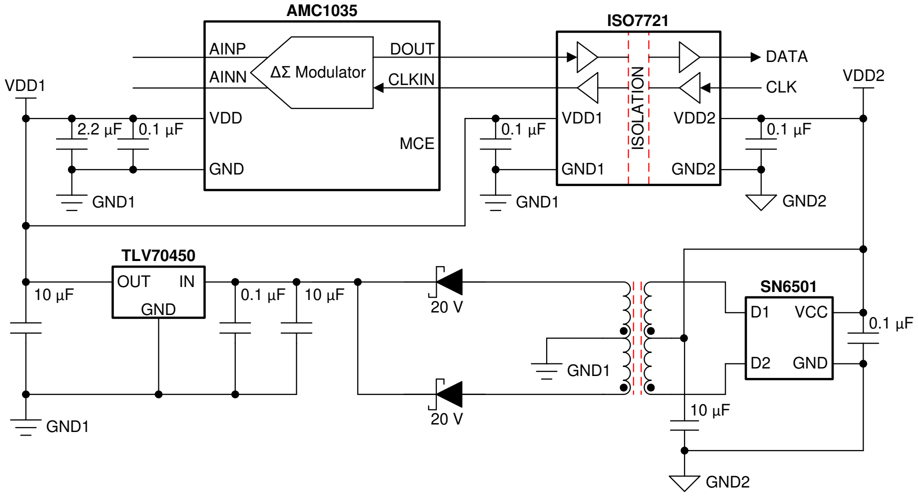


Figure 49. Galvanic Isolation of the AMC1035

Figure 50 shows an alternative solution that uses the ISOW7821 to isolate the signal path and provide the isolated power supply for the AMC1035.

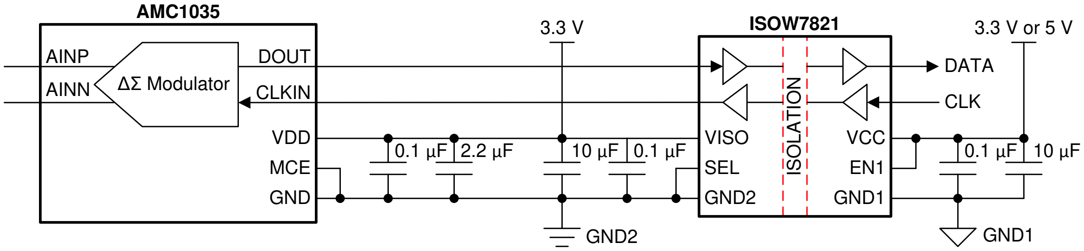


Figure 50. Galvanic Isolation of the AMC1035 for PCB Space-Constrained Applications

10 Layout

10.1 Layout Guidelines

Figure 51 shows two layout recommendations for designs based on 1206-SMD or 0603-SMD size decoupling capacitors placed as close as possible to the AMC1035. For best performance, place the AMC1035 as close as possible to the source of the analog signal to be converted and keep the layout of the AINP and AINN traces symmetrical.

10.2 Layout Example

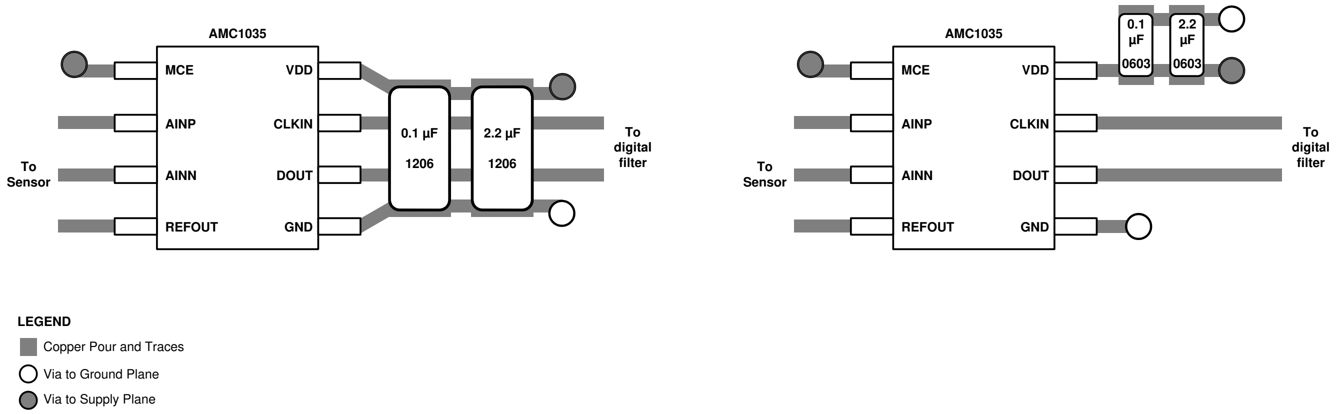


Figure 51. Recommended Layout of the AMC1035

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMS320F28004x Piccolo™ Microcontrollers* data sheet
- Texas Instruments, *TMS320F2807x Piccolo™ Microcontrollers* data sheet
- Texas Instruments, *TMS320F2837xD Dual-Core Delfino™ Microcontrollers* data sheet
- Texas Instruments, *ISO772x High-Speed, Robust EMC Reinforced Dual-Channel Digital Isolators* data sheet
- Texas Instruments, *MSP430F677x Polyphase Metering SoCs* data sheet
- Texas Instruments, *AMC1210 Quad Digital Filter for 2nd-Order Delta-Sigma Modulator* data sheet
- Texas Instruments, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application report
- Texas Instruments, *AMC1306x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With High CMTI* data sheet
- Texas Instruments, *CDCLVC11xx 3.3-V and 2.5-V LVCMOS High-Performance Clock Buffer Family* data sheet
- Texas Instruments, *LM117, LM317-N Wide Temperature Three-Pin Adjustable Regulator* data sheet
- Texas Instruments, *SN6502 Low-Noise 350mA, 410 kHz Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *ISOW7821 HIgh-Performance, 5000-*V_{RMS} *Reinforced Dual-Channel Digital Isolator With Integrated High-Efficiency, Low-Emissions DC-DC Converter* data sheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1035D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC1035	Samples
AMC1035DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC1035	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AMC1035 :

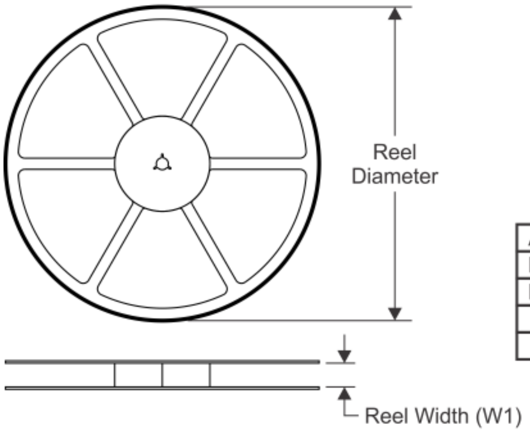
- Automotive: AMC1035-Q1

NOTE: Qualified Version Definitions:

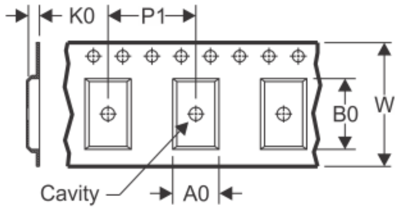
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

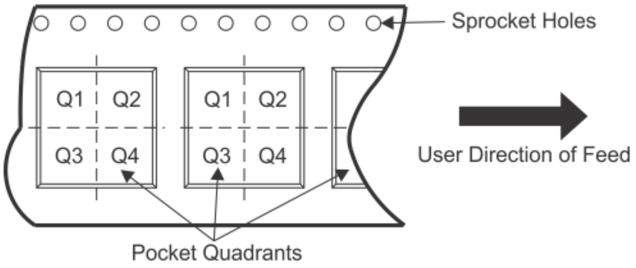


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

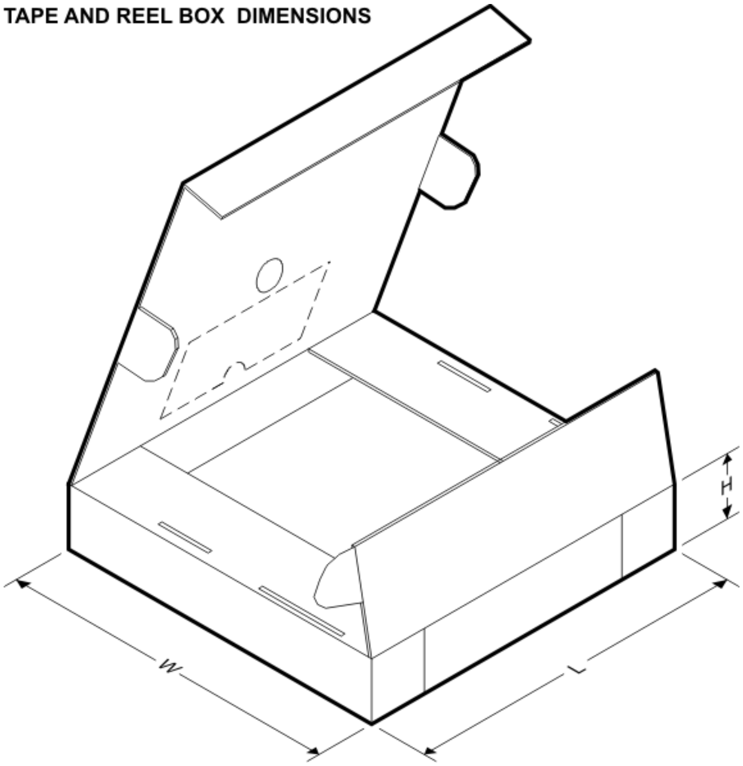
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1035DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



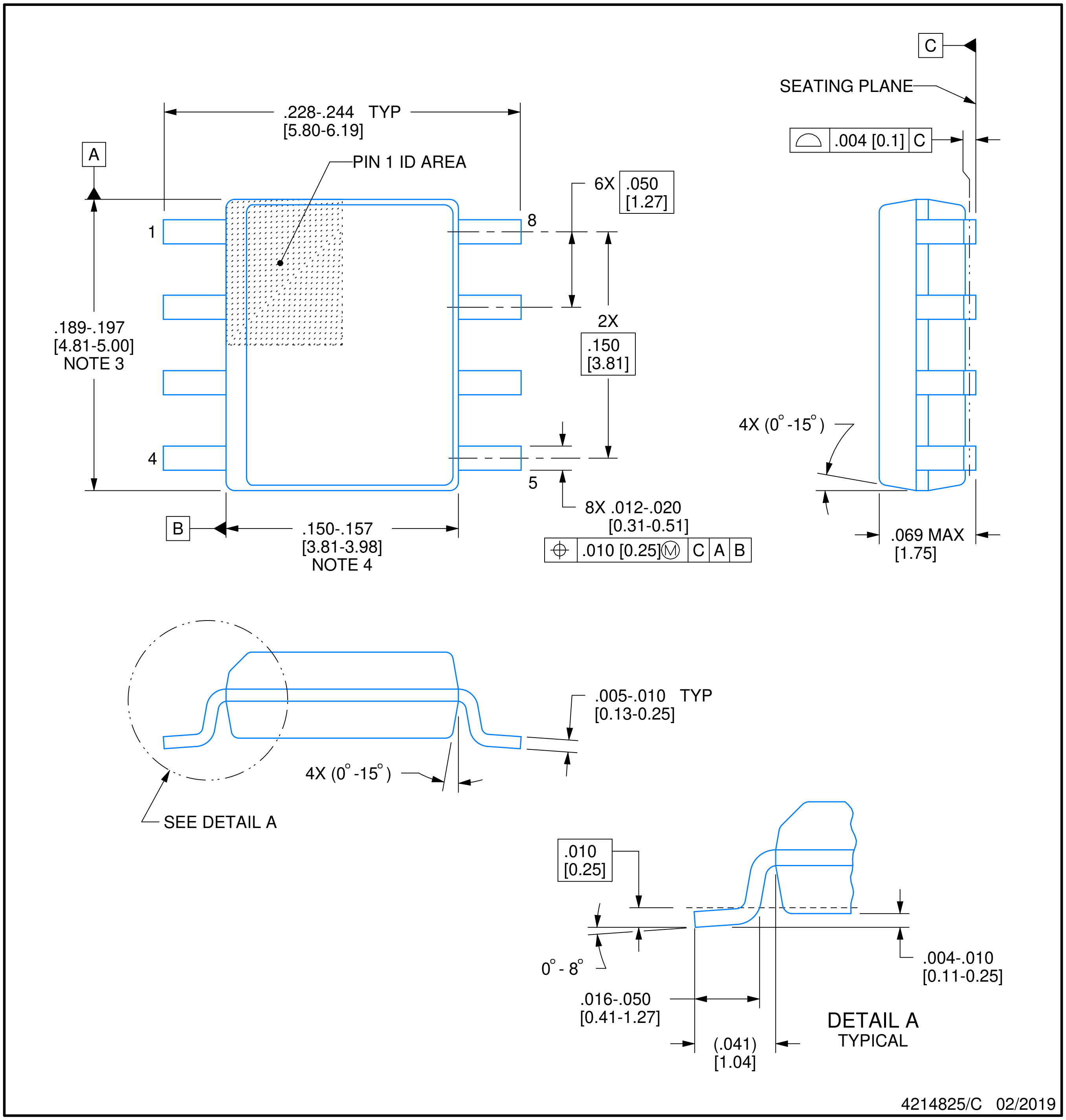
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1035DR	SOIC	D	8	2500	340.5	338.1	20.6

PACKAGE OUTLINE

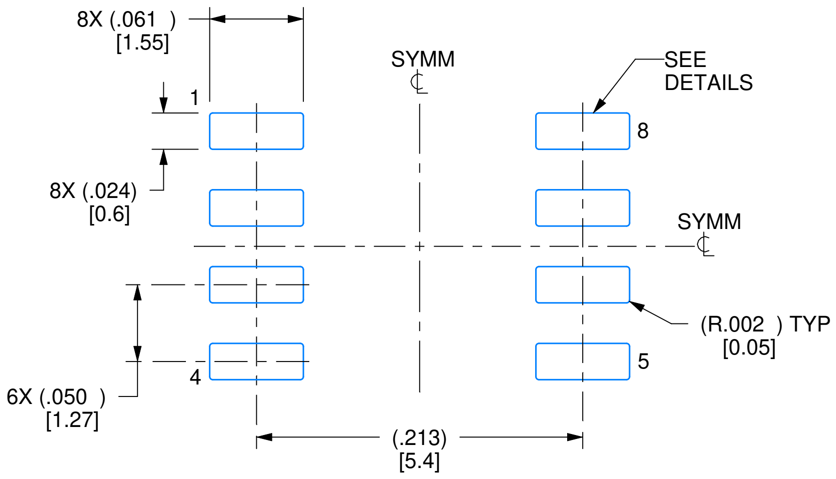
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

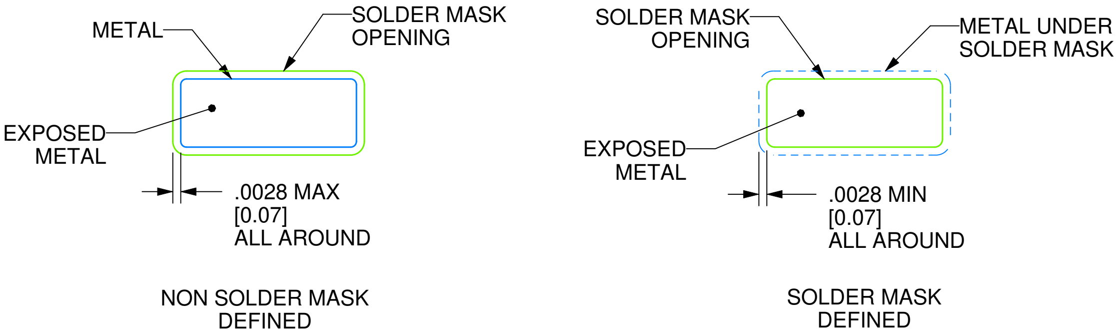


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



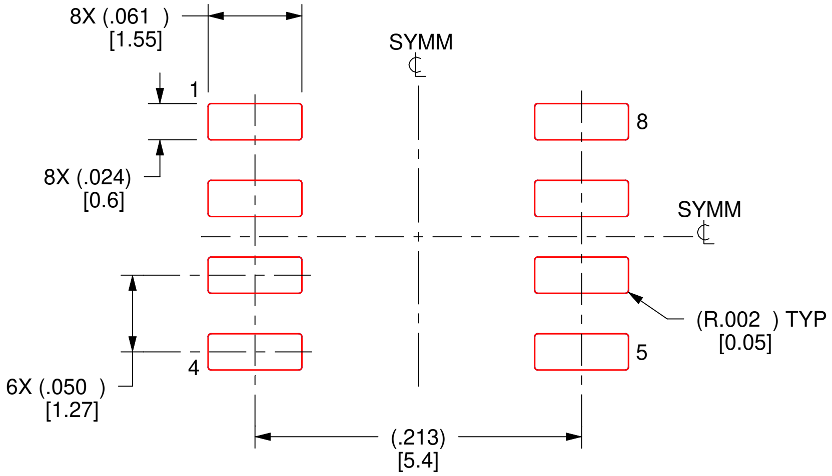
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2020, Texas Instruments Incorporated