

Programmable Timing Control Hub™ for P4™

Recommended Application:

CK-408 clock for Intel® 845 chipset.

Output Features:

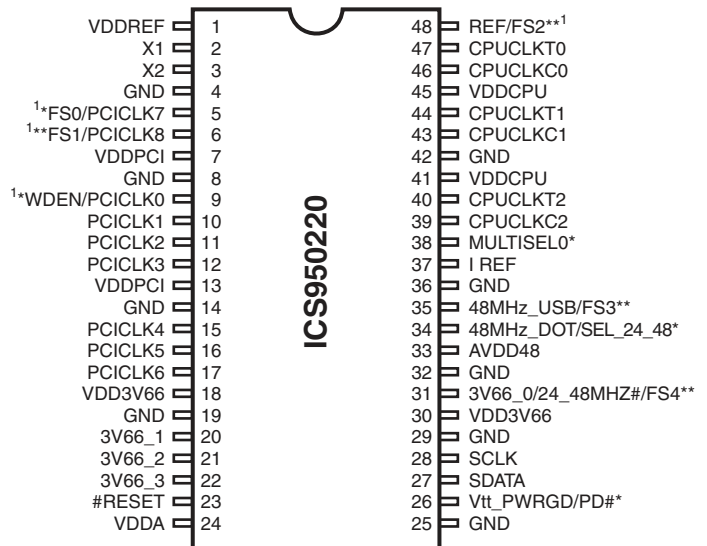
- 3 - Pairs of differential CPU clocks @ 3.3V
- 3 - 3V66 @ 3.3V
- 9 - PCI @ 3.3V
- 2 - 48MHz @ 3.3V fixed
- 1 - 24_48MHz @ 3.3V, 48MHz, 24MHz or 66MHz
- 1 - REF @ 3.3V, 14.318MHz

Features/Benefits:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I²C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

Key Specifications:

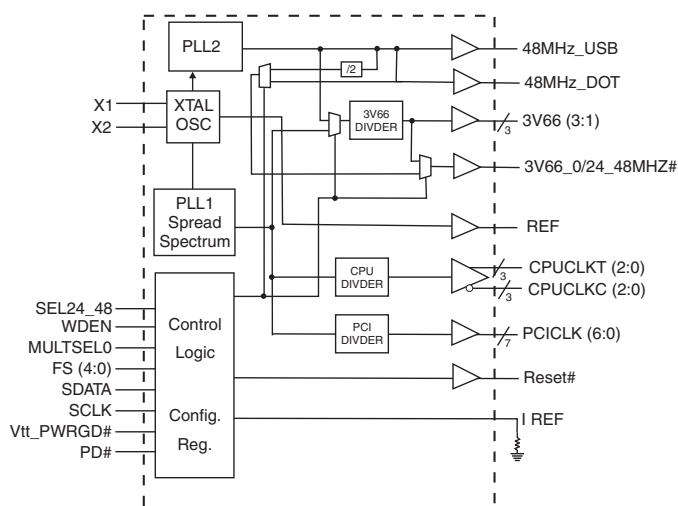
- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- CPU Output Skew <100ps

Pin Configuration

48-Pin 300-mil SSOP

1. These outputs have 2X drive strength.

* Internal Pull-up resistor of 120K to VDD

** these inputs have 120K internal pull-down to GND

Block Diagram

Frequency Table

| FS4 | FS3 | FS2 | FS1 | FS0 | CPUCLK MHz | 3V66 MHz | PCICLK MHz |
|-----|-----|-----|-----|-----|------------|----------|------------|
| 0 | 0 | 0 | 0 | 1 | 100.00 | 66.67 | 33.33 |
| 1 | 0 | 0 | 0 | 1 | 133.33 | 66.67 | 33.33 |
| 1 | 1 | 1 | 1 | 0 | 66.67 | 66.67 | 33.34 |
| 1 | 1 | 1 | 1 | 1 | 200.00 | 66.67 | 33.33 |

For additional frequency selections please refer to Byte 0.

Power Groups

VDDA = Analog Core PLL

VDDREF = REF, Xtal

AVDD48 = 48MHz

General Description

The **ICS950220** is a single chip clock solution for desktop designs using the Intel 845 chipset with PC133 or DDR memory. It provides all necessary clock signals for such a system.

The **ICS950220** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I²C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Pin Description

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|----------------------------------|------------------|------|---|
| 1, 7, 13, 18, 30, 41, 45 | VDD | PWR | 3.3V power supply. |
| 2 | X1 | IN | Crystal input, has internal load cap (33pF) and feedback resistor from X2. |
| 3 | X2 | OUT | Crystal output, nominally 14.318MHz. Has internal load cap (33pF). |
| 4, 8, 14, 19, 25, 29, 32, 36, 42 | GND | PWR | Ground pins for 3.3V supply. |
| 22, 21, 20 | 3V66 (3:1) | OUT | 3.3V Fixed 66MHz clock outputs for HUB. |
| 5 | PCICLK7 | OUT | 3.3V PCI clock output |
| | FS0 | IN | Logic input frequency select bit. Input latched at power on. |
| 6 | PCICLK8 | OUT | 3.3V PCI clock output. |
| | FS1 | IN | Logic input frequency select bit. Input latched at power on. |
| 9 | WDEN | IN | Hardware enable of watch dog circuit. Enabled when latched high. |
| | PCICLK0 | OUT | 3.3V PCI clock output. |
| 17, 16, 15, 12, 11, 10 | PCICLK (6:1) | OUT | 3.3V PCI clock outputs. |
| 23 | RESET# | OUT | Real time system reset signal for frequency value or watchdog timer timeout. This signal is active low. |
| 24 | VDDA | PWR | Analog power 3.3V. |
| 26 | Vtt_PWRGD | IN | This 3.3V LVTTTL input is a level sensitive strobe used to determine when FS (4:0) inputs are valid and are ready to be sampled (active high). |
| | PD# | IN | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. |
| 28 | SCLK | IN | Clock pin for I ² C circuitry 5V tolerant. |
| 27 | SDATA | I/O | Data pin for I ² C circuitry 5V tolerant. |
| 31 | 3V66_0/24_48MHZ# | OUT | 3.3V output selectable through I ² C to be 66MHz from internal VCO or 48MHz/24MHz. |
| | FS4 | IN | Logic input frequency select bit. Input latched at power on. |
| 33 | AVDD48 | PWR | Analog power 3.3V. |
| 34 | 48MHz_DOT | OUT | 3.3V Fixed 48MHz clock output for DOT. |
| | SEL24_48 | IN | This selects the frequency for the SEL24_48 output. High = 24MHz, Low = 48MHz. |
| 35 | FS3 | IN | Logic input frequency select bit. Input latched at power on. |
| | 48MHz_USB | OUT | 3.3V Fixed 48MHz clock output for USB. |
| 37 | I REF | OUT | This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. |
| 38 | MULTSELO | IN | 3.3V LVTTTL input for selecting the current multiplier for CPU outputs |
| 39, 43, 46 | CPUCLKC (2:0) | OUT | "Complementary" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias. |
| 40, 44, 47 | CPUCLKT (2:0) | OUT | "True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias. |
| 48 | FS2 | IN | Logic input frequency select bit. Input latched at power on. |
| | REF | OUT | 3.3V, 14.318MHz reference clock output. |

Maximum Allowed Current

| | |
|--|--|
| Condition | Max 3.3V supply consumption Max discrete cap loads, Vdd = 3.465V All static inputs = Vdd or GND |
| Powerdown Mode (PWRDWN# = 0) | 40mA |
| Full Active | 360mA |

Host Swing Select Functions

| MULTISEL0 | Board Target Trace/Term Z | Reference R, Iref = $V_{DD}/(3 \cdot R_r)$ | Output Current | Voh @ Z |
|------------------|------------------------------|--|-------------------|-----------|
| 0 | 50 ohms | Rr = 221 1%, Iref = 5.00mA | Ioh = 4 * I REF | 1.0V @ 50 |
| 1 | 50 ohms | Rr = 475 1%, Iref = 2.32mA | Ioh = 6 * I REF | 0.7V @ 50 |

General SMBus serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address $D2_{(H)}$ | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | X Byte |
| ○ | | |
| ○ | | |
| ○ | | |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address $D2_{(H)}$ | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address $D3_{(H)}$ | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count = X |
| ACK | | |
| ACK | | X Byte |
| | | |
| Beginning Byte N | | |
| ○ | | |
| ○ | | |
| ○ | | |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

Byte 0: Functionality and frequency select register (Default=0)

| Bit | Description | | | | | | | | | PWD |
|----------------|---|------|------|------|--------|---------------|-------------|------------------------|------------------------|--------|
| Bit (2,7:4) | Bit2 | Bit7 | Bit6 | Bit5 | Bit4 | CPUCLK MHz | 3V66 MHz | PCICLK MHz | Spread % | Note 1 |
| | FS4 | FS3 | FS2 | FS1 | FS0 | | | | | |
| | 0 | 0 | 0 | 0 | 0 | 100.90 | 67.27 | 33.63 | +/-0.35% center spread | |
| | 0 | 0 | 0 | 0 | 1 | 100.00 | 66.67 | 33.33 | 0 to -0.6% down spread | |
| | 0 | 0 | 0 | 1 | 0 | 103.00 | 68.67 | 34.33 | +/-0.35% center spread | |
| | 0 | 0 | 0 | 1 | 1 | 105.00 | 70.00 | 35.00 | +/-0.35% center spread | |
| | 0 | 0 | 1 | 0 | 0 | 107.00 | 71.33 | 35.67 | +/-0.35% center spread | |
| | 0 | 0 | 1 | 0 | 1 | 109.00 | 72.67 | 36.33 | +/-0.35% center spread | |
| | 0 | 0 | 1 | 1 | 0 | 111.00 | 74.00 | 37.00 | +/-0.35% center spread | |
| | 0 | 0 | 1 | 1 | 1 | 114.00 | 76.00 | 38.00 | +/-0.35% center spread | |
| | 0 | 1 | 0 | 0 | 0 | 117.00 | 78.00 | 39.00 | +/-0.35% center spread | |
| | 0 | 1 | 0 | 0 | 1 | 120.00 | 80.00 | 40.00 | +/-0.35% center spread | |
| | 0 | 1 | 0 | 1 | 0 | 127.00 | 84.67 | 42.33 | +/-0.35% center spread | |
| | 0 | 1 | 0 | 1 | 1 | 130.00 | 86.67 | 43.33 | +/-0.35% center spread | |
| | 0 | 1 | 1 | 0 | 0 | 133.33 | 88.89 | 44.44 | +/-0.35% center spread | |
| | 0 | 1 | 1 | 0 | 1 | 170.00 | 56.67 | 28.33 | +/-0.35% center spread | |
| | 0 | 1 | 1 | 1 | 0 | 180.00 | 60.00 | 30.00 | +/-0.35% center spread | |
| | 0 | 1 | 1 | 1 | 1 | 190.00 | 63.33 | 31.67 | +/-0.35% center spread | |
| | 1 | 0 | 0 | 0 | 0 | 133.90 | 66.95 | 33.48 | +/-0.35% center spread | |
| | 1 | 0 | 0 | 0 | 1 | 133.33 | 66.67 | 33.33 | 0 to -0.6% down spread | |
| | 1 | 0 | 0 | 1 | 0 | 120.00 | 60.00 | 30.00 | +/-0.35% center spread | |
| | 1 | 0 | 0 | 1 | 1 | 125.00 | 62.50 | 31.25 | +/-0.35% center spread | |
| | 1 | 0 | 1 | 0 | 0 | 134.90 | 67.45 | 33.73 | +/-0.35% center spread | |
| | 1 | 0 | 1 | 0 | 1 | 137.00 | 68.50 | 34.25 | +/-0.35% center spread | |
| | 1 | 0 | 1 | 1 | 0 | 139.00 | 69.50 | 34.75 | +/-0.35% center spread | |
| | 1 | 0 | 1 | 1 | 1 | 141.00 | 70.50 | 35.25 | +/-0.35% center spread | |
| | 1 | 1 | 0 | 0 | 0 | 143.00 | 71.50 | 35.75 | +/-0.35% center spread | |
| | 1 | 1 | 0 | 0 | 1 | 145.00 | 72.50 | 36.25 | +/-0.35% center spread | |
| 1 | 1 | 0 | 1 | 0 | 150.00 | 75.00 | 37.5 | +/-0.35% center spread | | |
| 1 | 1 | 0 | 1 | 1 | 155.00 | 77.50 | 38.75 | +/-0.35% center spread | | |
| 1 | 1 | 1 | 0 | 0 | 160.00 | 80.00 | 40.00 | +/-0.35% center spread | | |
| 1 | 1 | 1 | 0 | 1 | 170.00 | 85.00 | 42.50 | +/-0.35% center spread | | |
| 1 | 1 | 1 | 1 | 0 | 66.67 | 66.67 | 33.34 | 0 to -0.6% down spread | | |
| 1 | 1 | 1 | 1 | 1 | 200.00 | 66.67 | 33.33 | 0 to -0.6% down spread | | |
| Bit 3 | 0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit 2,7:4 | | | | | | | | | 0 |
| Bit 1 | 0 - Normal 1 - Spread spectrum enable | | | | | | | | | 1 |
| Bit 0 | 0 - Watch dog safe frequency will be selected by latch inputs 1 - Watch dog safe frequency will be programmed by Byte 10 bit (4:0) | | | | | | | | | 0 |

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

Byte 1: Output Control Register
(1 = enable, 0 = disable)

| Bit | Pin# | PWD | Description |
|------|--------|-----|---------------|
| Bit7 | 40, 39 | 1 | CPUT/C2 |
| Bit6 | 44, 43 | 1 | CPUT/C1 |
| Bit5 | 47, 46 | 1 | CPUT/C0 |
| Bit4 | - | X | FS4 Read back |
| Bit3 | - | X | FS3 Read back |
| Bit2 | - | X | FS2 Read back |
| Bit1 | - | X | FS1 Read back |
| Bit0 | - | X | FS0 Read back |

Byte 2: Output Control Register
(1 = enable, 0 = disable)

| Bit | Pin# | PWD | Description |
|------|------|-----|---------------------|
| Bit7 | - | X | MULTSEL (Read back) |
| Bit6 | 17 | 1 | PCICLK_6 |
| Bit5 | 16 | 1 | PCICLK_5 |
| Bit4 | 15 | 1 | PCICLK_4 |
| Bit3 | 12 | 1 | PCICLK_3 |
| Bit2 | 11 | 1 | PCICLK_2 |
| Bit1 | 10 | 1 | PCICLK_1 |
| Bit0 | 9 | 1 | PCICLK_0 |

Byte 3: Output Control Register
(1 = enable, 0 = disable)

| Bit | Pin# | PWD | Description |
|------|------|-----|---|
| Bit7 | 34 | 1 | 48MHZ_DOT |
| Bit6 | 35 | 1 | 48MHz_USB |
| Bit5 | - | 1 | Reset gear shift detect 1 = Enable, 0 = Disable |
| Bit4 | - | X | Reserved |
| Bit3 | 31 | 0 | 3V66_0/24_48MHZ#, (default) 1 = 66.66MHz, 0 = 24_48MHZ# |
| Bit2 | - | X | Reserved |
| Bit1 | 6 | 1 | PCICLK8 |
| Bit0 | 5 | 1 | PCICLK7 |

Byte 4: Output Control Register
(1 = enable, 0 = disable)

| Bit | Pin# | PWD | Description |
|-------|------|-----|--|
| Bit 7 | - | 1 | Async. 3V66 control bit 0 : 3V66 / PCI = 64/32 MHz asynchronous with CPU 1 : 3V66 / PCI = 66.6/33.3 MHz synchronous with CPU |
| Bit 6 | - | X | Reserved |
| Bit 5 | - | X | Reserved |
| Bit 4 | 31 | 1 | 3V66_0/24_48MHZ# |
| Bit 3 | - | X | Reserved |
| Bit 2 | 22 | 1 | 3V66_3 |
| Bit 1 | 21 | 1 | 3V66_2 |
| Bit 0 | 20 | 1 | 3V66_1 |

Notes:

1. PWD = Power on Default
2. For disabled clocks, they stop low for single ended clocks. Differential CPU clocks stop with CPUCLKT at high, CPUCLKC off, and external resistor termination will bring CPUCLKC low.

Byte 5: Programming Edge Rate
(1 = enable, 0 = disable)

| Bit | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | X | 1 | (Reserved) |
| Bit 6 | X | 1 | (Reserved) |
| Bit 5 | X | 1 | (Reserved) |
| Bit 4 | X | 1 | (Reserved) |
| Bit 3 | X | 1 | (Reserved) |
| Bit 2 | X | 1 | (Reserved) |
| Bit 1 | X | 1 | (Reserved) |
| Bit 0 | X | 1 | (Reserved) |

Byte 6: Vendor ID Register
(1 = enable, 0 = disable)

| Bit | Name | PWD | Description |
|-------|------------------|-----|--|
| Bit 7 | Revision ID Bit3 | X | Revision ID values will be based on individual device's revision |
| Bit 6 | Revision ID Bit2 | X | |
| Bit 5 | Revision ID Bit1 | X | |
| Bit 4 | Revision ID Bit0 | X | |
| Bit 3 | Vendor ID Bit3 | 0 | (Reserved) |
| Bit 2 | Vendor ID Bit2 | 0 | (Reserved) |
| Bit 1 | Vendor ID Bit1 | 0 | (Reserved) |
| Bit 0 | Vendor ID Bit0 | 1 | (Reserved) |

Byte 7: Revision ID and Device ID Register

| Bit | Name | PWD | Description |
|-------|------------|-----|---|
| Bit 7 | Device ID7 | 0 | Device ID values will be based on individual device "22H" in this case. |
| Bit 6 | Device ID6 | 0 | |
| Bit 5 | Device ID5 | 1 | |
| Bit 4 | Device ID4 | 0 | |
| Bit 3 | Device ID3 | 0 | |
| Bit 2 | Device ID2 | 0 | |
| Bit 1 | Device ID1 | 1 | |
| Bit 0 | Device ID0 | 0 | |

Byte 8: Byte Count Read Back Register

| Bit | Name | PWD | Description |
|-------|-------|-----|---|
| Bit 7 | Byte7 | 0 | Note: Writing to this register will configure byte count and how many bytes will be read back, default is 0FH = 15 bytes. |
| Bit 6 | Byte6 | 0 | |
| Bit 5 | Byte5 | 0 | |
| Bit 4 | Byte4 | 0 | |
| Bit 3 | Byte3 | 1 | |
| Bit 2 | Byte2 | 1 | |
| Bit 1 | Byte1 | 1 | |
| Bit 0 | Byte0 | 1 | |

Byte 9: Watchdog Timer Count Register

| Bit | Name | PWD | Description |
|-------|------|-----|---|
| Bit 7 | WD7 | 0 | The decimal representation of these 8 bits correspond to X • 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 8 • 290ms = 2.3 seconds. |
| Bit 6 | WD6 | 0 | |
| Bit 5 | WD5 | 0 | |
| Bit 4 | WD4 | 0 | |
| Bit 3 | WD3 | 1 | |
| Bit 2 | WD2 | 0 | |
| Bit 1 | WD1 | 0 | |
| Bit 0 | WD0 | 0 | |

Byte 10: Programming Enable bit 8 Watchdog Control Register

| Bit | Name | PWD | Description |
|-------|----------------|-----|--|
| Bit 7 | Program Enable | 0 | Programming Enable bit 0 = no programming. Frequencies are selected by HW latches or Byte0 1 = enable all PC programming. |
| Bit 6 | WD Enable | 1 | Watchdog Enable bit. This bit will over write WDEN latched value. 0 = disable, 1 = Enable. |
| Bit 5 | WD Alarm | 1 | Watchdog Alarm Status 0 = normal 1= alarm status |
| Bit 4 | SF4 | 0 | Watchdog safe frequency bits. Writing to these bits will configure the safe frequency corresponding to Byte 0 Bit 2, 7:4 table |
| Bit 3 | SF3 | 0 | |
| Bit 2 | SF2 | 0 | |
| Bit 1 | SF1 | 0 | |
| Bit 0 | SF0 | 0 | |

Byte 11: VCO Frequency M Divider (Reference divider) Control Register

| Bit | Name | PWD | Description |
|-------|--------|-----|---|
| Bit 7 | Ndiv 8 | X | N divider bit 8 |
| Bit 6 | Mdiv 6 | X | The decimal representation of Mdiv (6:0) correspond to the reference divider value. Default at power up is equal to the latched inputs selection. |
| Bit 5 | Mdiv 5 | X | |
| Bit 4 | Mdiv 4 | X | |
| Bit 3 | Mdiv 3 | X | |
| Bit 2 | Mdiv 2 | X | |
| Bit 1 | Mdiv 1 | X | |
| Bit 0 | Mdiv 0 | X | |

Byte 12: VCO Frequency N Divider (VCO divider) Control Register

| Bit | Name | PWD | Description |
|-------|--------|-----|--|
| Bit 7 | Ndiv 7 | X | The decimal representation of Ndiv (8:0) correspond to the VCO divider value. Default at power up is equal to the latched inputs selection. Notice Ndiv 8 is located in Byte 11. |
| Bit 6 | Ndiv 6 | X | |
| Bit 5 | Ndiv 5 | X | |
| Bit 4 | Ndiv 4 | X | |
| Bit 3 | Ndiv 3 | X | |
| Bit 2 | Ndiv 2 | X | |
| Bit 1 | Ndiv 1 | X | |
| Bit 0 | Ndiv 0 | X | |

Byte 13: Spread Spectrum Control Register

| Bit | Name | PWD | Description |
|-------|------|-----|--|
| Bit 7 | SS 7 | X | The Spread Spectrum (12:0) bit will program the spread percentage. Spread percent needs to be calculated based on the VCO frequency, spreading profile, spreading amount and spread frequency. It is recommended to use ICS software for spread programming. Default power on is latched FS divider. |
| Bit 6 | SS 6 | X | |
| Bit 5 | SS 5 | X | |
| Bit 4 | SS 4 | X | |
| Bit 3 | SS 3 | X | |
| Bit 2 | SS 2 | X | |
| Bit 1 | SS 1 | X | |
| Bit 0 | SS 0 | X | |

Byte 14: Spread Spectrum Control Register

| Bit | Name | PWD | Description |
|-------|----------|-----|------------------------|
| Bit 7 | Reserved | X | Reserved |
| Bit 6 | Reserved | X | Reserved |
| Bit 5 | Reserved | X | Reserved |
| Bit 4 | SS 12 | X | Spread Spectrum Bit 12 |
| Bit 3 | SS 11 | X | Spread Spectrum Bit 11 |
| Bit 2 | SS 10 | X | Spread Spectrum Bit 10 |
| Bit 1 | SS 9 | X | Spread Spectrum Bit 9 |
| Bit 0 | SS 8 | X | Spread Spectrum Bit 8 |

Byte 15: Output Divider Control Register

| Bit | Name | PWD | Description |
|-------|-----------|-----|---|
| Bit 7 | CPU Div 3 | 0 | CPU 2 clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider. |
| Bit 6 | CPU Div 2 | 1 | |
| Bit 5 | CPU Div 1 | 0 | |
| Bit 4 | CPU Div 0 | 0 | |
| Bit 3 | CPU Div 3 | 0 | CPU (1:0) clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider. |
| Bit 2 | CPU Div 2 | 1 | |
| Bit 1 | CPU Div 1 | 0 | |
| Bit 0 | CPU Div 0 | 0 | |

Byte 16: Output Divider Control Register

| Bit | Name | PWD | Description |
|-------|-------|-----|--|
| Bit 7 | Div 3 | 0 | 3V66_0 clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider. |
| Bit 6 | Div 2 | 1 | |
| Bit 5 | Div 1 | 0 | |
| Bit 4 | Div 0 | 1 | |
| Bit 3 | Div 3 | 0 | 3V66 (3:1) clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider. |
| Bit 2 | Div 2 | 1 | |
| Bit 1 | Div 1 | 0 | |
| Bit 0 | Div 0 | 1 | |

Byte 17: Output Divider Control Register

| Bit | Name | PWD | Description |
|-------|-----------|-----|---|
| Bit 7 | 3V66_INV | 0 | 3V66_0 Phase Inversion bit |
| Bit 6 | 3V66_INV | 0 | 3V66 (3:1) Phase Inversion bit |
| Bit 5 | CPU_INV | 0 | CPU 2 Phase Inversion bit |
| Bit 4 | CPU_INV | 0 | CPU (1:0) Phase Inversion bit |
| Bit 3 | PCI Div 3 | 1 | PCI clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 2. Default at power up is latched FS divider. |
| Bit 2 | PCI Div 2 | 0 | |
| Bit 1 | PCI Div 1 | 0 | |
| Bit 0 | PCI Div 0 | 1 | |

Table 1

| Div (3:2) | 00 | 01 | 10 | 11 |
|-----------|----|-----|-----|-----|
| Div (1:0) | | | | |
| 00 | /2 | /4 | /8 | /16 |
| 01 | /3 | /6 | /12 | /24 |
| 10 | /5 | /10 | /20 | /40 |
| 11 | /7 | /14 | /28 | /56 |

Table 2

| Div (3:2) | 00 | 01 | 10 | 11 |
|-----------|----|-----|-----|-----|
| Div (1:0) | | | | |
| 00 | /4 | /8 | /16 | /32 |
| 01 | /3 | /6 | /12 | /24 |
| 10 | /5 | /10 | /20 | /40 |
| 11 | /9 | /18 | /36 | /72 |

Byte 18: Group Skew Control Register

| Bit | Name | PWD | Description |
|-------|------------|-----|--|
| Bit 7 | CPU_Skew 1 | 0 | These 2 bits delay the CPUCLKC/T2 with respect to CPUCLKC/T (1:0) 00 = 0ps 01 = 250ps 10 = 500ps 11 =750ps |
| Bit 6 | CPU_Skew 0 | 0 | |
| Bit 5 | Reserved | 0 | Reserved |
| Bit 4 | Reserved | 0 | Reserved |
| Bit 3 | CPU_Skew 1 | 0 | These 2 bits delay the CPUCLKC/T (1:0) clock with respect to CPUCLKC/T2 00 = 0ps 01 = 250ps 10 = 500ps 11 = 750ps |
| Bit 2 | CPU_Skew 0 | 0 | |
| Bit 1 | Reserved | 0 | Reserved |
| Bit 0 | Reserved | 0 | Reserved |

Byte 19: Group Skew Control Register

| Bit | Name | PWD | Description |
|-------|-------------|-----|--|
| Bit 7 | 3V66_Skew 1 | 0 | These 2 bits delay the 3V66 (3:1) with respect to CPUCLK 00 = 0ps 01 = 250ps 10 = 500ps 11 =750ps |
| Bit 6 | 3V66_Skew 0 | 0 | |
| Bit 5 | Reserved | 0 | Reserved |
| Bit 4 | Reserved | 0 | Reserved |
| Bit 3 | 3V66_Skew 1 | 0 | These 2 bits delay the 3V66_0 with respect to CPUCLK 00 = 0ps 01 = 250ps 10 = 500ps 11 =750ps |
| Bit 2 | 3V66_Skew 0 | 0 | |
| Bit 1 | Reserved | 0 | Reserved |
| Bit 0 | Reserved | 0 | Reserved |

Byte 20: Group Skew Control Register

| Bit | Name | PWD | Description |
|-------|------------|-----|---|
| Bit 7 | PCI_Skew 3 | 1 | These 4 bits can change the CPU to PCI (6:0) skew from -0.3ns 1.2ns. Default at power up is 0.5ns. Each binary increment or decrement of Bits (3:0) will increase or decrease the delay of the PCI clocks by 100ps. |
| Bit 6 | PCI_Skew 2 | 0 | |
| Bit 5 | PCI_Skew 1 | 0 | |
| Bit 4 | PCI_Skew 0 | 0 | |
| Bit 3 | PCI_Skew 3 | 1 | These 4 bits can change the CPU to PCI (8:7) skew from -0.6ns 1.2ns. Default at power up is 0.4ns. Each binary increment or decrement of Bit (3:0) will increase or decrease the delay of the PCI clocks by 100ps. |
| Bit 2 | PCI_Skew 2 | 0 | |
| Bit 1 | PCI_Skew 1 | 0 | |
| Bit 0 | PCI_Skew 0 | 0 | |

Byte 21: Slew Rate Control Register

| Bit | Name | PWD | Description |
|-------|-------------------|-----|---|
| Bit 7 | Reserved | 1 | Reserved |
| Bit 6 | Reserved | 0 | Reserved |
| Bit 5 | PCIF Slew 1 | 1 | PCIF(1:0) clock slew rate control bits. 01 = strong; 11 = normal; 10 = weak |
| Bit 4 | PCIF Slew 0 | 0 | |
| Bit 3 | 3V66 (3:1) Slew 1 | 1 | 3V66 (3:1) clock slew rate control bits. 01 = strong; 11 = normal; 10 = weak |
| Bit 2 | 3V66 (3:1) Slew 1 | 0 | |
| Bit 1 | 3V66_0 Slew 1 | 1 | 3V66_0 clock slew rate control bits. 01 = strong; 11 = normal; 10 = weak |
| Bit 0 | 3V66_0 Slew 0 | 0 | |

Byte 22: Slew Rate Control Register

| Bit | Name | PWD | Description |
|-------|------------------|-----|--|
| Bit 7 | REF Slew 1 | 1 | REF clock slew rate control bits. 01 = strong; 11 = normal; 10 = weak |
| Bit 6 | REF Slew 0 | 0 | |
| Bit 5 | PCI (6:4) Slew 1 | 1 | PCI (6:4) clock slew rate control bits. 01 = strong; 11 = normal; 10 = weak |
| Bit 4 | PCI (6:4) Slew 0 | 0 | |
| Bit 3 | PCI (3:1) Slew 1 | 1 | PCI (3:1) clock slew rate control bits. 01 = strong; 11 = normal; 10 = weak |
| Bit 2 | PCI (3:1) Slew 0 | 0 | |
| Bit 1 | PCI0 Slew 1 | 1 | PCI0 clock slew rate control bits. 01 = strong; 11 = normal; 10 = weak |
| Bit 0 | PCI0 Slew 0 | 0 | |

Byte 23: Slew Rate Control Register

| Bit | Name | PWD | Description |
|-------|--------------|-----|--|
| Bit 7 | Reserved | X | Reserved |
| Bit 6 | Reserved | X | |
| Bit 5 | VCH Slew 1 | 1 | VCH clock slew rate control bits. 01 = strong; 11 = normal; 10 = weak |
| Bit 4 | VCH Slew 0 | 0 | |
| Bit 3 | 48USB Slew 1 | 1 | 48USB clock slew rate control bits. 01 = strong; 11 = normal; 10 = weak |
| Bit 2 | 48USB Slew 0 | 0 | |
| Bit 1 | 48DOT Slew 1 | 1 | 48DOT clock slew rate control bits. 01 = strong; 11 = normal; 10 = weak |
| Bit 0 | 48DOT Slew 0 | 0 | |

Absolute Maximum Ratings

| | |
|-------------------------------|--------------------------------|
| Supply Voltage | 5.5 V |
| Logic Inputs | GND -0.5 V to $V_{DD} + 0.5$ V |
| Ambient Operating Temperature | 0°C to +70°C |
| Case Temperature | 115°C |
| Storage Temperature | -65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = 3.3$ V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|--------------------|--|----------------|--------|----------------|-------|
| Input High Voltage | V_{IH} | | 2 | | $V_{DD} + 0.3$ | V |
| Input Low Voltage | V_{IL} | | $V_{SS} - 0.3$ | | 0.8 | V |
| Input High Current | I_{IH} | $V_{IN} = V_{DD}$ | -5 | | 5 | mA |
| Input Low Current | I_{IL1} | $V_{IN} = 0$ V; Inputs with no pull-up resistors | -5 | | | mA |
| | I_{IL2} | $V_{IN} = 0$ V; Inputs with pull-up resistors | -200 | | | |
| Operating Supply Current | $I_{DD3.3OP}$ | $C_L = \text{Full load}$ | 229 | 221 | 360 | mA |
| Powerdown Current | $I_{DD3.3PD}$ | IREF=2.32 mA | | 21 | 25 | mA |
| Input Frequency | F_i | $V_{DD} = 3.3$ V | | 14.318 | | MHz |
| Pin Inductance | L_{pin} | | | | 7 | nH |
| Input Capacitance ¹ | C_{IN} | Logic Inputs | | | 5 | pF |
| | C_{OUT} | Output pin capacitance | | | 6 | pF |
| | C_{INX} | X1 & X2 pins | 27 | | 45 | pF |
| Transition time ¹ | T_{trans} | To 1st crossing of target frequency | | | 3 | ms |
| Settling time ¹ | T_s | From 1st crossing to 1% target frequency | | | 3 | ms |
| Clk Stabilization ¹ | T_{STAB} | From $V_{DD} = 3.3$ V to 1% target frequency | | | 3 | ms |
| Delay ¹ | t_{PZH}, t_{PZL} | Output enable delay (all outputs) | 1 | | 10 | ns |
| | t_{PHZ}, t_{PLZ} | Output disable delay (all outputs) | 1 | | 10 | ns |
| 3V66 to PCI | $S_{3V66-PCI}$ | 3V66 (5:0) leads 33MHz PCI | 1.5 | 2.12 | 3.5 | ns |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 2\text{pF}$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------------|-----------------------|--|--------|-----|---------|----------|-------|
| Current Source Output Impedance | Z_o^1 | $V_o = V_x$ | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | 770 | 850 | mV | 1 |
| Voltage Low | VLow | | -150 | 5 | 150 | | 1 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | 756 | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | -7 | | | 1 |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | 350 | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | 12 | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Average period | Tperiod | 200MHz nominal | 4.9985 | | 5.0015 | ns | 2 |
| | | 200MHz spread | 4.9985 | | 5.0266 | ns | 2 |
| | | 166.66MHz nominal | 5.9982 | | 6.0018 | ns | 2 |
| | | 166.66MHz spread | 5.9982 | | 6.0320 | ns | 2 |
| | | 133.33MHz nominal | 7.4978 | | 7.5023 | ns | 2 |
| | | 133.33MHz spread | 7.4978 | | 5.4000 | ns | 2 |
| | | 100.00MHz nominal | 9.9970 | | 10.0030 | ns | 2 |
| | | 100.00MHz spread | 9.9970 | | 10.0533 | ns | 2 |
| Absolute min period | T_{absmin} | 200MHz nominal | 4.8735 | | | ns | 1,2 |
| | | 166.66MHz nominal/spread | 5.8732 | | | ns | 1,2 |
| | | 133.33MHz nominal/spread | 7.3728 | | | ns | 1,2 |
| | | 100.00MHz nominal/spread | 9.8720 | | | ns | 1,2 |
| Rise Time | t_r | $V_{OL} = 0.175\text{V}$, $V_{OH} = 0.525\text{V}$ | 175 | 332 | 700 | ps | 1 |
| Fall Time | t_f | $V_{OH} = 0.525\text{V}$ $V_{OL} = 0.175\text{V}$ | 175 | 344 | 700 | ps | 1 |
| Rise Time Variation | d- t_r | | | 30 | 125 | ps | 1 |
| Fall Time Variation | d- t_f | | | 30 | 125 | ps | 1 |
| Duty Cycle | d_{t3} | Measurement from differential waveform | 45 | 49 | 55 | % | 1 |
| Skew | t_{sk3} | $V_T = 50\%$ | | 8 | 150 | ps | 1 |
| Jitter, Cycle to cycle | $t_{j\text{cyc-cyc}}$ | Measurement from differential waveform | | 60 | 150 | ps | 1 |

¹Guaranteed by design, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------|------------------------------------|---|-----|-------|------|-------|
| Output Frequency | F _{O1} | | | 33.33 | | MHz |
| Output Impedance | R _{DSP1} ¹ | V _O = V _{DD} *(0.5) | 12 | | 55 | Ω |
| Output High Voltage | V _{OH} ¹ | I _{OH} = -1 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} ¹ | I _{OL} = 1 mA | | | 0.55 | V |
| Output High Current | I _{OH} ¹ | V _{OH@MIN} = 1.0 V, V _{OH@MAX} = 3.135 V | -33 | | -33 | mA |
| Output Low Current | I _{OL} ¹ | V _{OL@MIN} = 1.95 V, V _{OL@MAX} = 0.4 V | 30 | | 38 | mA |
| Rise Time | t _{r1} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 0.5 | 188 | 2 | ns |
| Fall Time | t _{f1} ¹ | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 0.5 | 1.79 | 2 | ns |
| Duty Cycle | d _{t1} ¹ | V _T = 1.5 V | 45 | 52 | 55 | % |
| Skew | t _{sk1} ¹ | V _T = 1.5 V | | 280 | 500 | ps |
| Jitter, cycle to cyc | t _{jcvc-cyc} ¹ | V _T = 1.5 V | | 200 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|------------------------------------|---|-----|------|------|-------|
| Output Frequency | F _{O1} | | | | | MHz |
| Output Impedance | R _{DSP1} ¹ | V _O = V _{DD} *(0.5) | 12 | 33 | 55 | Ω |
| Output High Voltage | V _{OH} ¹ | I _{OH} = -1 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} ¹ | I _{OL} = 1 mA | | | 0.55 | V |
| Output High Current | I _{OH} ¹ | V _{OH@MIN} = 1.0 V, V _{OH@MAX} = 3.135 V | -33 | | -33 | mA |
| Output Low Current | I _{OL} ¹ | V _{OL@MIN} = 1.95 V, V _{OL@MAX} = 0.4 V | 30 | | 38 | mA |
| Rise Time | t _{r1} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 0.5 | 1.55 | 2 | ns |
| Fall Time | t _{f1} ¹ | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 0.5 | 1.32 | 2 | ns |
| Duty Cycle | d _{t1} ¹ | V _T = 1.5 V | 45 | 51.7 | 55 | % |
| Skew | t _{sk1} ¹ | V _T = 1.5 V | | 16 | 250 | ps |
| Jitter | t _{jcvc-cyc} ¹ | V _T = 1.5 V | | 200 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.

Note: 3V66@66Mhz- main PLL

Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10\text{-}20\text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------|-----------------|---|-----|------|------|----------|
| Output Frequency | F_{O1} | $V_O = V_{DD}^*(0.5)$ | | 48 | | MHz |
| Output Impedance | R_{DSP1}^1 | $V_O = V_{DD}^*(0.5)$ | 12 | | 55 | Ω |
| Output High Voltage | V_{OH}^1 | $I_{OH} = -1\text{ mA}$ | 2.4 | 3.1 | | V |
| Output Low Voltage | V_{OL}^1 | $I_{OL} = 1\text{ mA}$ | | 0.19 | 0.55 | V |
| Output High Current | I_{OH}^1 | $V_{OH@MIN} = 1.0\text{ V}$, $V_{OH@MAX} = 3.135\text{ V}$ | -29 | | -23 | mA |
| Output Low Current | I_{OL}^1 | $V_{OL@MIN} = 1.95\text{ V}$, $V_{OL@MAX} = 0.4\text{ V}$ | 29 | | 27 | mA |
| 48DOT Rise Time | t_{r1}^1 | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | 0.5 | 0.77 | 1 | ns |
| 48DOT Fall Time | t_{f1}^1 | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 0.5 | 0.84 | 1 | ns |
| VCH 48 USB Rise Time | t_{r1}^1 | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | 1 | 1.12 | 2 | ns |
| VCH 48 USB Fall Time | t_{f1}^1 | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 1 | 1.42 | 2 | ns |
| 48DOT Duty Cycle | d_{t1}^1 | $V_T = 1.5\text{ V}$ | 45 | 49.9 | 55 | % |
| 48 USB Duty Cycle | d_{t1}^1 | $V_T = 1.5\text{ V}$ | 45 | 54.9 | 55 | % |
| Jitter | $t_{jvc-cvc}^1$ | $V_T = 1.5\text{ V}$ | | 131 | 350 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10\text{-}20\text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|-----------------|---|-----|-------|------|----------|
| Output Frequency | F_{O1} | | | 14.31 | | MHz |
| Output Impedance | R_{DSP1}^1 | $V_O = V_{DD}^*(0.5)$ | 20 | | 60 | Ω |
| Output High Voltage | V_{OH}^1 | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL}^1 | $I_{OL} = 1\text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH}^1 | $V_{OH@MIN} = 1.0\text{ V}$, $V_{OH@MAX} = 3.135\text{ V}$ | -29 | | -23 | mA |
| Output Low Current | I_{OL}^1 | $V_{OL@MIN} = 1.95\text{ V}$, $V_{OL@MAX} = 0.4\text{ V}$ | 29 | | 27 | mA |
| Rise Time | t_{r1}^1 | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | 1 | 1.7 | 2 | ns |
| Fall Time | t_{f1}^1 | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 1 | 1.76 | 2 | ns |
| Duty Cycle | d_{t1}^1 | $V_T = 1.5\text{ V}$ | 45 | 53.5 | 55 | % |
| Jitter | $t_{jvc-cvc}^1$ | $V_T = 1.5\text{ V}$ | | 305 | 1000 | ps |

¹Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kiloohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

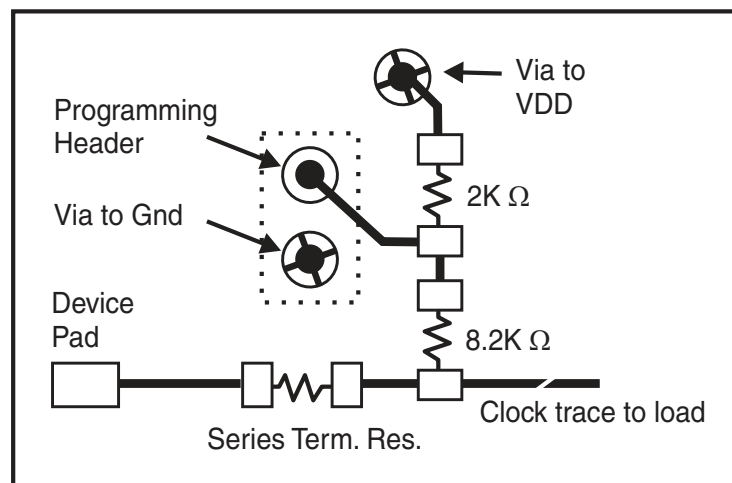
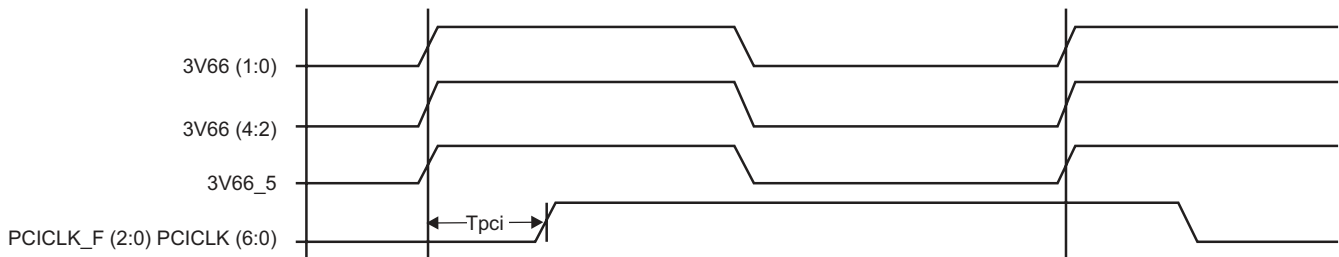


Fig. 1

3V66 & PCI Phase Relationship

All 3V66 clocks are to be in pphase with each other. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1/VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.



Group Skews at Common Transition Edges

| GROUP | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------|-----------------------|---|-----|-----|-----|-------|
| 3V66 | 3V66 | 3V66 (5:0) pin to pin skew | 0 | | 500 | ps |
| PCI | PCI | PCI_F (2:0) and PCI (6:0) pin to pin skew | 0 | | 500 | ps |
| 3V66 to PCI | S _{3V66-PCI} | 3V66 (5:0) leads 33MHz PCI | 1.5 | | 3.5 | ns |

¹Guaranteed by design, not 100% tested in production.

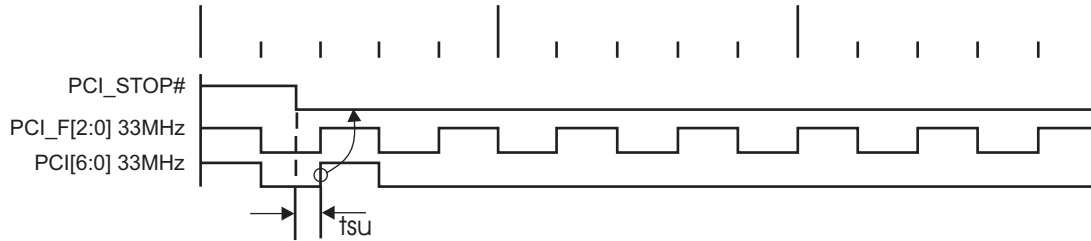
PD# Functionality

| CPU_STOP# | CPUT | CPUC | 3V66 | 66MHz_OUT | PCICLK_F PCICLK | PCICLK | USB/DOT 48MHz |
|-----------|-------------|--------|-------|-----------|--------------------|----------|------------------|
| 1 | Normal | Normal | 66MHz | 66MHz_IN | 66MHz_IN | 66MHz_IN | 48MHz |
| 0 | iref * Mult | Float | Low | Low | Low | Low | Low |

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI[6:0] and stoppable PCI_F[2,0] clocks will latch low in their next high to low transition. The PCI_STOP# setup time t_{su} is 10 ns, for transitions to be recognized by the next rising edge.

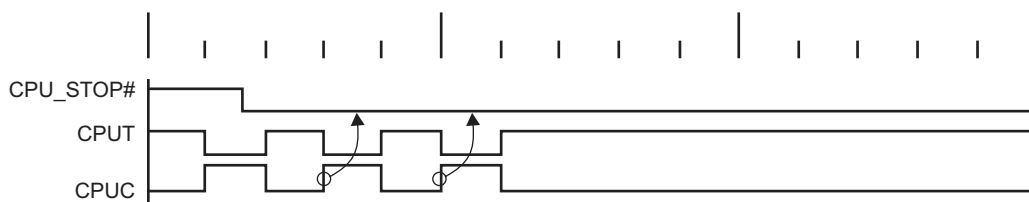
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

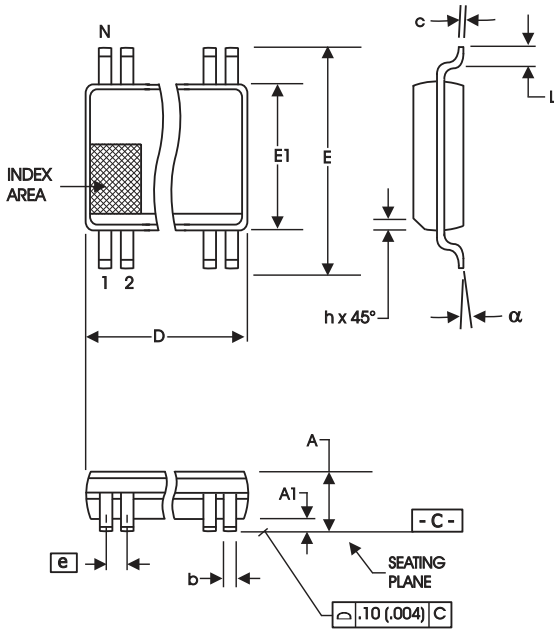
The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I²C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition following the two CPU clock edge sampling as shown. The final state of the stopped CPU signals is CPUT=High and CPUC=Low. There is to be no change to the output drive current values. The CPUT will be driven high with a current value equal to (MULTSEL0) X (I REF), the CPUC signal will not be driven.

Assertion of CPU_STOP# Waveforms



CPU_STOP# Functionality

| CPU_STOP# | CPUT | CPUC |
|-----------|-------------|--------|
| 1 | Normal | Normal |
| 0 | iref * Mult | Float |



300 mil SSOP Package

| SYMBOL | In Millimeters | | In Inches | |
|--------|-------------------|-------|-------------------|-------|
| | COMMON DIMENSIONS | | COMMON DIMENSIONS | |
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| alpha | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 48 | 15.75 | 16.00 | .620 | .630 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950220yFLFT

Example:

ICS XXXX y F LF - T



Revision History

| Rev. | Issue Date | Description | Page # |
|-------------|-------------------|---|---------------|
| F | 7/28/2005 | Added LF Ordering Information. | 19 |
| G | 3/2/2007 | Updated Electrical Characteristics CPU Skew spec. | 13 |
| | | | |
| | | | |
| | | | |

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.