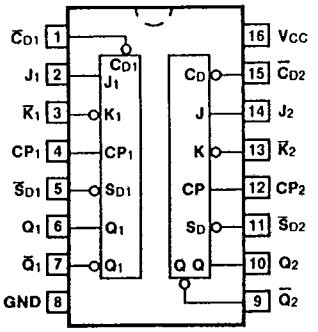
54S/74S109
54LS/74LS109

DUAL JK̄ POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '109 consists of two high speed, completely independent transition clocked JK̄ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK̄ design allows operation as a D flip-flop (refer to '74 data sheet) by connecting the J and K̄ inputs together. The '109 is functionally equivalent to the 9024.

CONNECTION DIAGRAM
PINOUT A



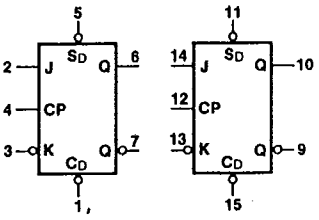
TRUTH TABLE

INPUTS		OUTPUTS
@ t_n		@ t_{n+1}
J	K	Q Q
L	H	No Change
L	L	L H
H	H	H L
H	L	Toggles

Asynchronous Inputs:
LOW input to S̄D sets Q to HIGH level
LOW input to C̄D sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on C̄D and S̄D makes both Q and Q̄ HIGH

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S109PC, 74LS109PC		9A
Ceramic DIP (D)	A	74S109DC, 74LS109DC	54S109DM, 54LS109DM	6A
Flatpak (F)	A	74S109FC, 74LS109FC	54S109FM, 54LS109FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J1, J2, K̄1, K̄2	Data Inputs	1.25/1.25	0.5/0.25
CP1, CP2	Clock Pulse Inputs (Active Rising Edge)	2.5/2.5	1.0/0.5
C̄D1, C̄D2	Direct Clear Inputs (Active LOW)	5.0/5.0	1.0/1.0
S̄D1, S̄D2	Direct Set Inputs (Active LOW)	2.5/2.5	1.0/0.5
Q1, Q2, Q̄1, Q̄2	Outputs	25/12.5	10/5.0 (2.5)

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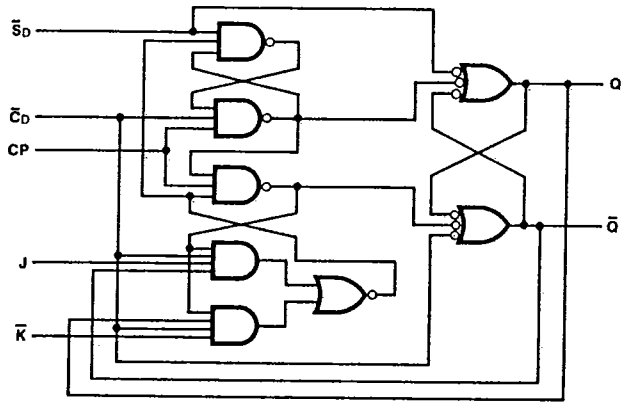
LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		52		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	75		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$		9.0 11		25 35	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		6.0 12		15 35	ns	$V_{CP} \geq 2.0$ V Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		6.0 12		15 24	ns	$V_{CP} \leq 0.8$ V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time J_n or $\overline{K}_n$ to CP_n	6.0 6.0		18 18		ns	Fig.3-6
t_h (H) t_h (L)	Hold Time J_n or $\overline{K}_n$ to CP_n	0 0		0 0		ns	
t_w (H) t_w (L)	CP_n Pulse Width	7.0 6.5		20 13.5		ns	Fig. 3-8
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	6.0		15		ns	Fig. 3-10