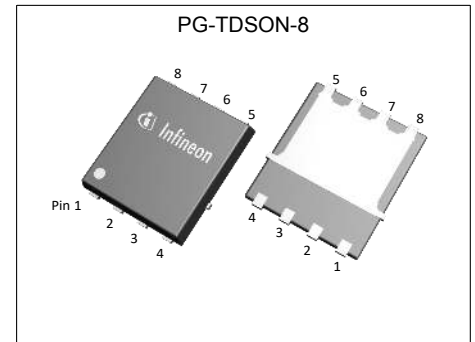


# MOSFET

## OptiMOS™3 Power-Transistor, 300 V

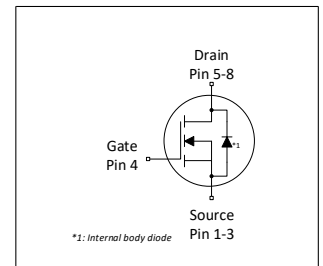
### Features

- N-channel, normal level
- 175 °C rated
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target application
- Halogen-free according to IEC61249-2-21
- Ideal for high-frequency switching and synchronous rectification



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	300	V
$R_{DS(on),max}$	130	m $\Omega$
$I_D$	16	A



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSC13DN30NSFD	PG-TDSON-8	13DN30NF	-

<sup>1)</sup> J-STD20 and JESD22

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	16 14	A	$T_C=25\text{ °C}$ $T_C=100\text{ °C}$
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	-	-	64	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	56	mJ	$I_D=14.4\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Reverse diode peak $dv/dt$	$dv/dt$	-	-	60	kV/ $\mu$ s	$I_D=36\text{ A}$ , $V_{DS}=150\text{ V}$ , $di/dt=1000\text{ A}/\mu\text{s}$ , $T_{j,max}=175\text{ °C}$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	150	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	-

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	0.6	1	K/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	75	K/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thJA}$	-	-	50	K/W	-

## 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	300	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS}=V_{GS}$ , $I_D=90\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=240\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=240\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	1	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	114	130	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=16\text{ A}$
Gate resistance	$R_G$	-	3.3	5	$\Omega$	-
Transconductance	$g_{fs}$	19	38	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=16\text{ A}$

<sup>1)</sup> See Diagram 3

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu$ m thick) copper area for drain connection. PCB is vertical in still air.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1840	2450	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=150\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	76	102	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=150\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	5.4	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=150\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	8.0	-	ns	$V_{DD}=150\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=8\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Rise time	$t_r$	-	4.0	-	ns	$V_{DD}=150\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=8\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	19	-	ns	$V_{DD}=150\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=8\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Fall time	$t_f$	-	4.0	-	ns	$V_{DD}=150\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=8\text{ A}$ , $R_{G,ext}=1.6\ \Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	8.0	-	nC	$V_{DD}=150\text{ V}$ , $I_D=16\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	2.9	-	nC	$V_{DD}=150\text{ V}$ , $I_D=16\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	5.4	-	nC	$V_{DD}=150\text{ V}$ , $I_D=16\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	23	30	nC	$V_{DD}=150\text{ V}$ , $I_D=16\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DD}=150\text{ V}$ , $I_D=16\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge	$Q_{oss}$	-	48	-	nC	$V_{DD}=150\text{ V}$ , $V_{GS}=0\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	16	A	$T_C=25\text{ °C}$
Diode pulse current <sup>3)</sup>	$I_{S,pulse}$	-	-	64	A	$T_C=25\text{ °C}$
Diode hard commutation current <sup>4)</sup>	$I_{S,hard}$	-	-	16	A	$T_C=25\text{ °C}$ , $di_F/dt=1000\text{ A}/\mu\text{s}$
Diode forward voltage	$V_{SD}$	-	0.9	1.2	V	$V_{GS}=0\text{ V}$ , $I_F=16\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	111	222	ns	$V_R=150\text{ V}$ , $I_F=12.6\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	249	498	nC	$V_R=150\text{ V}$ , $I_F=12.6\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

<sup>3)</sup> Diode pulse current is defined by thermal and/or package limits

<sup>4)</sup> Maximum allowed hard-commutated current through diode at  $di/dt=1000\text{ A}/\mu\text{s}$

### 4 Electrical characteristics diagrams

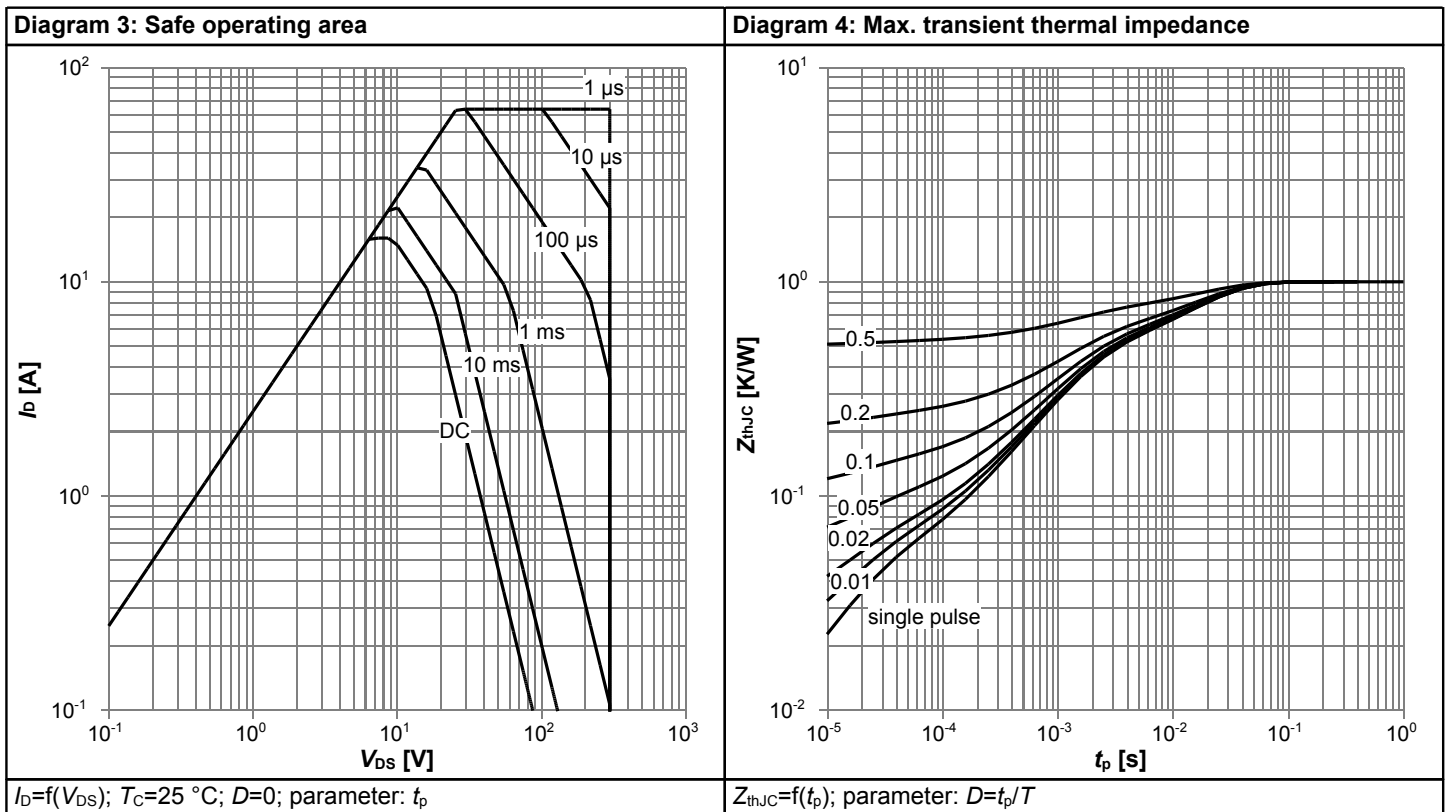
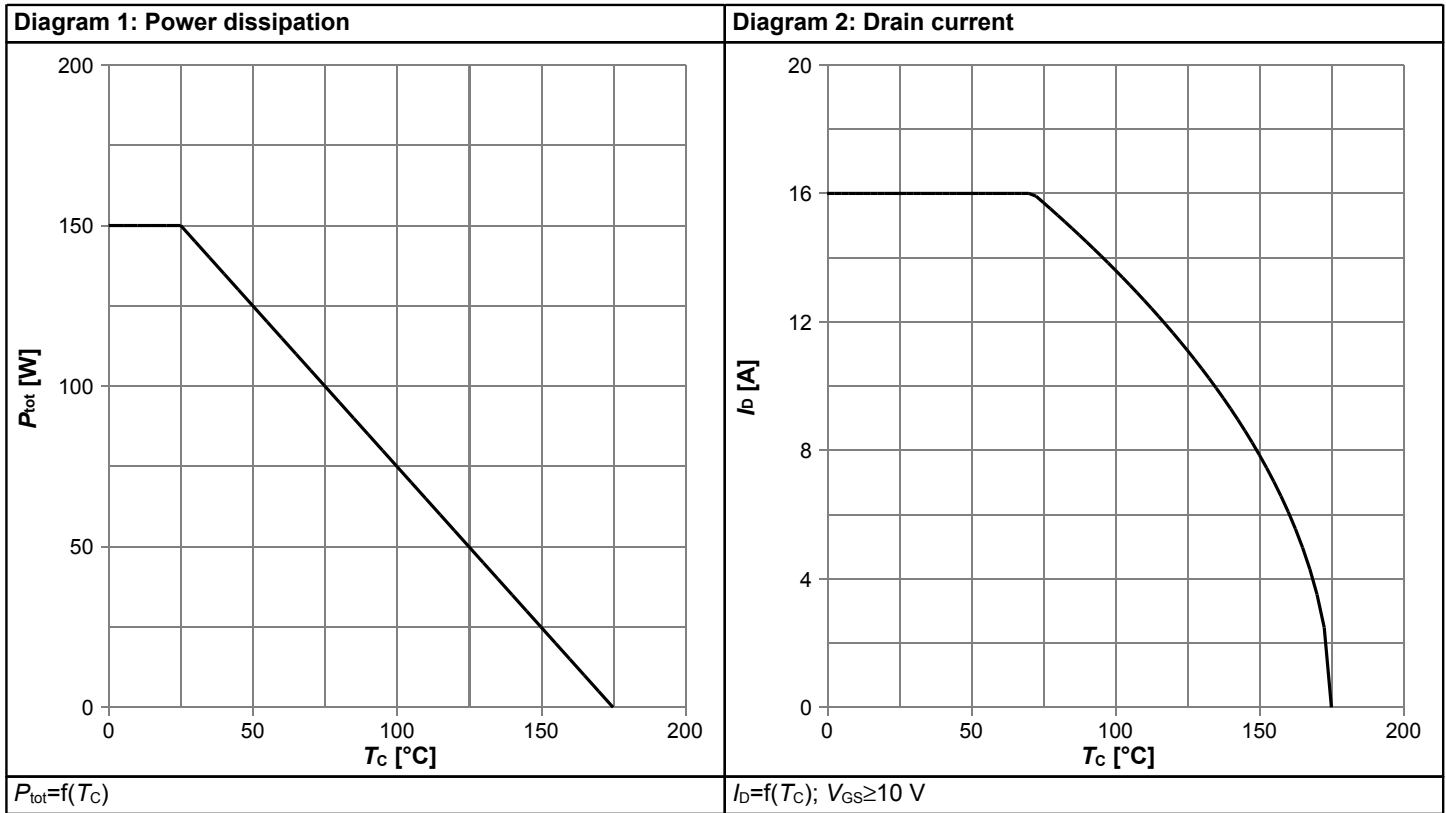
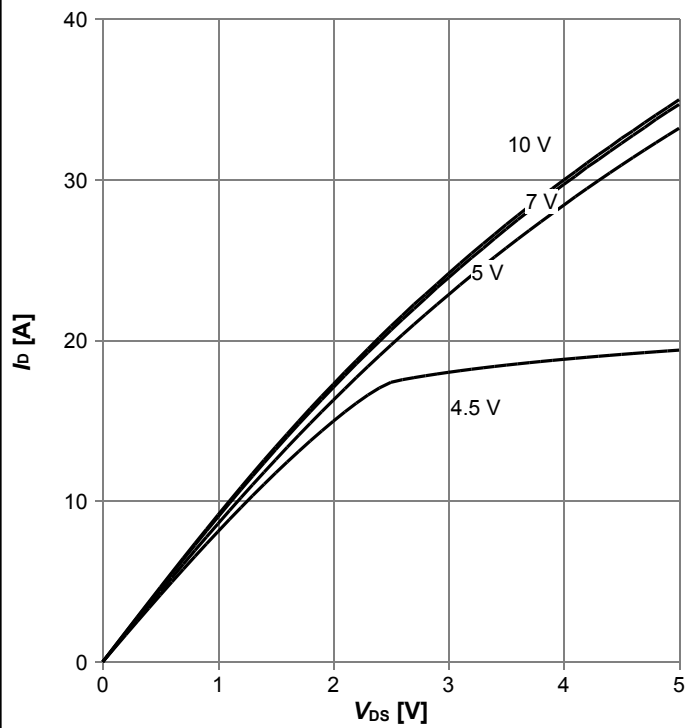
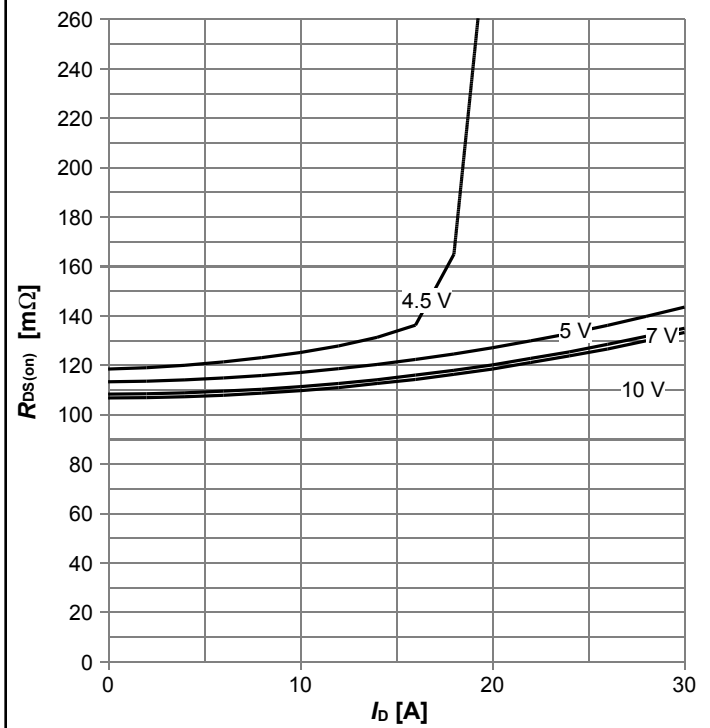


Diagram 5: Typ. output characteristics



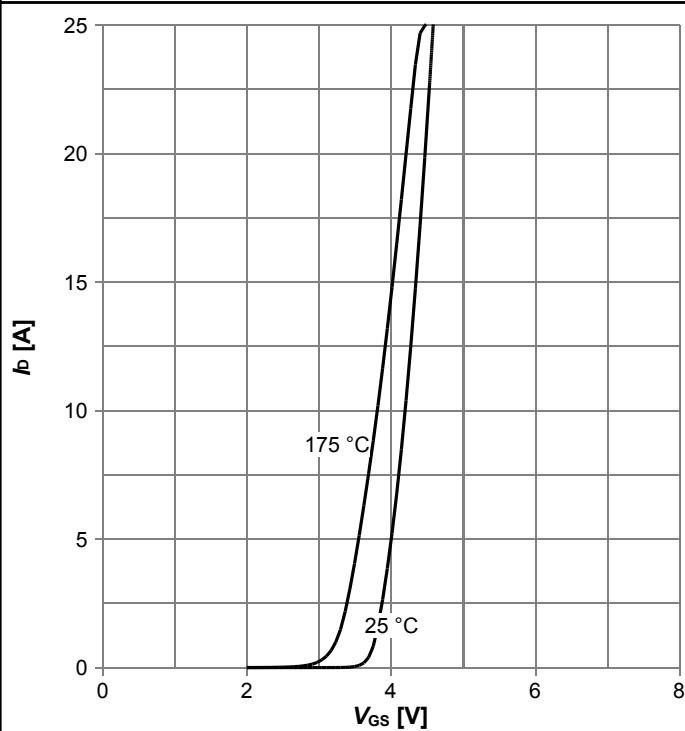
$I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance



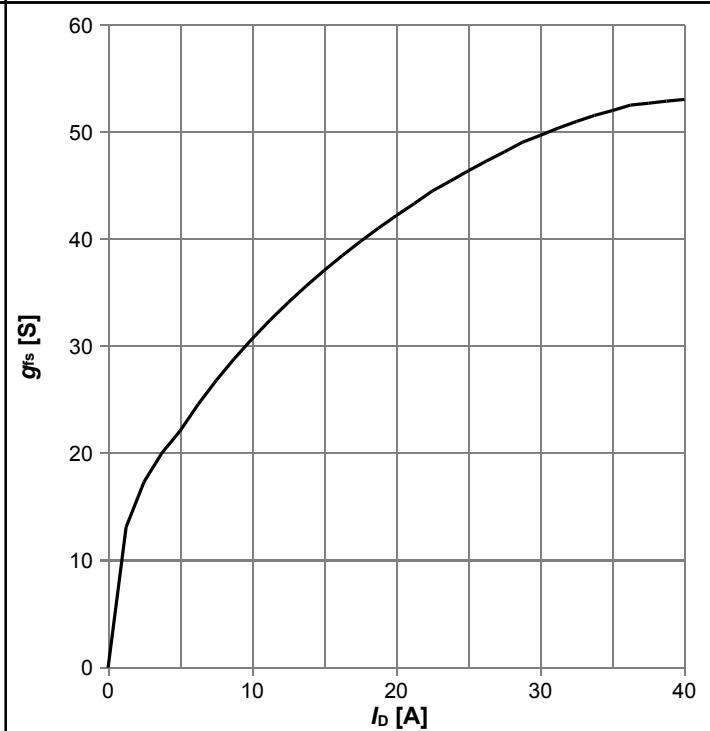
$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



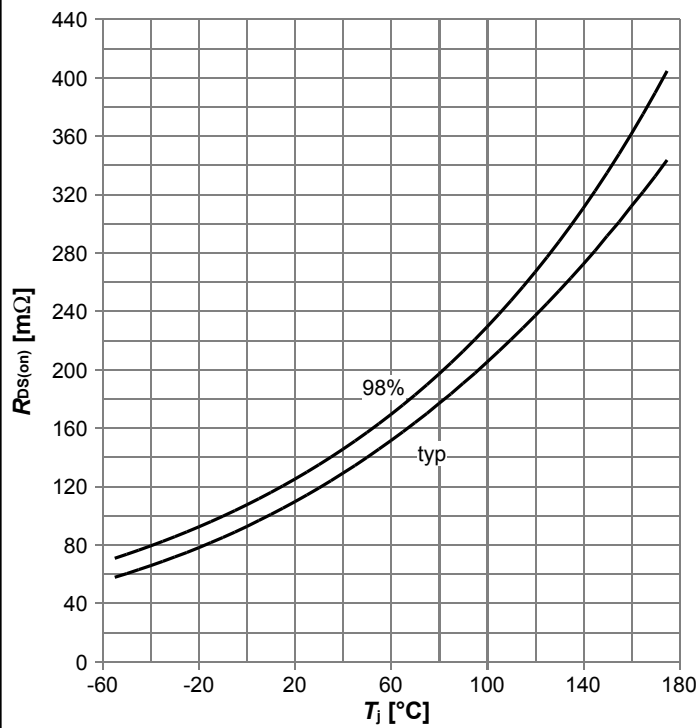
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$

Diagram 8: Typ. forward transconductance



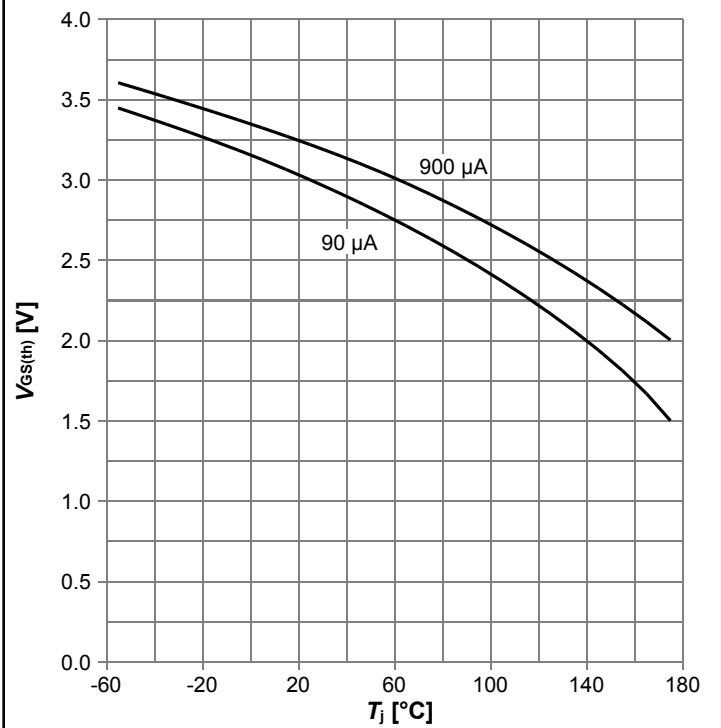
$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



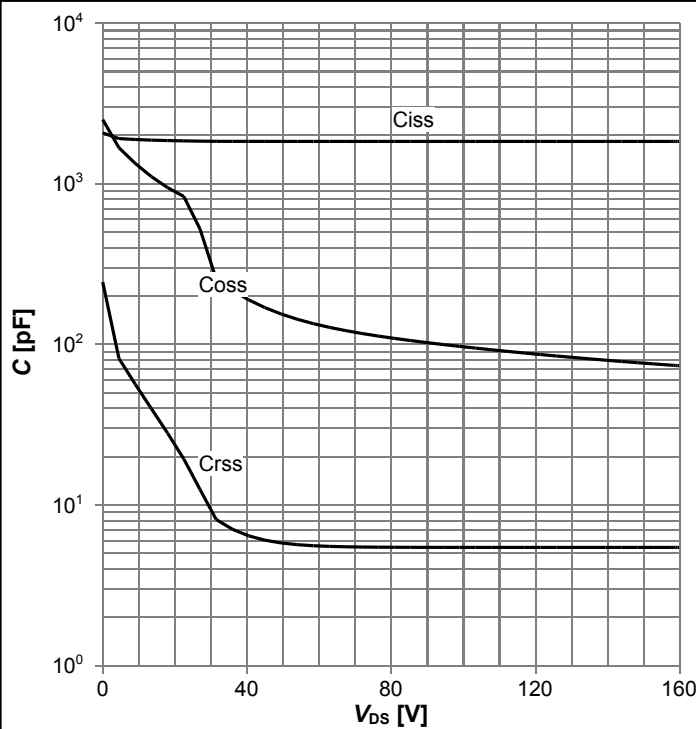
$R_{DS(on)}=f(T_j)$ ;  $I_D=16\text{ A}$ ;  $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



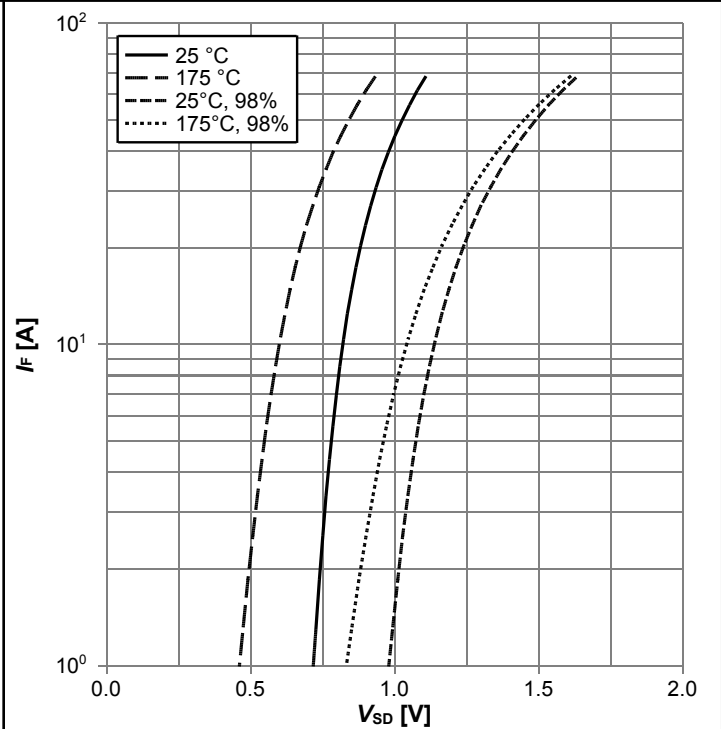
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



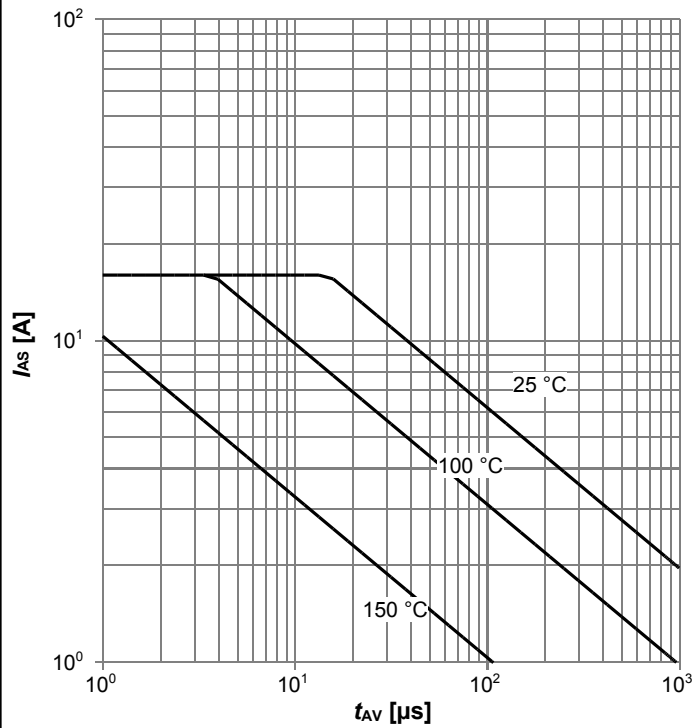
$C=f(V_{DS})$ ;  $V_{GS}=0\text{ V}$ ;  $f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



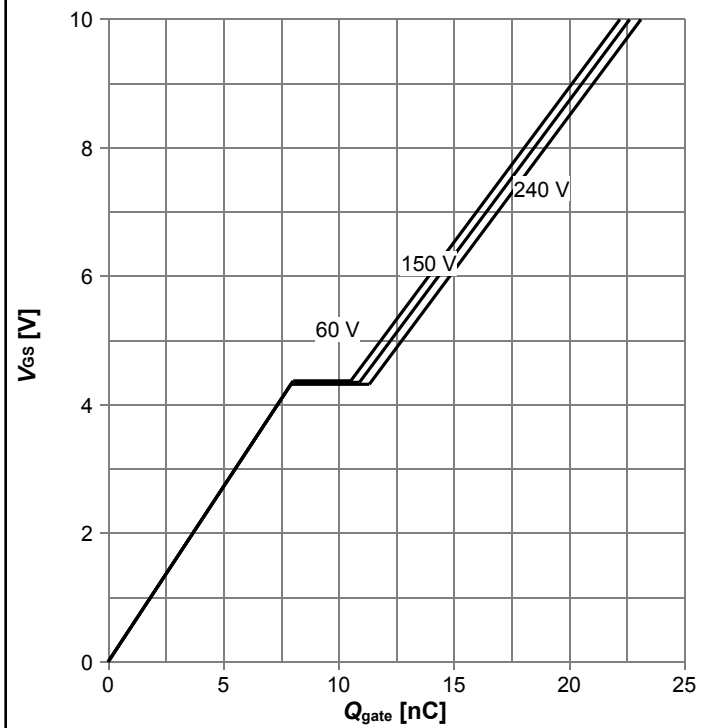
$I_F=f(V_{SD})$ ; parameter:  $T_j$

**Diagram 13: Avalanche characteristics**



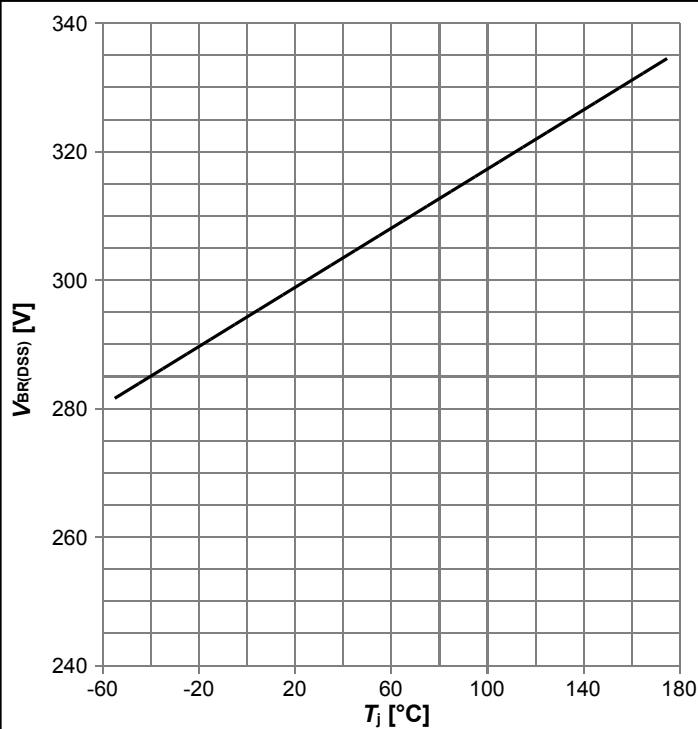
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

**Diagram 14: Typ. gate charge**



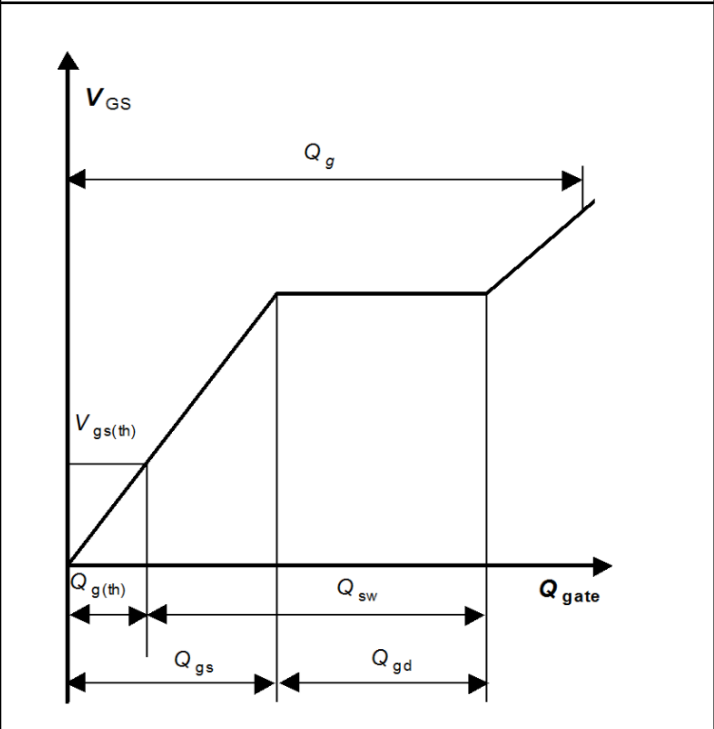
$V_{GS}=f(Q_{gate}); I_D=16 \text{ A pulsed}$ ; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**



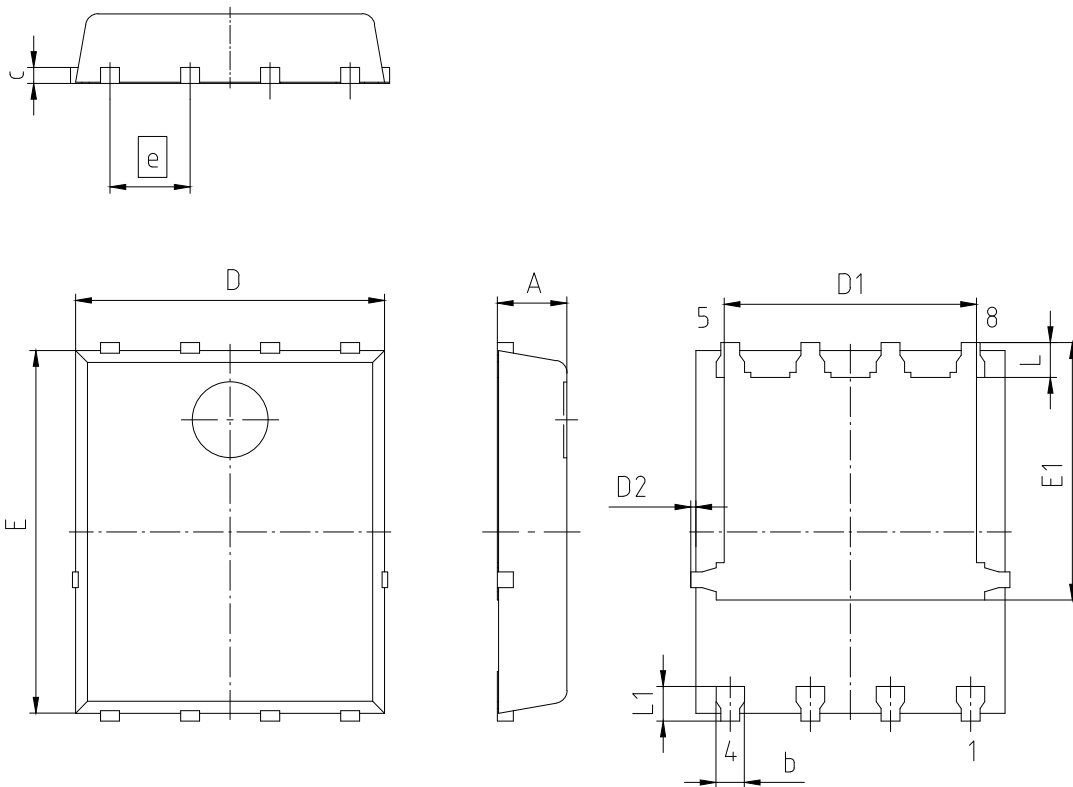
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Diagram Gate charge waveforms**





## 5 Package Outlines



PACKAGE - GROUP NUMBER: <b>PG-TDSON-8-U08</b>		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
<b>A</b>	0.90	1.20
<b>b</b>	0.34	0.54
<b>c</b>	0.15	0.35
<b>D</b>	4.80	5.35
<b>D1</b>	3.90	4.40
<b>D2</b>	0.00	0.22
<b>E</b>	5.70	6.10
<b>E1</b>	4.05	4.25
<b>e</b>	1.27	
<b>L</b>	0.45	0.65
<b>L1</b>	0.45	0.65

- 1) EXCLUDING MOLD FLASH
- 2) REMOVAL ON MOLD GATE  
INTRUSION 0.1 MM  
PROTRUSION 0.1 MM
- 3) ALL METAL SURFACES ARE PLATED,  
EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

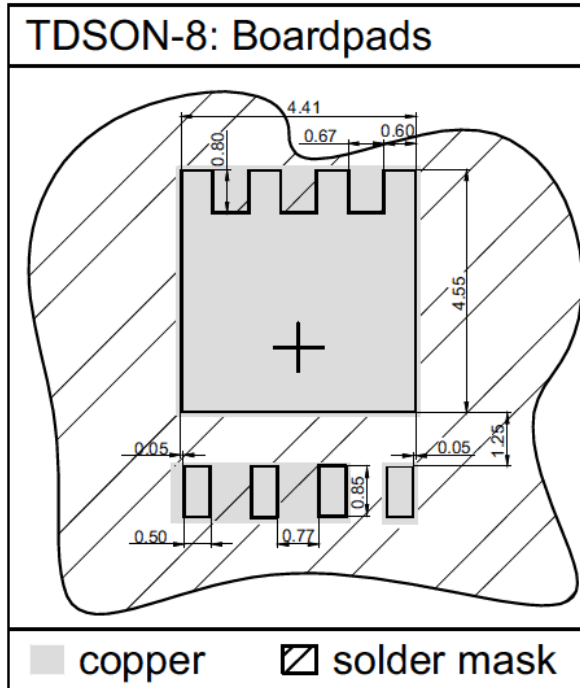


Figure 2 Outline Footprint (TDSO-8)

## Revision History

BSC13DN30NSFD

**Revision: 2022-11-09, Rev. 2.2**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-10-21	Release of final version
2.1	2016-12-05	Update Eas
2.2	2022-11-09	Update package outline drawing and footnotes

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