VSP5324-Q1 4-Channel, 12-Bit, 80-MSPS ADC

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 2: –40°C to +105°C
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Designed for Low Power:
  - One-Lane Interface: 65 mW per Channel at 50 MSPS
  - Two-Lane Interface: 82 mW per Channel at 80 MSPS
- Dynamic Performance:
  - 5-MHz Input Frequency, 80 MSPS
  - SNR: 70 dBFS
  - SFDR: 85 dBc
- Serial LVDS ADC Data Outputs
- Variety of LVDS Test Patterns to Verify Data Capture
- Package: 9-mm × 9-mm VQFN-64
- Operating Temperature: –40°C to +105°C

2 Applications

- Depth Sensing:
  - Location and Proximity Sensing
  - 3D Scanning
  - 3D Machine Vision
  - Security and Surveillance
  - Gesture Controls

3 Description

The VSP5324-Q1 device is a low-power, 12-bit, 80-MSPS, quad-channel, analog-to-digital converter (ADC). Low-power consumption and multiple-channel integration in a compact package makes the device attractive for 3D time-of-flight (ToF) systems.

Serial low-voltage differential signaling (LVDS) outputs reduce the number of interface lines and enable high system integration.

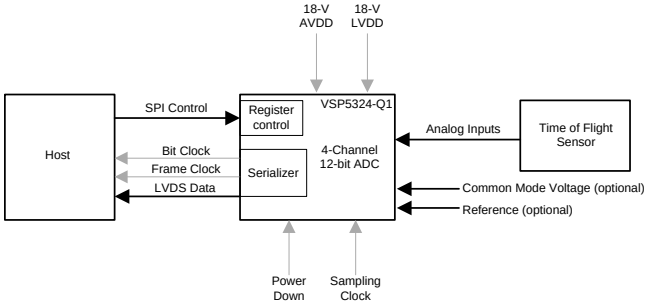
The device is available in a compact 9-mm × 9-mm VQFN-64 Package.

Device Information(1)

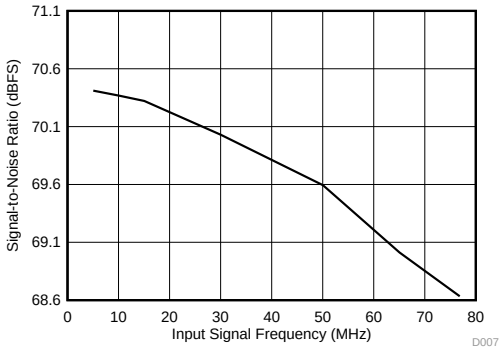
PART NUMBER	PACKAGE	BODY SIZE (NOM)
VSP5324-Q1	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Signal-to-Noise Ratio vs Input Signal Frequency



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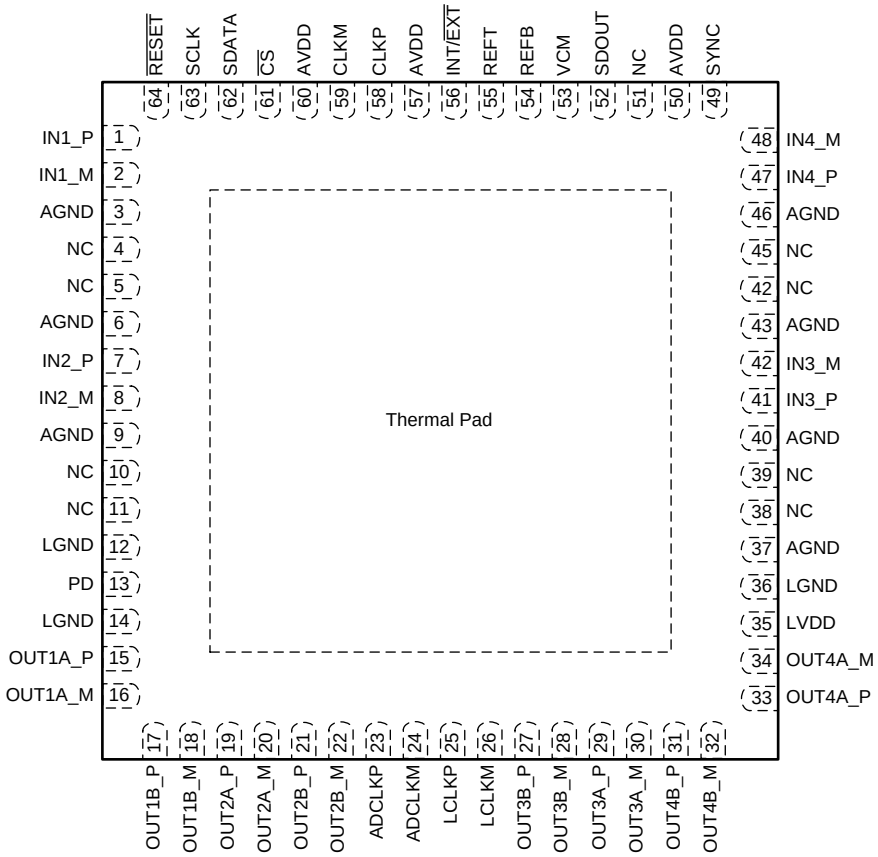
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2014) to Revision A	Page
• Changed device visibility from custom to catalog	1
• Added *Receiving Notification of Documentation Updates* and *Community Resources*	57

5 Pin Configuration and Functions

RGC Package
64-Pin VQFN With Exposed Thermal Pad
Top View



NC - No internal connection

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADCLKM	24	Digital output	Negative LVDS differential frame clock output pin
ADCLKP	23	Digital output	Positive LVDS differential frame clock output pin
AGND	3	Ground	Analog ground pin
	6		
	9		
	37		
	40		
	43		
	46		
AVDD	50	Supply	Analog supply pin, 1.8 V
	57		
	60		
CLKM	59	Analog input	Negative clock input Differential clock input: apply differential clocks (sine wave, LVPECL, and LVDS) to CLKP and CLKM. Single-ended clock input: apply a CMOS clock to CLKP and tie CLKM to ground.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
CLKP	58	Analog input	Positive clock input Differential clock input: apply differential clocks (sine wave, LVPECL, and LVDS) to CLKP and CLKM. Single-ended clock input: apply a CMOS clock to CLKP and tie CLKM to ground.
$\overline{CS}$	61	Digital input	Serial interface enable pin
IN1_M	2	Analog input	Channel 1 negative differential analog input
IN1_P	1	Analog input	Channel 1 positive differential analog input
IN2_M	8	Analog input	Channel 2 negative differential analog input
IN2_P	7	Analog input	Channel 2 positive differential analog input
IN3_M	42	Analog input	Channel 3 negative differential analog input
IN3_P	41	Analog input	Channel 3 positive differential analog input
IN4_M	48	Analog input	Channel 4 negative differential analog input
IN4_P	47	Analog input	Channel 4 positive differential analog input
INT/$\overline{EXT}$	56	Digital input	Internal and external reference control input pin Logic high: device uses internal reference Logic low: device uses external reference
LCLKM	26	Digital output	Negative LVDS differential bit clock output pin
LCLKP	25	Digital output	Positive LVDS differential bit clock output pin
LGND	12	Ground	Digital ground pin
	14		
	36		
LVDD	35	Supply	Digital and LVDS supply pin, 1.8 V
NC	4	—	Unused; do not connect
	5		
	10		
	11		
	38		
	39		
	44		
	45		
	51		
OUT1A_M	16	Interface	Channel 1A negative LVDS differential output pin. This pin can be used with either one- or two-lane interface.
OUT1A_P	15	Interface	Channel 1A positive LVDS differential output pin. This pin can be used with either one- or two-lane interface.
OUT1B_M	18	Interface	Channel 1B negative LVDS differential output pin. This pin is used with two-lane interface. In one-lane interface, this pin is unused and must be floated without a 100-Ω termination.
OUT1B_P	17	Interface	Channel 1B positive LVDS differential output pin. This pin is used with two-lane interface. In one-lane interface, this pin is unused and must be floated without a 100-Ω termination.
OUT2A_M	20	Interface	Channel 2A negative LVDS differential output pin. This pin can be used with either one- or two-lane interface.
OUT2A_P	19	Interface	Channel 2A positive LVDS differential output pin. This pin can be used with either one- or two-lane interface.
OUT2B_M	22	Interface	Channel 2B negative LVDS differential output pin. This pin is used with two-lane interface. In one-lane interface, this pin is unused and must be floated without a 100-Ω termination.
OUT2B_P	21	Interface	Channel 2B positive LVDS differential output pin. This pin is used with two-lane interface. In one-lane interface, this pin is unused and must be floated without a 100-Ω termination.
OUT3A_M	30	Interface	Channel 3A negative LVDS differential output pin. This pin can be used with either one- or two-lane interface.
OUT3A_P	29	Interface	Channel 3A positive LVDS differential output pin. This pin can be used with either one- or two-lane interface.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUT3B_M	28	Interface	Channel 3B negative LVDS differential output pin. This pin is used with two-lane interface. In one-lane interface, this pin is unused and must be floated without a 100-Ω termination.
OUT3B_P	27	Interface	Channel 3B positive LVDS differential output pin. This pin is used with two-lane interface. In one-lane interface, this pin is unused and must be floated without a 100-Ω termination.
OUT4A_M	34	Interface	Channel 4A negative LVDS differential output pin. This pin can be used with either one- or two-lane interface.
OUT4A_P	33	Interface	Channel 4A positive LVDS differential output pin. This pin can be used with either one- or two-lane interface.
OUT4B_M	32	Interface	Channel 4B negative LVDS differential output pin. This pin is used with two-lane interface. In one-lane interface, this pin is unused and must be floated without a 100-Ω termination.
OUT4B_P	31	Interface	Channel 4B positive LVDS differential output pin. This pin is used with two-lane interface. In one-lane interface, this pin is unused and must be floated without a 100-Ω termination.
PD	13	Digital input	Power-down control input pin Logic high: device is in power-down state; logic low: normal operation
REFB	54	Analog input	Reference bottom voltage pin Internal reference mode: the reference bottom voltage (0.45 V) is output on this pin. External reference mode: the reference bottom voltage (0.45 V) must be externally applied to this pin. There are no required decoupling capacitors on this pin.
REFT	55	Analog input	Reference top voltage pin Internal reference mode: the reference top voltage (1.45 V) is output on this pin. External reference mode: reference top voltage (1.45 V) must be externally applied to this pin. There are no required decoupling capacitors on this pin.
$\overline{\text{RESET}}$	64	Digital input	Serial interface reset pin; active low
SCLK	63	Digital input	Serial interface clock pin
SDATA	62	Digital input	Serial interface data pin
SDOUT	52	Digital output	Serial interface readout pin
SYNC	49	Digital input	Control input pin synchronizes test patterns across channels. When unused, this pin should be tied to ground.
VCM	53	Analog output	Common-mode voltage pin Internal reference mode: common-mode voltage output pin, 0.95 V. External reference mode: reference voltage must be externally applied to this pin.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Supply voltage	AVDD	–0.3	2.2	V
	LVDD	–0.3	2.2	V
Ground voltage differences	Between AGND and LGND	–0.3	0.3	V
Input voltage	Digital outputs	–0.3	lesser of 2.2 or (LVDD + 0.3)	V
	Digital inputs (CLKN, CLKP(2), $\overline{\text{RESET}}$, SCLK, SDATA, $\overline{\text{CS}}$, SYNC, PD, INT/$\overline{\text{EXT}}$)	–0.3	lesser of 2.2 or (LVDD + 0.3)	V
	Analog inputs	–0.3	lesser of 2.2 or (LVDD + 0.3)	V
Input current (all pins except supplies)		–10	10	mA
Ambient temperature, under bias, T_A		–40	105	°C
Junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP, CLKN is less than |0.3 V|). This setting prevents the ESD protection diodes at the clock input pins from turning on.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Other pins	±500	
			Corner pins (1, 16, 17, 32, 33, 48, 49, and 64)	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

			MIN	NOM	MAX	UNIT
$V_{(AVDD)}$	Analog supply voltage		1.7	1.8	1.9	V
$V_{(LVDD)}$	Digital supply voltage		1.7	1.8	1.9	V
V_{ID}	Differential input voltage			2		V_{PP}
V_{IC}	Input common-mode voltage			V_{IC} ± 50		mV
	Input clock sample rate	Two-lane LVDS interface	10		80	MSPS
		One-lane LVDS interface	10		50	MSPS
(V_{CLKP} – V_{CLKM})	Input clock amplitude differential	Sine wave, ac-coupled		1.5		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		3.3		V
	Duty cycle		35%	50%	65%	
C_{LOAD}	Maximum external capacitance from each output pin to DRGND			5		pF
R_{LOAD}	Differential resistance between LVDS output pairs (LVDS mode)			100		Ω
T_A	Operating free-air		–40		105	°C

6.4 Thermal Information

THERMAL METRIC[1]		VSP5324-Q1 RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	20.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: Dynamic Performance

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, sampling frequency = 80 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 105°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution				12	Bits
SNR	Signal-to-noise ratio	f_{IN} = 5 MHz	68	70		dBFS
		f_{IN} = 30 MHz		69.5		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 5 MHz		69.8		dBFS
		f_{IN} = 30 MHz		69.2		dBFS
SFDR	Spurious-free dynamic range	f_{IN} = 5 MHz	64	85		dBc
		f_{IN} = 30 MHz		82		dBc
THD	Total harmonic distortion	f_{IN} = 5 MHz	63	81.5		dBc
		f_{IN} = 30 MHz		78		dBc
HD2	Second-harmonic distortion	f_{IN} = 5 MHz	64	90		dBc
		f_{IN} = 30 MHz		86		dBc
HD3	Third-harmonic distortion	f_{IN} = 5 MHz	64	85		dBc
		f_{IN} = 30 MHz		82		dBc
	Worst spur (other than second and third harmonics)	f_{IN} = 5 MHz		91		dBc
		f_{IN} = 30 MHz		83		dBc
IMD	Two-tone intermodulation distortion	$f1$ = 8 MHz, $f2$ = 10 MHz, each tone at –7 dBFS		83		dBc
	Crosstalk (far channel)	10-MHz full-scale signal on aggressor channel; no input signal applied on victim channel		95		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1		Clock cycle
PSRR	AC power-supply rejection ratio	For 50-mV_{PP} signal on AVDD supply, up to 10 MHz, no signal applied to analog inputs		50		dB
ENOB	Effective number of bits	f_{IN} = 5 MHz		11.3		Bits
DNL	Differential nonlinearity	f_{IN} = 5 MHz	–0.8	±0.2	0.8	LSBs
INL	Integral nonlinearity	f_{IN} = 5 MHz		±0.3	1	LSBs

6.6 Electrical Characteristics: General

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, sampling frequency = 80 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 105°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INx_PUT							
V_{ID}	Differential input	Voltage range			2		V_{PP}
		Resistance, at dc			2		kΩ
		Capacitance, at dc			2.2		pF
	Analog input bandwidth				550		MHz
	Analog input common-mode current (per input pin)				1.6		µA/MSPS
V_{OC}	Common-mode output voltage				0.95		V
$I_{O(VCM)}$	VCM output current capability				5		mA
DC ACCURACY							
	Offset error				±5	±20	mV
EGREF	Gain error resulting from internal reference inaccuracy alone			–2		2	%FS
EGCHAN	Gain error of channel alone				0.5		%FS
POWER SUPPLY							
IAVDD	Analog supply current		80 MSPS		114	135	mA
			50 MSPS		86		mA
ILVDD	Output buffer supply current		Two-lane LVDS interface, 80 MSPS, 350-mV swing with 100-Ω external termination		69	85	mA
			One-lane LVDS interface, 50 MSPS, 350-mV swing with 100-Ω external termination		56		mA
	Analog power		80 MSPS		205		mW
			50 MSPS		155		mW
	Digital power LVDS interface		Two-lane LVDS interface, 80 MSPS, 350-mV swing with 100-Ω external termination		124		mW
			One-lane LVDS interface, 50 MSPS, 350-mV swing with 100-Ω external termination		101		mW
	Total power		80 MSPS, two-lane LVDS interface		329		mW
			50 MSPS, one-lane LVDS interface		256		mW
	Global power-down					40	mW
	Standby power				135		mW

6.7 Electrical Characteristics: Digital

At $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, unless otherwise noted. The DC specifications refer to the condition where the digital outputs do not switch, but are tied permanently to a valid logic level 0 or 1.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INx_PUTS (RESET, SCLK, SDATA, CS, PDN, SYNC, INT/EXT)						
V_{IH}	High-level input voltage	All digital inputs support 1.8-V and 3.3-V CMOS logic levels	> 1.3			V
V_{IL}	Low-level input voltage	All digital inputs support 1.8-V and 3.3-V CMOS logic levels			< 0.4	V
I_{IH}	High-level input current	V_{IH} = 1.8 V		6		µA
I_{IL}	Low-level input current	V_{IL} = 0 V		< 0.1		µA
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage	CMOS interface (SDOUT)	AVDD – 0.1			V
V_{OL}	Low-level output voltage	CMOS interface (SDOUT)			0.1	V
$V_{OD(H)}$	High-level output differential voltage	LVDS interface (OUTP, OUTM, LCLKP, LCLKM, ADCLKP, ADCLKM), with an external 100-Ω termination	245		420	mV
$V_{OD(L)}$	Low-level output differential voltage	LVDS interface (OUTP, OUTM, LCLKP, LCLKM, ADCLKP, ADCLKM), with an external 100-Ω termination	–420		–245	mV
V_{OC}	Output common-mode voltage			1.05		V

6.8 Timing Requirements(1)

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, sampling frequency = 80 MSPS, sine wave input clock, $C_{(LOAD)}$ = 5 pF, and $R_{(LOAD)}$ = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 105°C, $V_{(AVDD)}$ = 1.8 V, and $V_{(LVDD)}$ = 1.7 V to 1.9 V.

			MIN	NOM	MAX	UNIT
	Aperture delay			4		ns
	Aperture delay matching(2)(3)	Between the two channels of the same device		±175		ps
	Aperture delay variation	Between two devices at the same temperature and LVDD supply		2.5		ns
	Aperture jitter (RMS)			320		fs
	Wakeup time	Time to valid data after coming out of partial power-down mode		5	50	µs
		Time to valid data after coming out of global power-down mode		100	500	µs
	ADC latency	One-lane LVDS output interface		11		Clock cycles
		Two-lane LVDS output interface		15		Clock cycles
t_{su}	Data setup time	Data valid to zero crossing of LCLKP, 80 MSPS, two-lane LVDS	0.61			ns
t_h	Data hold time(4)	Zero crossing of LCLKP to data becoming invalid, 80 MSPS, two-lane LVDS	0.74			ns
t_p	Clock propagation delay	Input clock rising edge crossover to frame clock rising edge crossover, two-lane LVDS for $10 \le f_S \le 80$ MSPS		$(11 / 12) \times t_S + t_d$		ns
		Input clock rising edge crossover to frame clock rising edge crossover, one-lane LVDS for $10 \le f_S \le 65$ MSPS		$(9 / 12) \times t_S + t_d$		ns
t_d	Delay time		6.8	9	11.8	ns

(1) Timing parameters are ensured by design and characterization and are not tested in production.
(2) $C_{(LOAD)}$ is the effective external single-ended load capacitance between each output pin and ground.
(3) $R_{(LOAD)}$ is the differential load resistance between the LVDS output pair.
(4) Data valid refers to a logic high of 100 mV and a logic low of –100 mV.

Timing Requirements[1] (continued)

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, sampling frequency = 80 MSPS, sine wave input clock, $C_{(LOAD)}$ = 5 pF, and $R_{(LOAD)}$ = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 105°C, $V_{(AVDD)}$ = 1.8 V, and $V_{(LVDD)}$ = 1.7 V to 1.9 V.

			MIN	NOM	MAX	UNIT
	LVDS bit clock duty cycle	Differential clock duty cycle (LCLKP – LCLKM)		50		%
t_f	Data fall time	Rise time measured from –100 mV to 100 mV, 10 MSPS ≤ sampling frequency ≤ 80 MSPS		0.2		ns
t_r	Data rise time	Rise time measured from –100 mV to 100 mV, 10 MSPS ≤ sampling frequency ≤ 80 MSPS		0.2		ns
$t_{r(CLK)}$	Output clock rise time	Rise time measured from –100 mV to 100 mV, 10 MSPS ≤ sampling frequency ≤ 80 MSPS		0.18		ns
$t_{f(CLK)}$	Output clock fall time	Rise time measured from –100 mV to 100 mV, 10 MSPS ≤ sampling frequency ≤ 80 MSPS		0.18		ns

6.9 LVDS Timing at Different Sampling Frequencies (One-Lane Interface, 12x Serialization)

See Figure 1 and Figure 2.

			MIN	MAX	UNIT
t_h	LCLKP zero-crossing to data becoming invalid (both edges)	$f_{(SAMPLE)}$ = 40 MSPS	0.75		ns
		$f_{(SAMPLE)}$ = 50 MSPS	0.47		
		$f_{(SAMPLE)}$ = 65 MSPS	0.25		
t_{su}	Data valid to LCLKP zero-crossing (both edges)	$f_{(SAMPLE)}$ = 40 MSPS	0.62		ns
		$f_{(SAMPLE)}$ = 50 MSPS	0.38		
		$f_{(SAMPLE)}$ = 65 MSPS	0.19		

6.10 LVDS Timing at Different Sampling Frequencies (Two-Lane Interface, 6x Serialization)

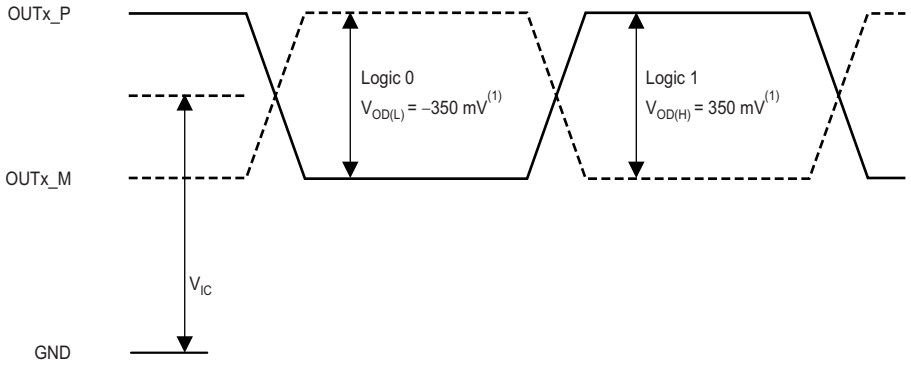
See Figure 1 and Figure 2.

			MIN	MAX	UNIT
t_h	LCLKP zero-crossing to data becoming invalid (both edges)	$f_{(SAMPLE)}$ = 40 MSPS	1.9		ns
		$f_{(SAMPLE)}$ = 50 MSPS	1.55		
		$f_{(SAMPLE)}$ = 65 MSPS	1.1		
t_{su}	Data valid to LCLKP zero-crossing (both edges)	$f_{(SAMPLE)}$ = 40 MSPS	1.44		ns
		$f_{(SAMPLE)}$ = 50 MSPS	1.02		
		$f_{(SAMPLE)}$ = 65 MSPS	0.64		

6.11 Serial Interface Timing Requirements

See Figure 3.

		MIN	MAX	UNIT
$f_{(SCLK)}$	SCLK frequency = 1 / t_{SCLK}	> DC		MHz
$t_{su(LOADS)}$	SEN to SCLK setup time	33		ns
$t_{su(LOADH)}$	SCLK to SEN hold time	33		ns
$t_{su(D)}$	SDATA setup time	33		ns
$t_{h(D)}$	SDATA hold time	33		ns



(1) With an external 100-Ω termination..

Figure 1. LVDS Output Voltage Levels

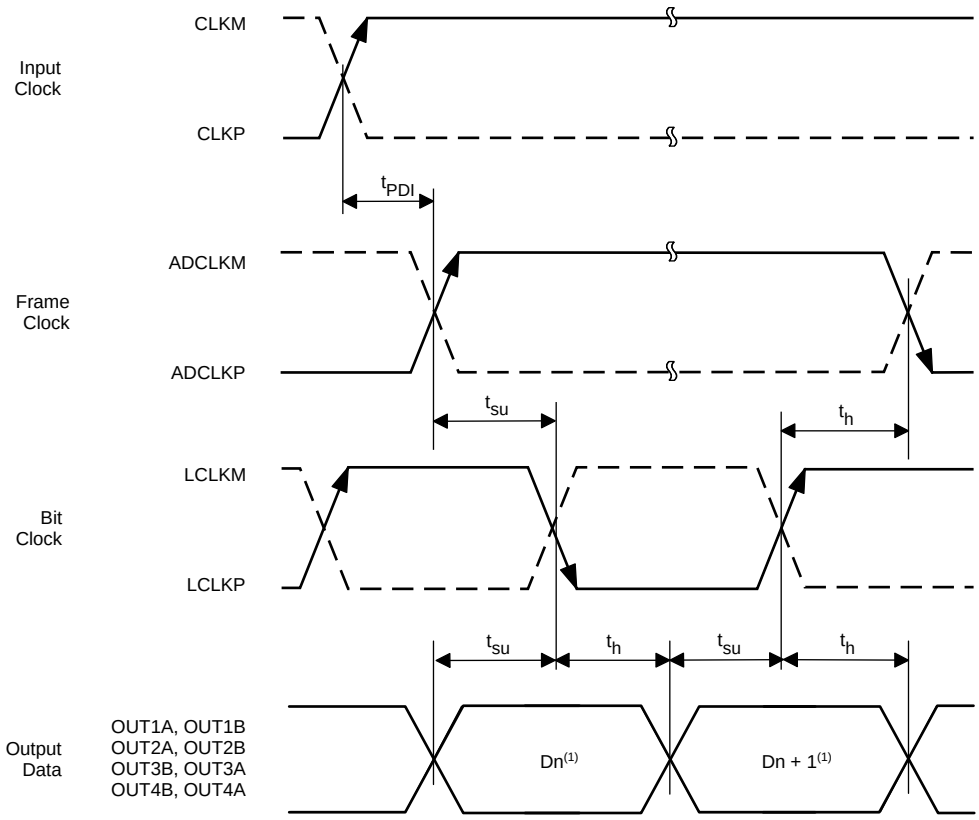


Figure 2. LVDS Mode Timing

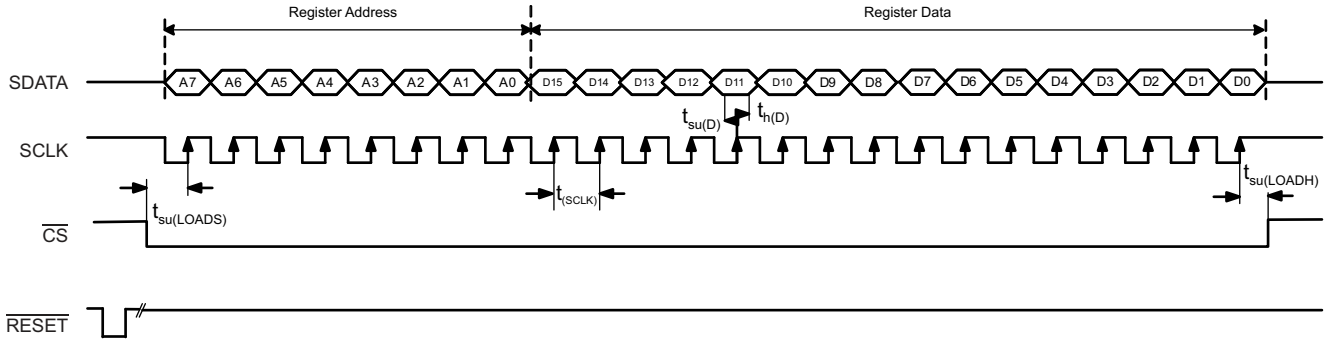


Figure 3. Serial Interface Timing

6.12 Typical Characteristics

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, 80-MSPS sampling clock frequency, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

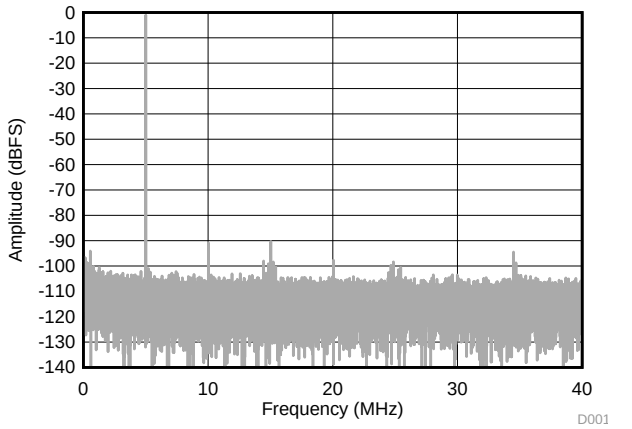


Figure 4. FFT for 5-MHz Input Signal

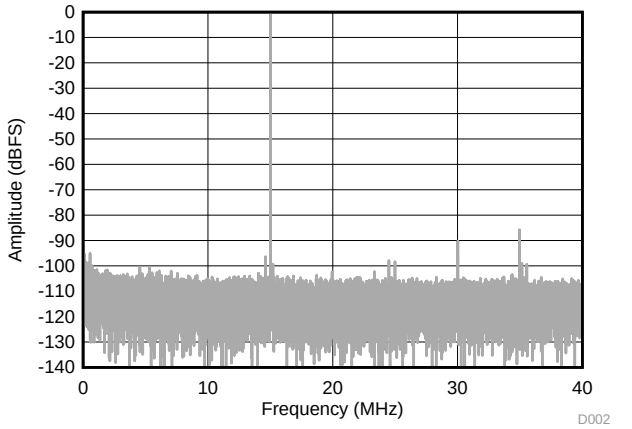


Figure 5. FFT for 15-MHz Input Signal

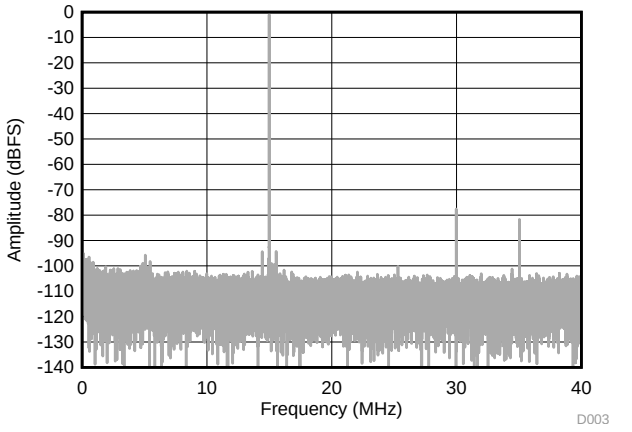


Figure 6. FFT for 65-MHz Input Signal

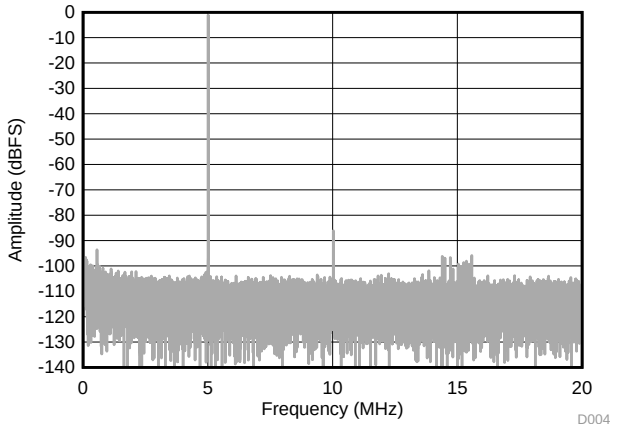
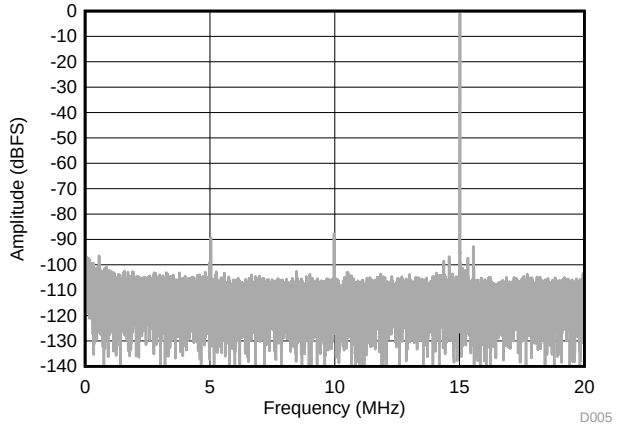


Figure 7. FFT For 5-MHz Input Signal

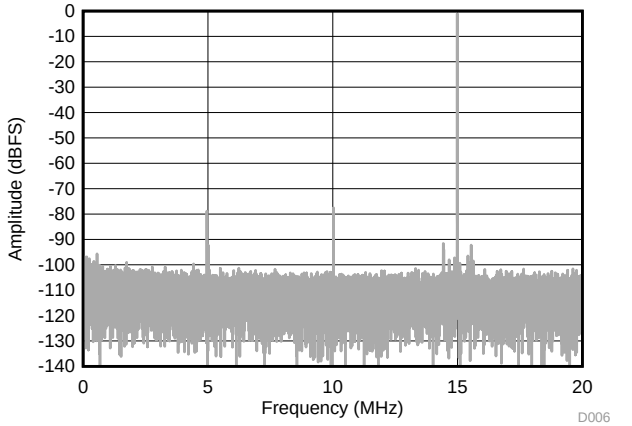
Typical Characteristics (continued)

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, 80-MSPS sampling clock frequency, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.



SNR = 69.6 dBFS SINAD = 69.5 dBFS
SFDR = 86.8 dBc THD = 84 dBc
Sample Rate = 40 MSPS

Figure 8. FFT for 15-MHz Input Signal



SNR = 67.2 dBFS SINAD = 66.6 dBFS
SFDR = 76.5 dBc THD = 74 dBc
Sample Rate = 40 MSPS

Figure 9. FFT for 65-MHz Input Signal

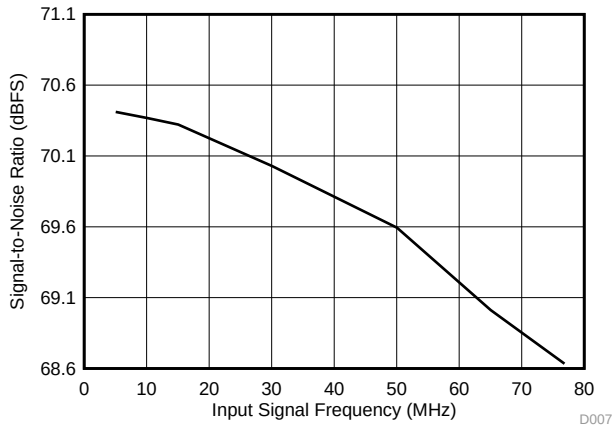


Figure 10. Signal-to-Noise Ratio (SNR) vs Input Signal Frequency

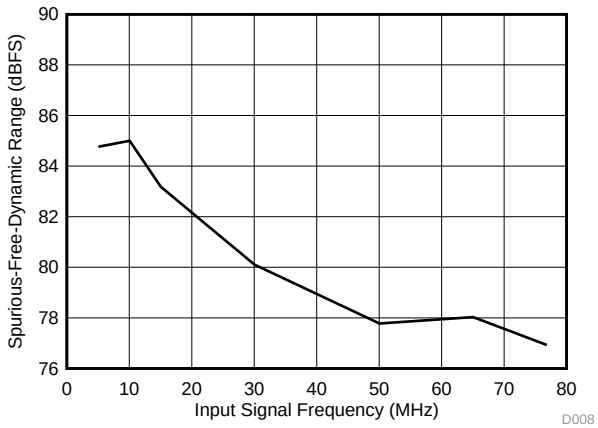


Figure 11. Spurious-Free-Dynamic Range (SFDR) vs Input Signal Frequency

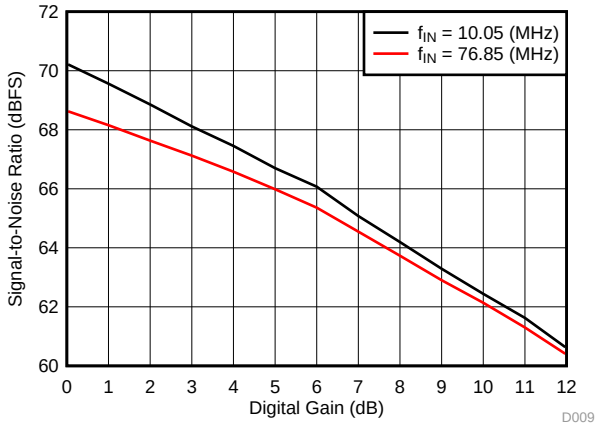


Figure 12. SNR vs Digital Gain

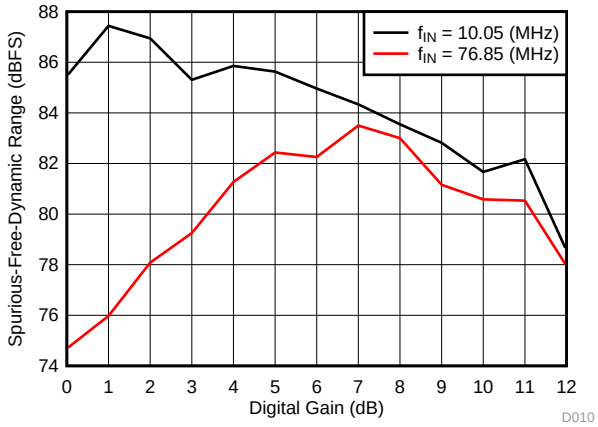


Figure 13. SFDR vs Digital Gain

Typical Characteristics (continued)

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, 80-MSPS sampling clock frequency, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

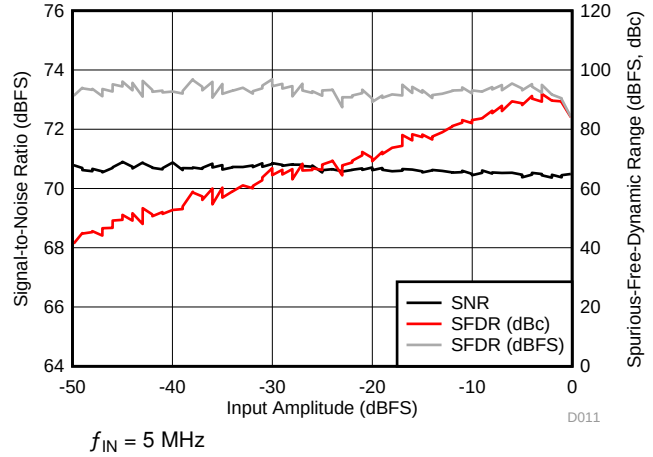


Figure 14. Performance vs Input Signal Amplitude

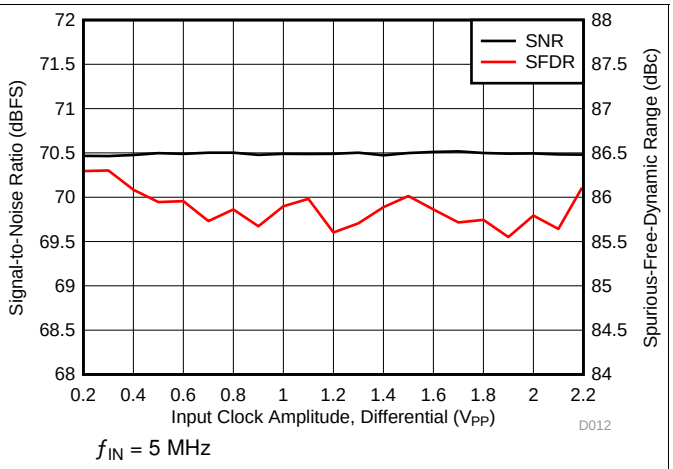


Figure 15. Performance vs Input Clock Amplitude

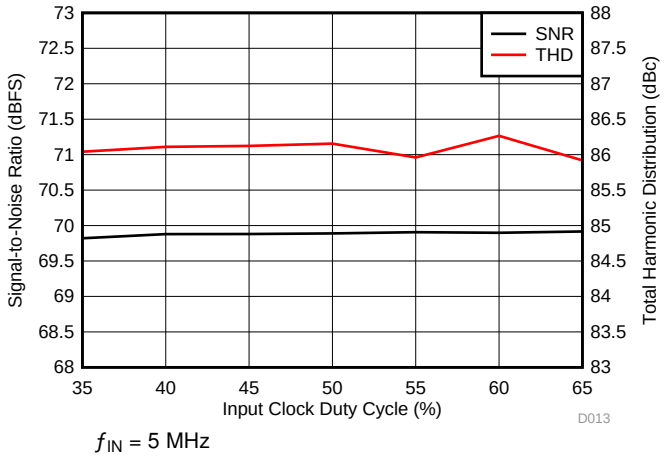


Figure 16. Performance vs Input Clock Duty Cycle

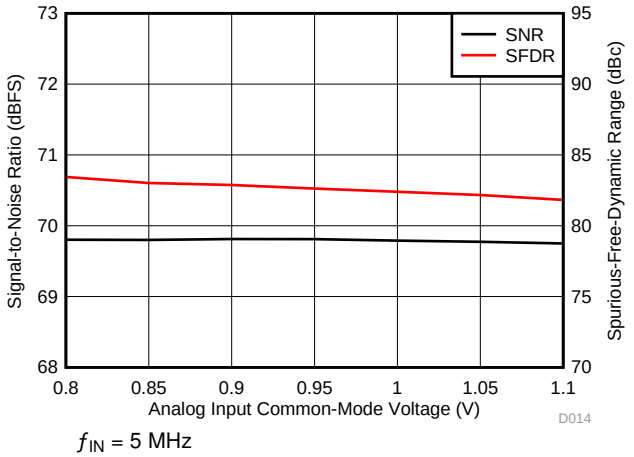


Figure 17. Performance vs Input Common-Mode

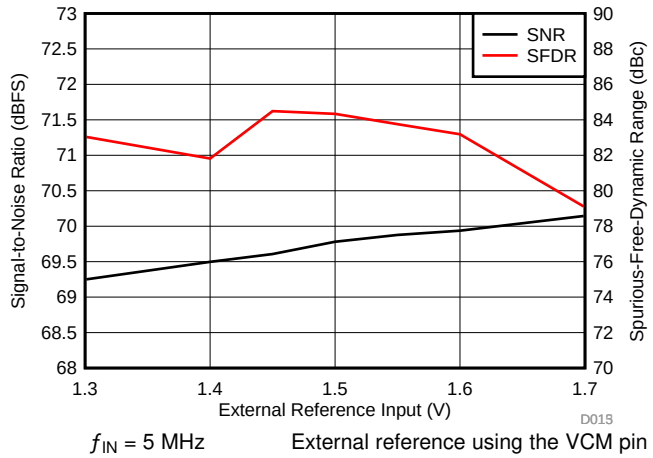


Figure 18. Performance in External Reference Mode

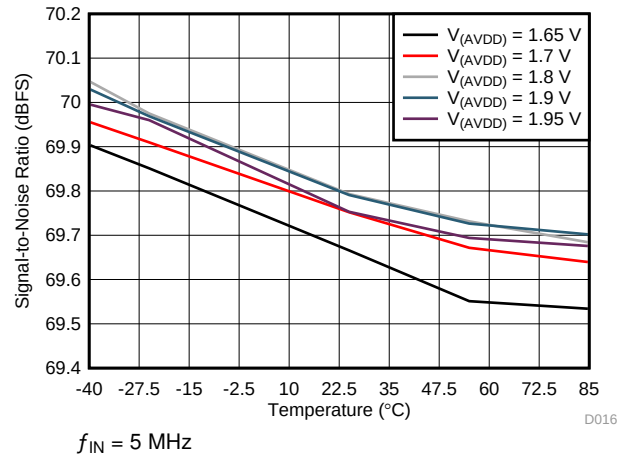
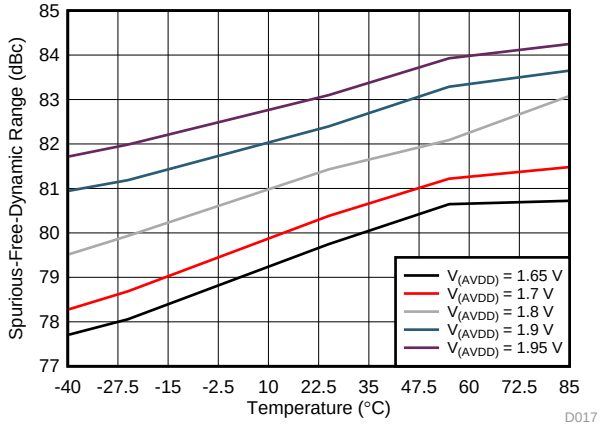


Figure 19. SNR vs AVDD and Temperature

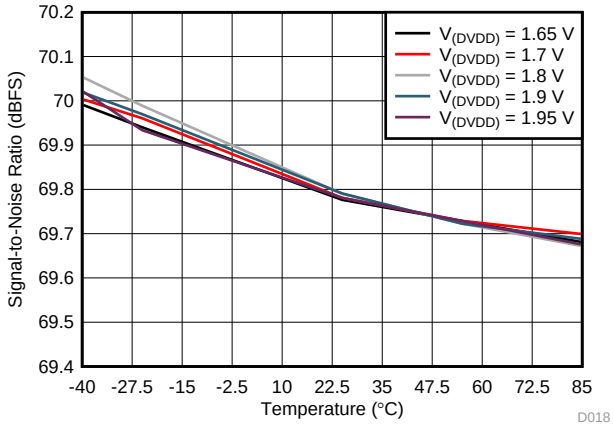
Typical Characteristics (continued)

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, 80-MSPS sampling clock frequency, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.



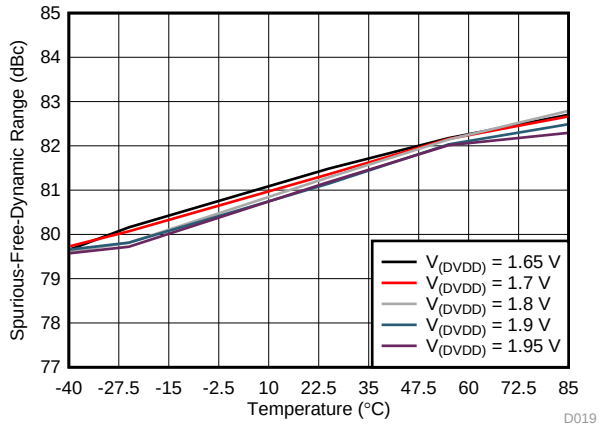
f_{IN} = 5 MHz

Figure 20. SFDR vs AVDD and Temperature



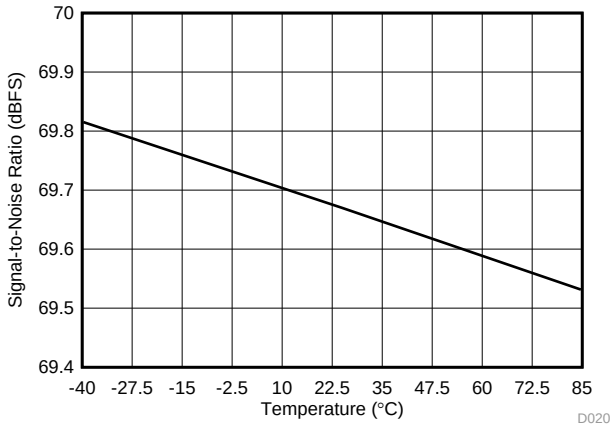
f_{IN} = 5 MHz

Figure 21. SNR vs DVDD and Temperature



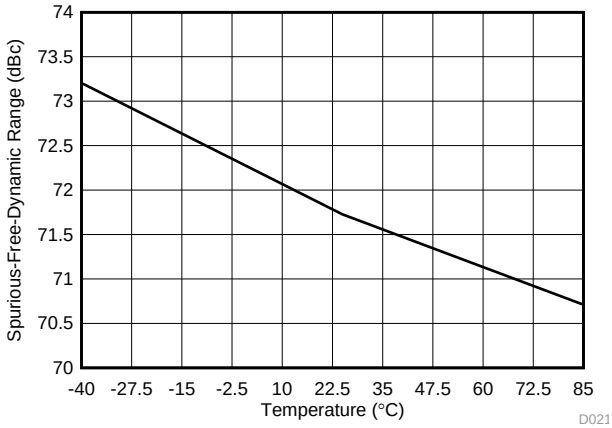
f_{IN} = 5 MHz

Figure 22. SFDR vs DVDD and Temperature



A 0.7-V_{PP} 5-MHz sine-wave input is applied on the INx_P pin
The INx_M pin is connected to the device VCM pin

Figure 23. SNR vs Temperature For Single-Ended Input



A 0.7-V_{PP} 5-MHz sine-wave input is applied on the INx_P pin
The INx_M pin is connected to the device VCM pin

Figure 24. SFDR vs Temperature for Single-ended Input

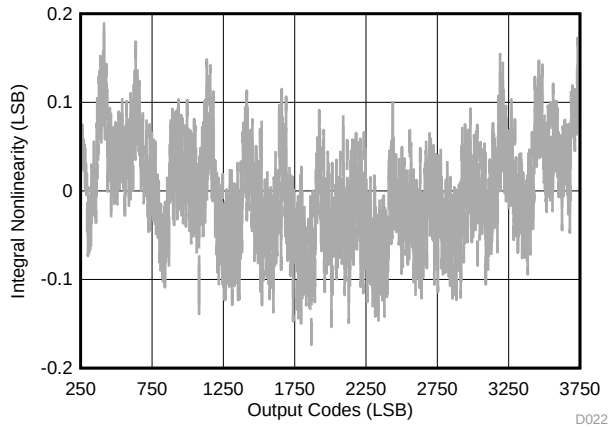


Figure 25. Integral Nonlinearity

Typical Characteristics (continued)

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, 80-MSPS sampling clock frequency, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

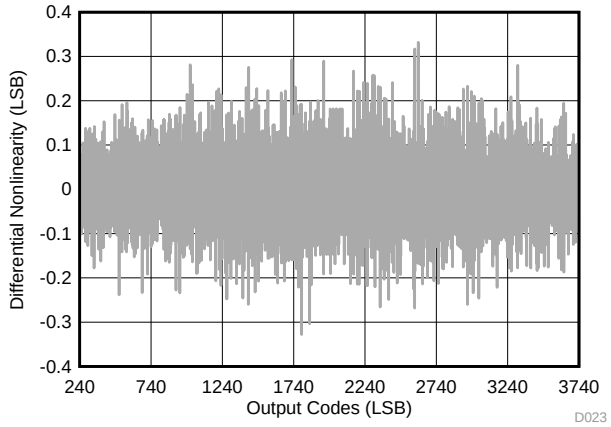
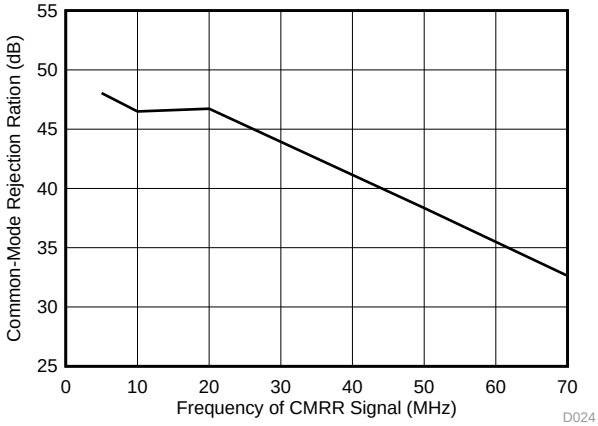


Figure 26. Differential Nonlinearity



f_{IN} = 3 MHz 50-mV_{PP} signal superimposed on the input common-mode

Figure 27. CMRR vs Frequency

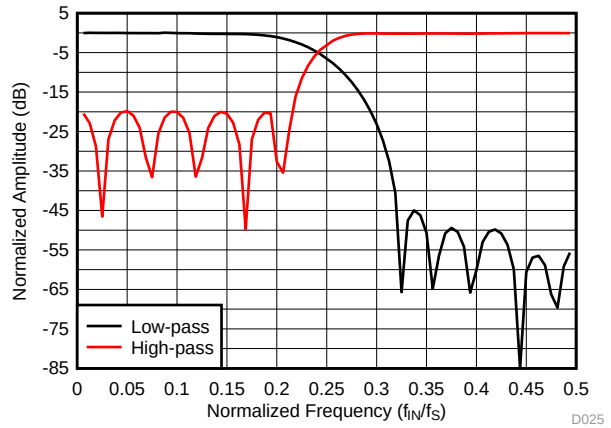


Figure 28. Filter Response (Decimate-by-2)

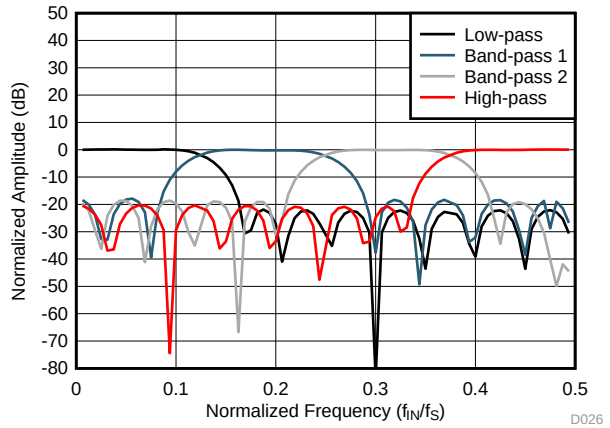


Figure 29. Filter Response (Decimate-by-4)

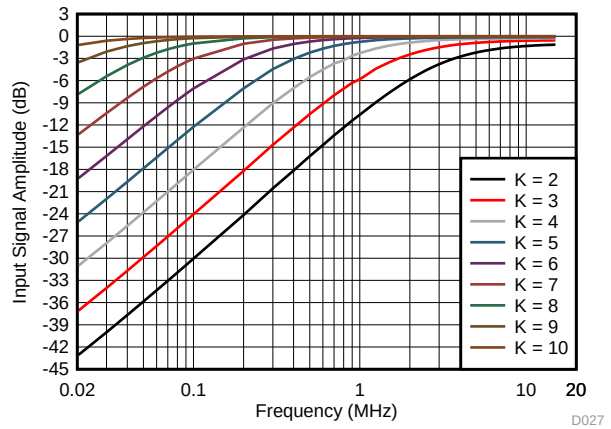
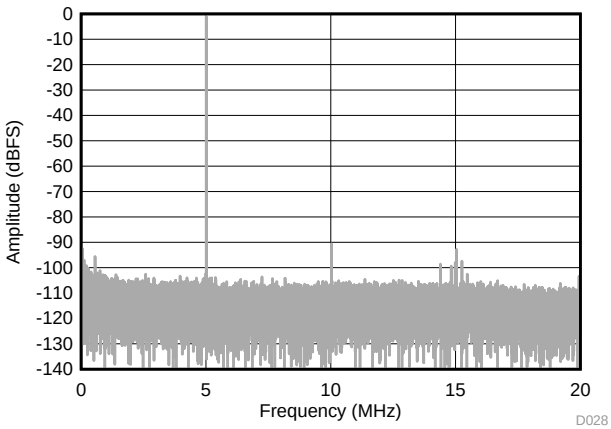


Figure 30. Digital High-Pass Filter Response



SNR = 70.8 dBFS SINAD = 70.7 dBFS SFDR = 88.7 dBc
THD = 87.3 dBc Decimate-by-2 filter enabled

Figure 31. FFT for 5-MHz Input Signal (Sample Rate = 80 MSPS With Decimation Filter = 2)

Typical Characteristics (continued)

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, 80-MSPS sampling clock frequency, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

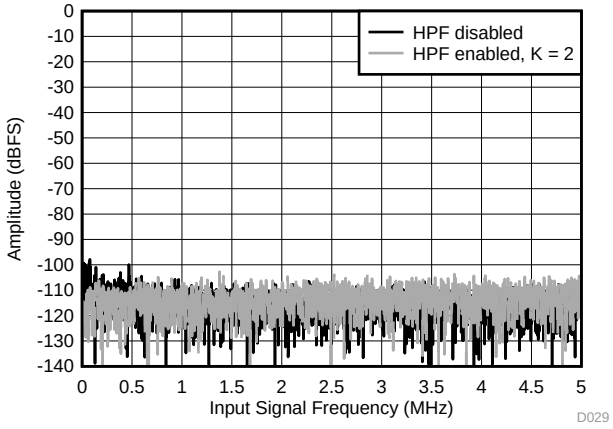


Figure 32. FFT With HPF Enabled and Disabled (No Input Signal)

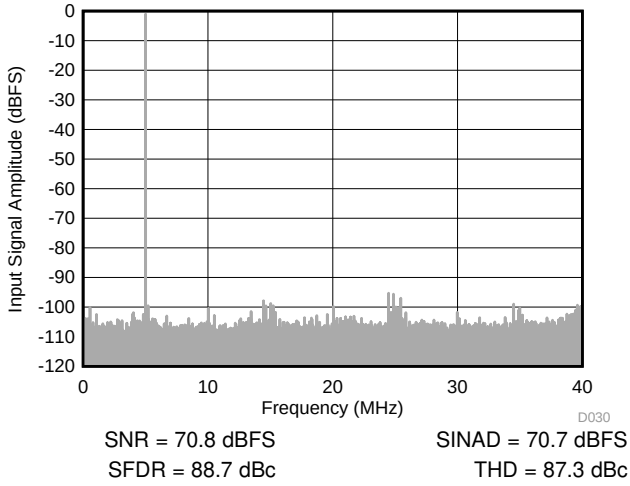


Figure 33. FFT (Full-Band) for 5-MHz Input Signal (Sample Rate = 80 MSPS With Low-Frequency Noise Suppression Enabled)

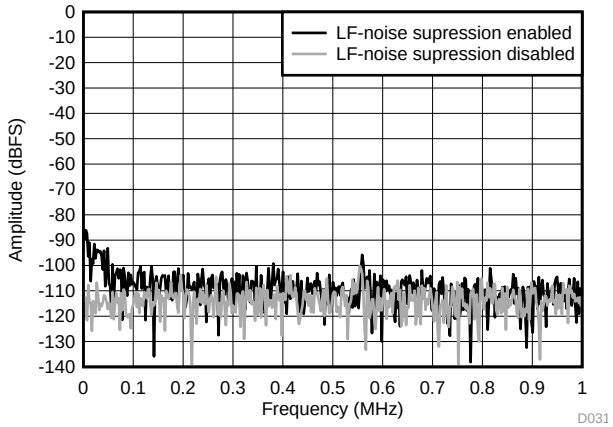


Figure 34. FFT (0 MHz to 1 MHz) for 5-MHz Input Signal (Sample Rate = 80 MSPS With Low-Frequency Noise Suppression Enabled)

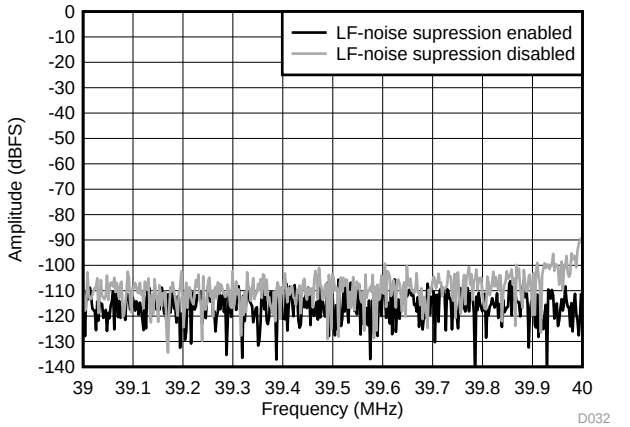


Figure 35. FFT (39 MHz to 40 MHz) for 5-MHz Input Signal (Sample Rate = 80 MSPS With Low-Frequency Noise Suppression Enabled)

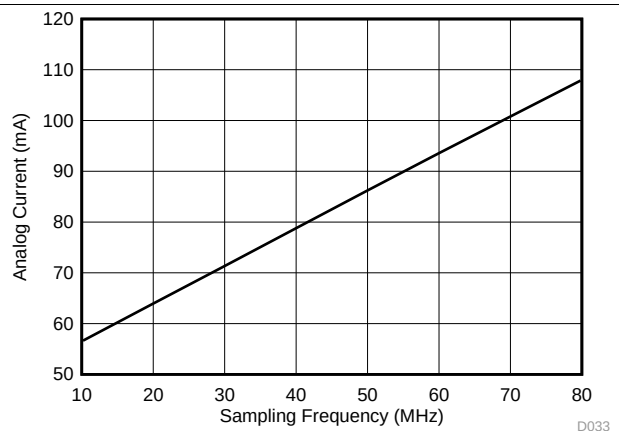


Figure 36. Analog Supply Current

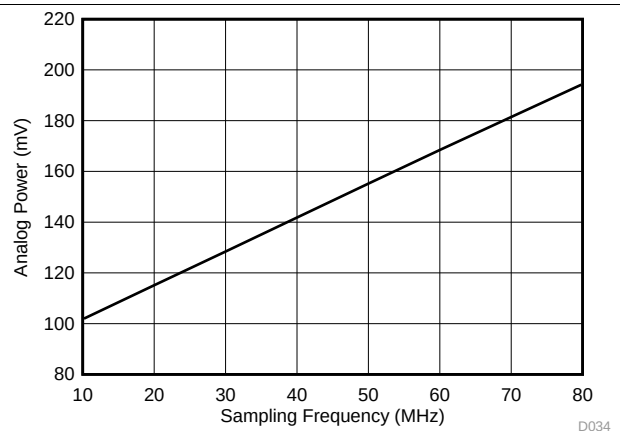


Figure 37. Power Consumption on Analog Supply

Typical Characteristics (continued)

Typical values are at 25°C, $V_{(AVDD)}$ = 1.8 V, $V_{(LVDD)}$ = 1.8 V, 80-MSPS sampling clock frequency, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

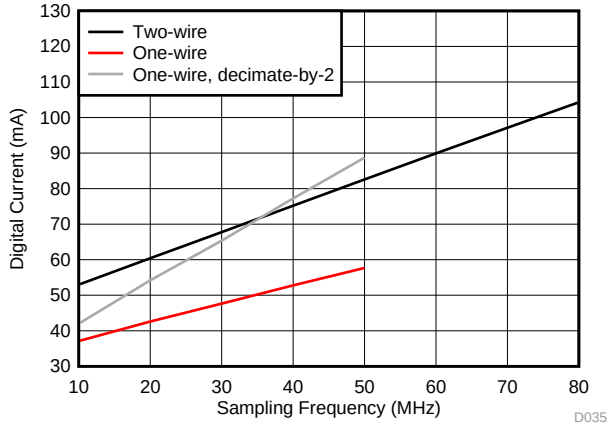


Figure 38. Digital Supply Current

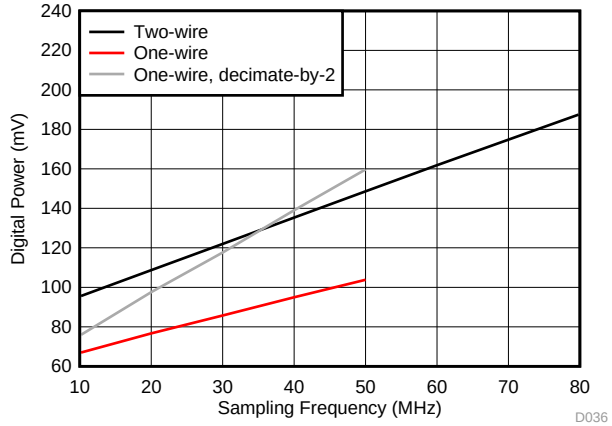


Figure 39. Power Consumption on Digital Supply

7 Detailed Description

7.1 Overview

The VSP5324-Q1 device is a high-performance, 12-bit, quad-channel, analog-to-digital converter (ADC) with sample rates up to 80 MSPS. The conversion process is initiated by a rising edge of the external input clock and when the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 11 clock cycles. The output is available as 12-bit data, in serial (low-voltage differential signaling) LVDS format, coded in either offset binary or binary twos complement format.

7.2 Functional Block Diagrams

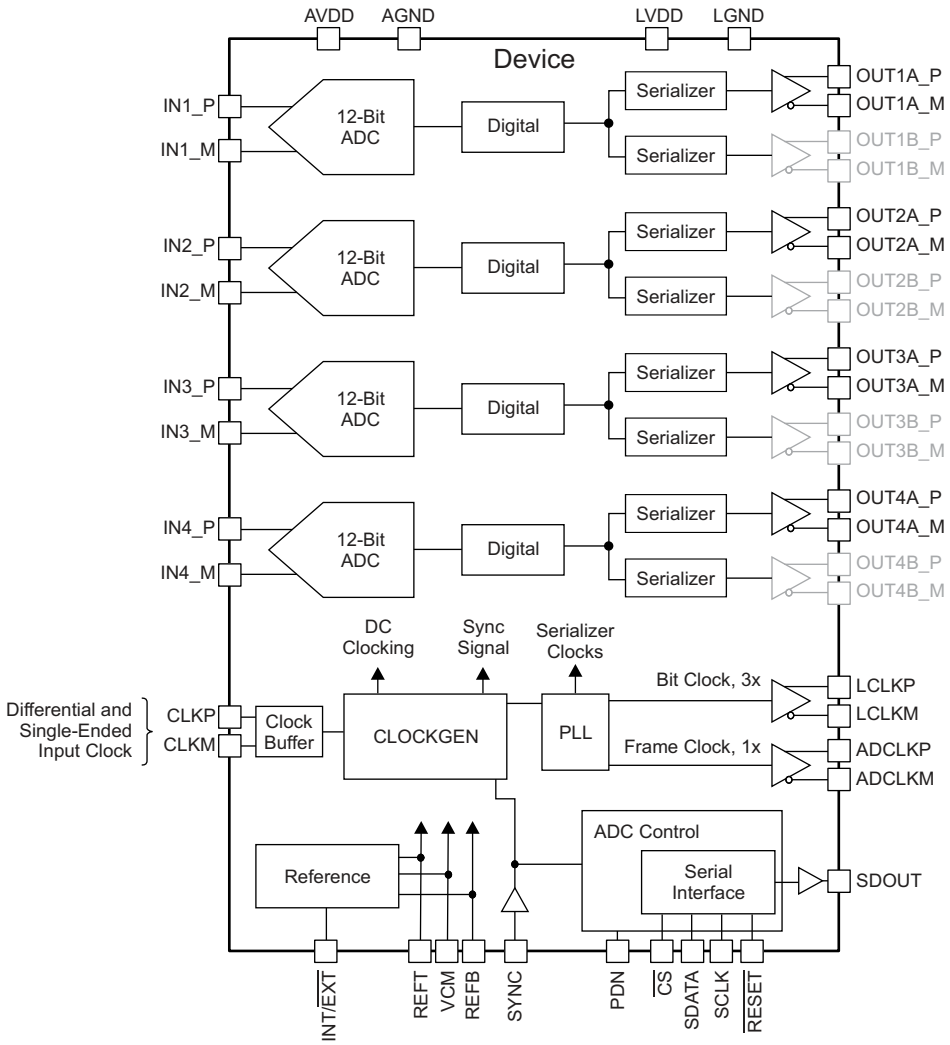


Figure 40. Quad ADC, One-Lane Configuration

Functional Block Diagrams (continued)

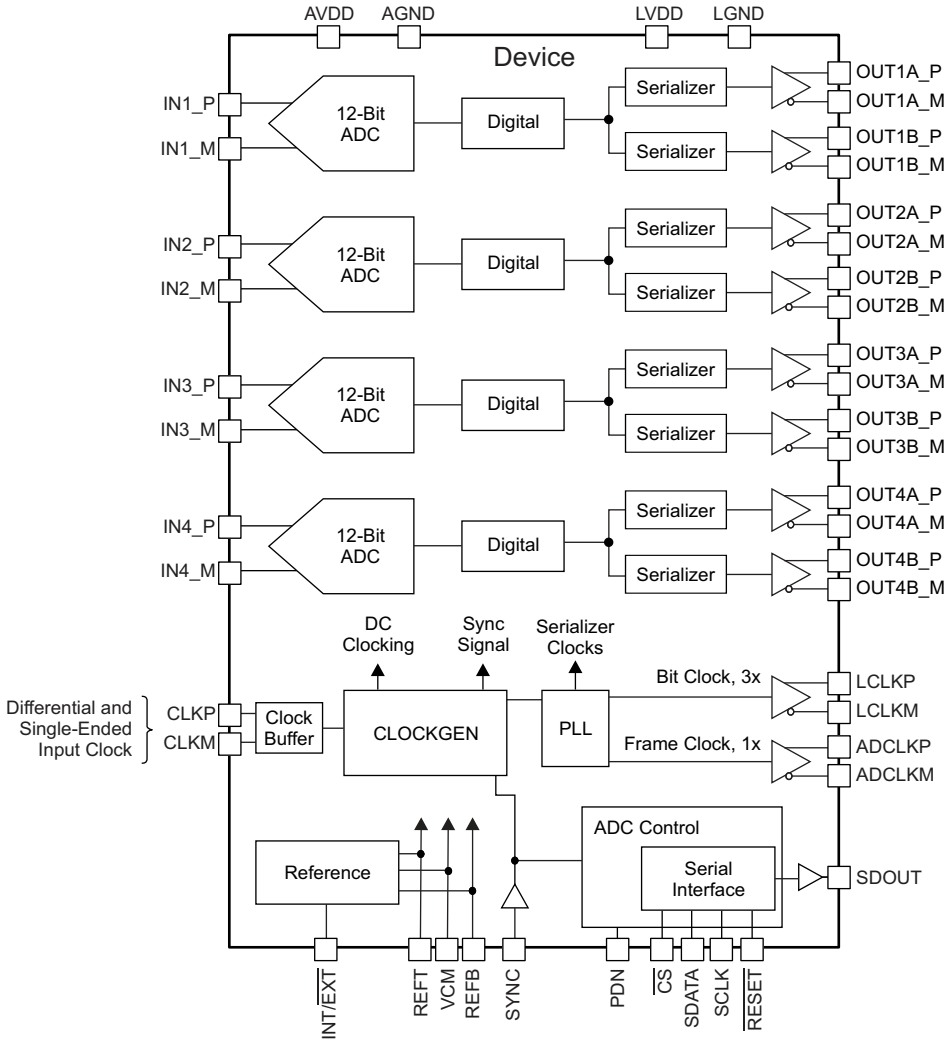


Figure 41. Quad ADC, Two-Lane Configuration

7.3 Feature Description

7.3.1 Analog Input

The analog input consists of a switched-capacitor-based differential sample-and-hold architecture, as shown in Figure 42. This differential topology results in very good AC performance even for high-input frequencies at high sampling rates. The INx_P and INx_M pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input pin (INx_P, INx_M) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing. The input sampling circuit has a high 3-dB bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage).

Feature Description (continued)

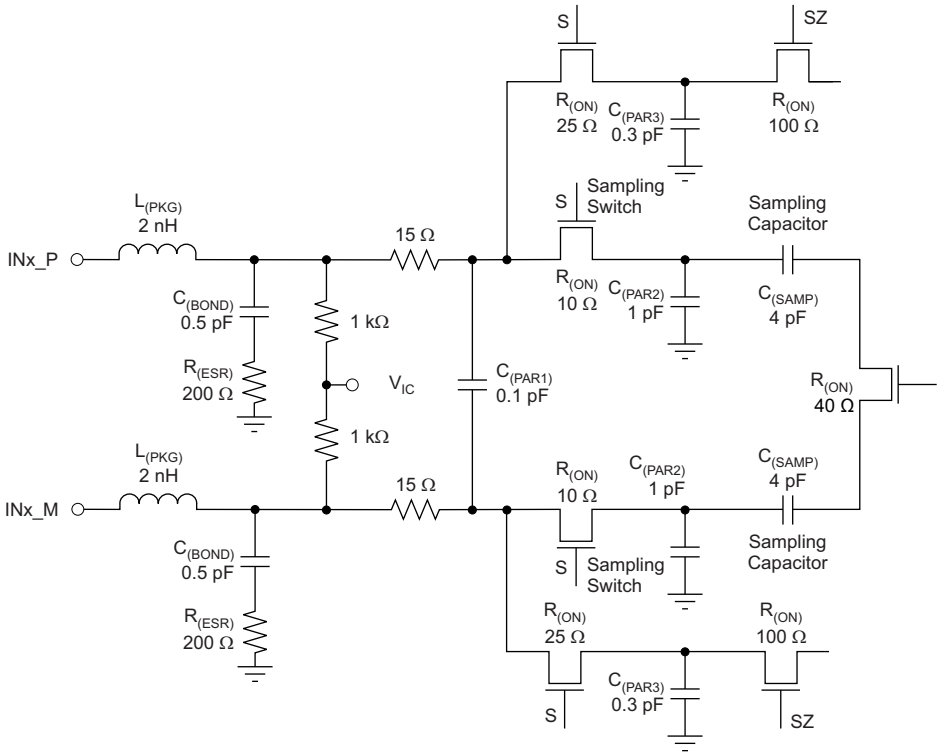


Figure 42. Analog Input Equivalent Circuit

7.3.1.1 Large- and Small-Signal Input Bandwidth

The analog input circuit small-signal bandwidth is high, approximately 550 MHz. When using an amplifier to drive the VSP5324-Q1 device, the total amplifier noise up to small-signal bandwidth must be considered. The device large-signal bandwidth depends on the input signal amplitude. The VSP5324-Q1 device supports 2-V_{PP} amplitude for input signal frequencies up to 80 MHz. For higher frequencies (greater than 80 MHz), the input signal amplitude must be decreased proportionally. For example, at 160 MHz, the device supports a maximum of 1-V_{PP} signal.

7.3.2 Digital Processing Block

The VSP5324-Q1 device integrates a set of commonly-used digital functions that can be used to ease system design such as test patterns and gain.

7.3.2.1 Digital Gain

The VSP5324-Q1 device includes programmable digital gain settings from 0 dB to 12 dB in 1-dB steps. The benefit of digital gain is to obtain improved SFDR performance. SFDR improvement is achieved at the expense of SNR; for each gain setting, SNR degrades by approximately 1 dB. Therefore, gain can be used to trade-off between SFDR and SNR.

For each gain setting, the analog input full-scale range support scales proportionally, as shown in Table 1. After reset, the device is in 0-dB gain mode. To use other gain settings, program the GAIN_CHx bits in registers 2Ah (see the *Register 2Ah (offset = 2Ah) [reset = 0]* section) and 2Bh (see the *Register 2Bh (offset = 2Bh) [reset = 0]* section).

Table 1. Analog Input Full-Scale Range Across Gains

DIGITAL GAIN (dB)	FULL-SCALE (V_{PP})
0	2
1	1.78
2	1.59
3	1.42
4	1.26
5	1.12
6	1.00
7	0.89
8	0.80
9	0.71
10	0.63
11	0.56
12	0.50

7.3.2.2 ADC Input Polarity Inversion

Normally, the INx_P pin represents the positive analog input pin and INx_M represents the complementary negative input. Setting the INVERT_ CH[4:1] bits listed in Table 2 (which provide individual control for each channel) causes the inputs to be swapped. INN now represents the positive input and INx_P represents the negative input.

Table 2. Polarity Inversion

ADDRESS (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
24	PRBS_SEED[22:16]							X(1)	INVERT_ CH4	X	INVERT_ CH3	X	X	INVERT_ CH2	X	INVERT_ CH1

(1) X = don't care.

7.3.2.3 SYNC Function

The SYNC function can be used to synchronize the RAMP test patterns across channels. This function can be enabled using either the hardware pin (SYNC) or software register bits.

To enable the software sync, set the register bit, EN_SYNC. To use the SYNC pin, set the EN_SYNC and HARD_SYNC_TP register bits. Note that SYNC pin is disabled after reset.

7.3.2.4 Output Data Format

Two output data formats are supported: twos complement and offset binary. These modes can be selected using the BTC_MODE serial interface register bit.

For a positive overload, the D[11:0] output data bits are FFFh in offset binary output format and 7FFh in twos complement output format. For a negative input overload, the output code is 000h in offset binary output format and 800h in twos complement output format.

7.3.3 Serial LVDS Interface

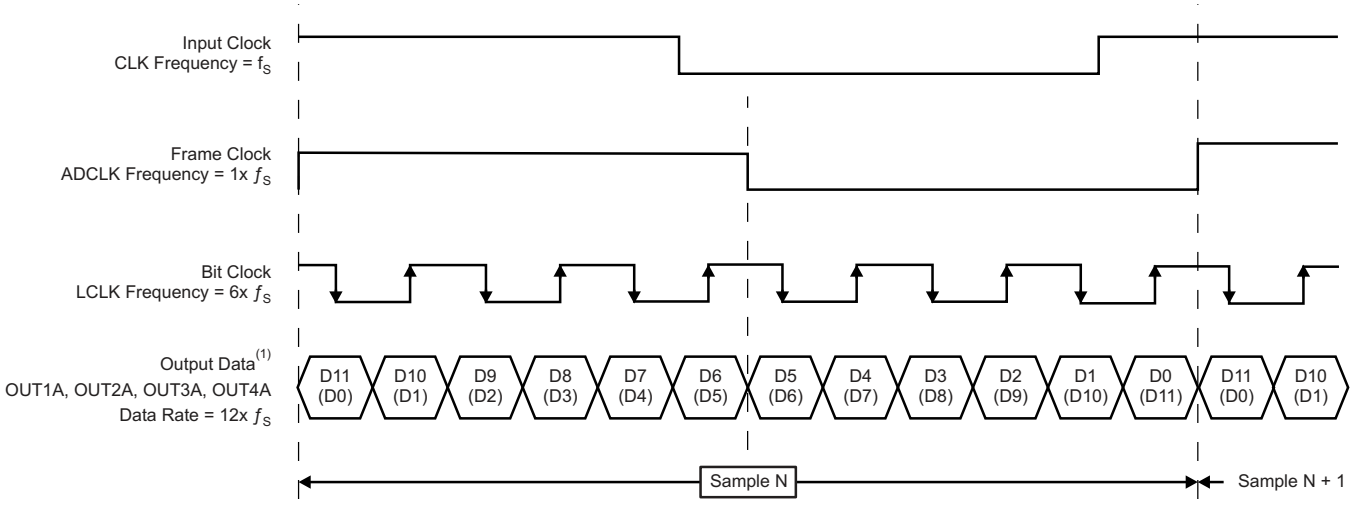
The VSP5324-Q1 device offers several flexible output options which makes interfacing to an (application-specific integrated circuit) ASIC or an (field-programmable gate array) FPGA easy. Each option can be easily programmed using the serial interface. Table 3 lists a summary of all options. This table also lists the default values after power-up and reset and a detailed description of each option. The output interface options are one-lane and two-lane serialization, and are described in the *One-Lane, 12x Serialization with DDR Bit Clock and 1x Frame Clock* and *Two-Lane, 6x Serialization with DDR Bit Clock and 0.5x Frame Clock* sections, respectively.

Table 3. Summary of Output Interface Options

FEATURE	OPTIONS	AVAILABLE IN		DEFAULT AFTER RESET	DESCRIPTION
		ONE-LANE	TWO-LANE		
Lane interface	One and two lanes	Yes	Yes	One-lane	One-lane: ADC data are sent serially over one pair of LVDS pins Two-lane: ADC data are split and sent serially over two pairs of LVDS pins
Serialization factor	12x	Yes	No	12x	—
DDR bit clock frequency	6x	Yes	No	6x	—
	3x	No	Yes	—	Only with two-lane interface
Frame clock frequency	1x sample rate	Yes	No	1x	—
	1/2x sample rate	No	Yes	—	Only with two-lane interface
Bit sequence	Byte-wise	No	Yes	Byte-wise	These options are available only with two-lane interface. Byte wise: ADC data are split into upper and lower bytes that are output on separate lanes. Bit wise: ADC data are split into even and odd bits that are output on separate lanes. Word wise: Successive ADC data samples are sent over separate lanes.
	Bit-wise	No	Yes	Byte-wise	
	Word-wise	No	Yes	Byte-wise	

7.3.3.1 One-Lane, 12x Serialization with DDR Bit Clock and 1x Frame Clock

The 12-bit ADC data are serialized and output over one LVDS pair per channel along with a 6x bit clock and 1x frame clock, as shown in Figure 43. The output data rate is 12x sample rate and is therefore suited for low sample rates (typically up to 50 MSPS).



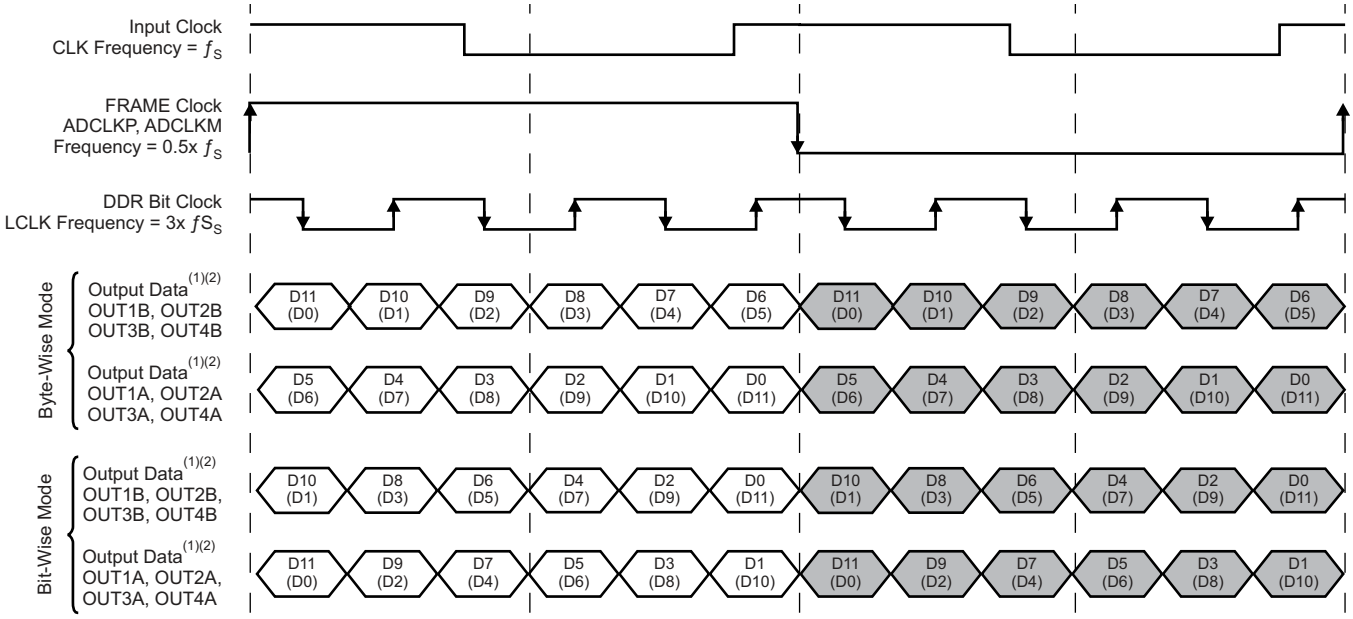
(1) Upper number is the data bit in MSB-first mode. Lower number in parenthesis is the data bit in LSB-first mode.

Figure 43. LVDS Output Interface, One-Lane, 12x Serialization

7.3.3.2 Two-Lane, 6x Serialization with DDR Bit Clock and 0.5x Frame Clock

In the two-lane serialization option, the 12-bit ADC data are serialized and output over two LVDS pairs per channel. The output data rate is a 6x sample rate with a 3x bit clock and a 1x frame clock.

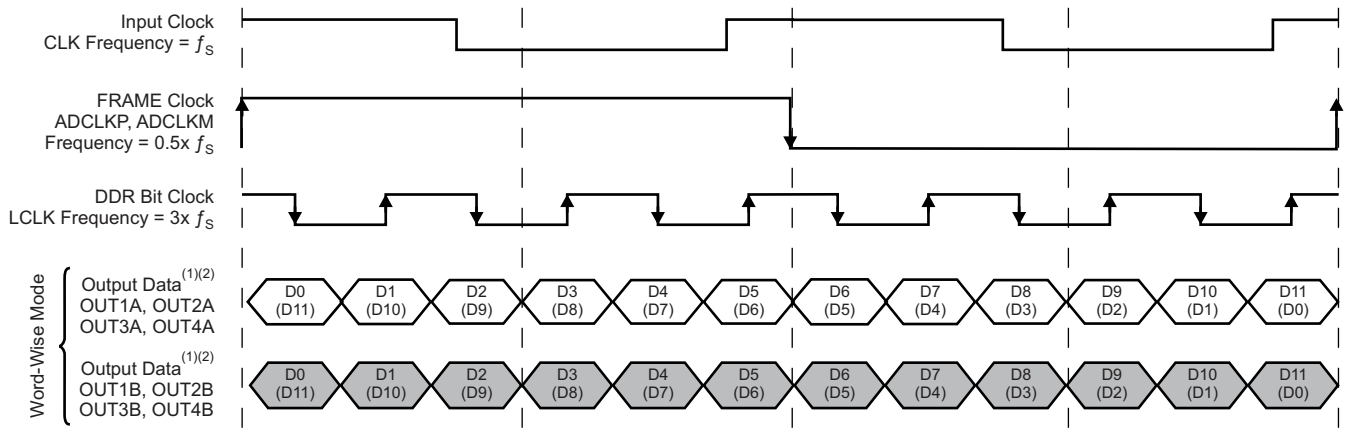
Compared to the one-line scenario, the two-line output data rate is half the amount. This difference allows the device to be used up to the maximum sampling rate. Two-lane serialization is available in bit-, byte-, and word-wise modes. Figure 44 shows the bit- and byte-wise modes and Figure 45 shows the word-wise mode.



(1) The upper number is the data bit in MSB-first mode. The lower number in parenthesis is the data bit in LSB-first mode.

(2) The unshaded cells indicate sample N data. The shaded cells indicate sample N + 1 data.

Figure 44. LVDS Output Interface, Two-Lane, 6x Serialization, Byte-Wise and Bit-Wise Modes



(1) The upper number is the data bit in MSB-first mode. The lower number in parenthesis is the data bit in LSB-first mode.

(2) The unshaded cells indicate sample N data. The shaded cells indicate sample N + 1 data.

Figure 45. LVDS Output Interface, Two-Lane, 6x Serialization, Word-Wise Mode

7.3.4 Bit Clock Programmability

The VSP5324-Q1 output interface is normally a DDR interface with the LCLK rising and falling edge transitions in the middle of alternate data windows. Figure 46 shows this default phase.

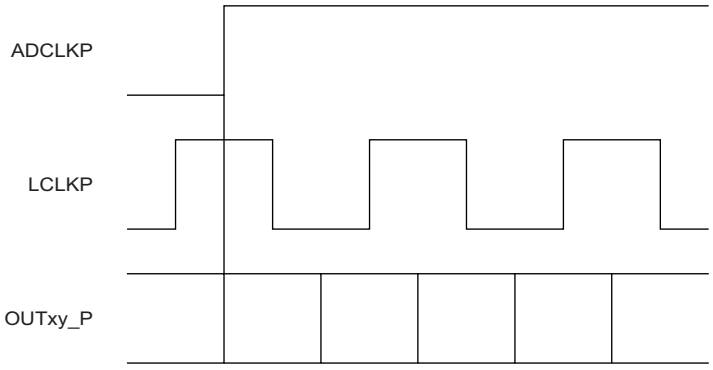


Figure 46. LCLK Default Phase (PHASE_DDR[1:0] = 10)

The LCLK phase can be programmed relative to the output frame clock and data using the PHASE_DDR[1:0] bits in Table 4. Figure 47 shows the LCLK phase modes.

Table 4. Clock Programmability

ADDRESS (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
42	EN_REF_VCM0	X(1)	X	X	X	X	X	X	X	PHASE_DDR[1:0]		X	EN_REF_VCM1	X	X	X

(1) X = don't care.

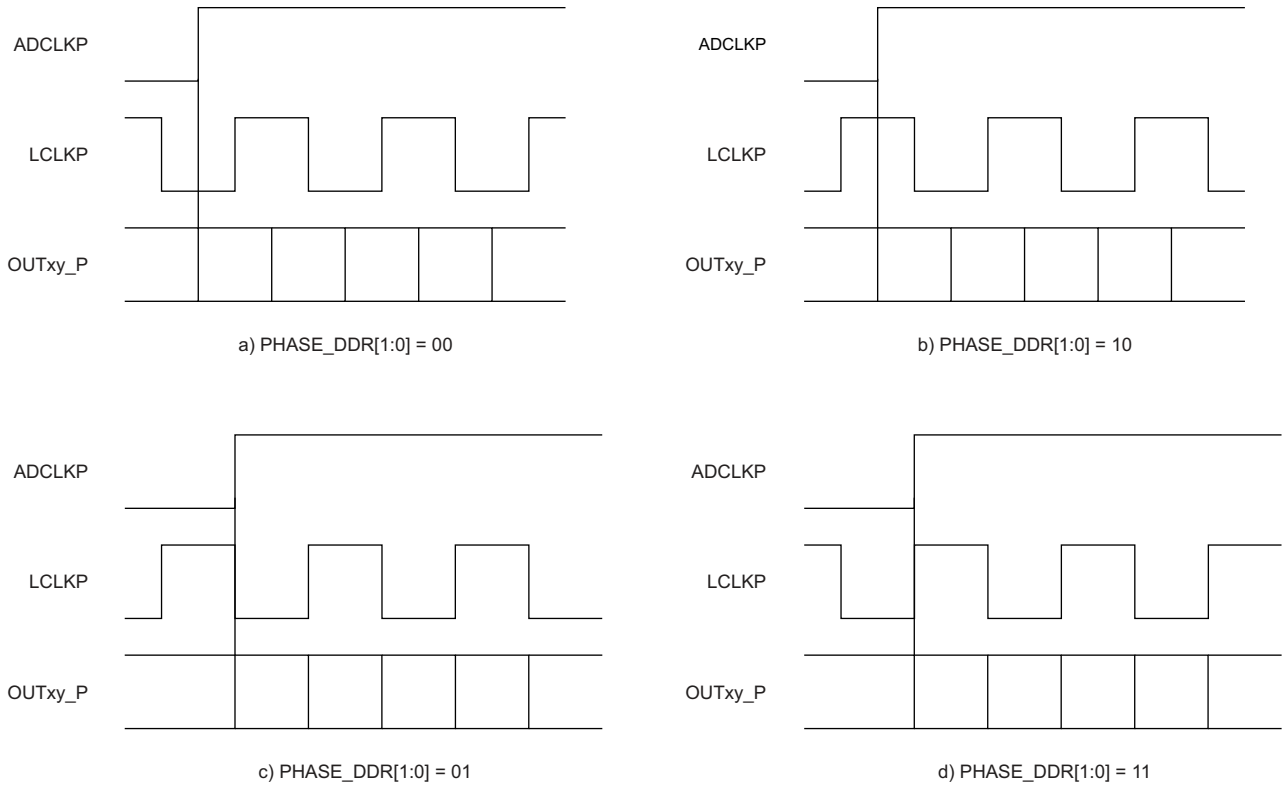


Figure 47. LCLK Phase Programmability Modes

7.3.5 LVDS Output Data and Clock Buffers

Figure 48 shows the equivalent circuit of each LVDS output buffer. After reset, the buffer presents a 100-Ω output impedance to match the external 100-Ω termination.

The V_{ID} voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100-Ω external termination. The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, the buffer helps improve signal integrity.

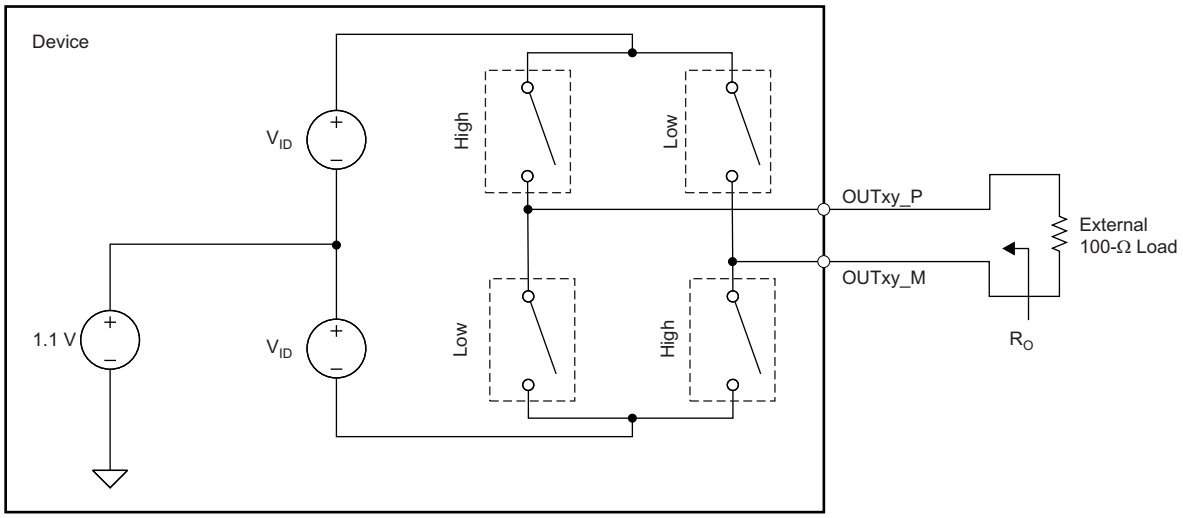


Figure 48. LVDS Buffer Equivalent Circuit

7.4 Device Functional Modes

7.4.1 External Reference Mode Of Operation

The VSP5324-Q1 device supports an external reference mode of operation either by:

- Forcing the reference voltages on the REFT and REFB pins, or by
- Applying the reference voltage on the VCM pin.

This mode can be used to operate multiple VSP5324-Q1 chips with the same (externally applied) reference voltage.

7.4.1.1 Using the REF Pins

For normal operation, the device requires two reference voltages, REFT and REFB. By default, the device generates these two voltages internally. To enable the external reference mode, set the register bits as listed in Table 5. This procedure powers down the internal reference amplifier and the two reference voltages can be forced directly on the REFT and REFB pins as ($V_{(REFT)}$ = 1.45 V ± 50 mV) and ($V_{(REFB)}$ = 0.45 V ±50 mV).

Use to calculate the relationship between the ADC full-scale input voltage (V_{FS}) and the applied reference voltages.

$$V_{FS} = 2 \times (V_{(REFT)} - V_{(REFB)}) \quad (1)$$

Device Functional Modes (continued)

7.4.1.2 Using the VCM Pin

In this mode, an external reference voltage (VREFIN) can be applied to the VCM pin. UseEquation 2 to calculate the relationship between the ADC full-scale input voltage and VREFIN.

$$V_{FS} = 2 \times VREFIN \quad (2)$$

To enable this mode, set the register bits as listed in Table 5. This action changes the function of the VCM pin to an external reference input pin. The voltage applied on VCM must be 1.5 V ±50 mV.

Table 5. External Reference Function

FUNCTION	EN_HIGH_ADDRS	EN_EXT_REF	EXT_REF_VCM
External reference using the REFT and REFB pins	1	1	00
External reference using the VCM pin	1	1	11

7.5 Programming

7.5.1 Serial Interface

The VSP5324-Q1 device has a set of internal registers that can be accessed by the serial interface formed by the $\overline{CS}$ (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. When $\overline{CS}$ is low the following occurs:

- The serial shift of bits into the device is enabled.
- Serial data (on the SDATA pin) are latched at every SCLK rising edge.
- The serial data are loaded into the register at every 24th SCLK rising edge.

If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active $\overline{CS}$ pulse.

The first eight bits form the register address and the remaining 16 bits form the register data. The interface can function with SCLK frequencies from 15 MHz down to very low speeds (of few Hertz) and also with a non-50% SCLK duty cycle.

7.5.2 Register Initialization

After power-up, the internal registers must be initialized to the default values. This reset can be accomplished in one of two ways:

1. A hardware reset is applied by a low-going pulse on the $\overline{RESET}$ pin (widths greater than 10 ns), as shown in Figure 3 and Serial Interface Timing Requirements.
2. A software reset is applied by using the serial interface and setting the RST bit (register 00h, bit D0) high. This setting initializes the internal registers to default values and then self-resets the RST bit low. In this case, the $\overline{RESET}$ pin is kept high (inactive).

See the *Serial Interface Timing Requirements* section and Figure 3 for timing information.

7.5.3 Serial Register Readout

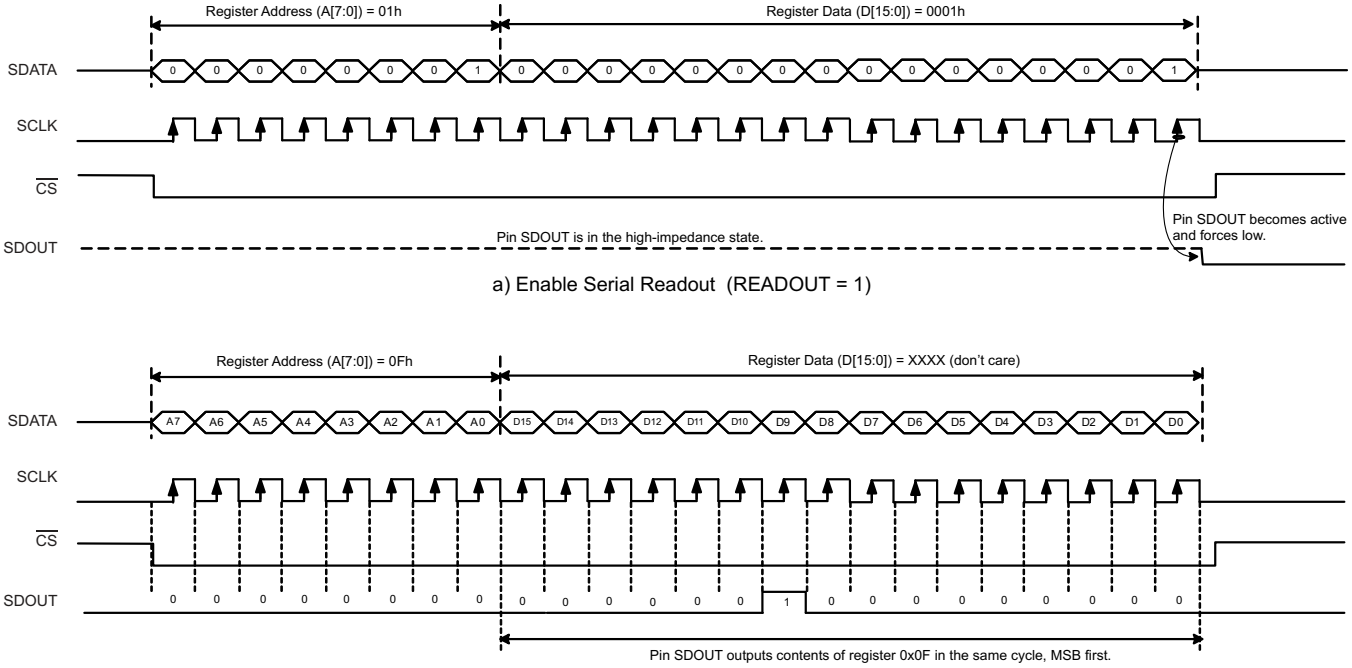
The device includes a mode where the contents of the internal registers can be readback on the SDOUT pin, as shown in Figure 49. This mode can useful as a diagnostic check to verify the serial interface communication between the external controller and ADC.

By default, after power-up and device reset, the SDOUT pin is high-impedance. When readout mode is enabled using the READOUT register bit, the SDOUT pin outputs the contents of the selected register serially in the following sequence:

1. The READOUT register bit must be set to 1 in order for the device to enter readout mode. This setting disables any further writes into the internal registers, except for the register at address 01h. Note that the READOUT bit is also located in this register. The device can exit readout mode by writing the READOUT bit to 0. Only the register contents of address 01h are unable to be read in register readout mode.
2. The read cycle is initiated by clocking the register address A[7:0] on the SDIN pin.

Programming (continued)

3. The device serially outputs the contents (D[15:0]) of the selected register on the SDOUT pin.
4. The external controller latches the contents at the SCLK rising edge.
5. The READOUT register bit is set to 0 to exit serial readout mode, which enables all registers of the device to be written to. At this point, the SDOUT pin enters a high-impedance state.



a) Enable Serial Readout (READOUT = 1)

b) Read contents of register 0Fh. This register is initialized with 0200h (previously, the device was in global power down).

Figure 49. Serial Readout Timing

After reset, the device default states include the following:

- The device is in normal operation mode with 12x serialization enabled for all channels.
- Output interface is one-lane, 12x serialization with a 6x bit clock and a 1x frame clock frequency.
- Data format is LSB-first and offset binary.
- Serial readout is disabled.
- The $\overline{PD}$ pin is configured as a global power-down pin.
- Digital gain is set to 0 dB.

7.6 Register Maps

Table 6. Serial Register Memory Map

ADDRESS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	X(1)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RST
01	X	X	X	X	X	X	X	X	X	X	X	EN_HIGH_ ADDRS	X	X	X	READOUT
02	X	X	EN_SYNC	X	X	X	X	X	X	X	X	X	X	X	X	X
0A	RAMP_PAT_RESET_VAL															
0F	X	X	X	X	X	PDN_PIN_ CFG	PDN_ COM PLETE	PDN_ PARTIAL	PDN_CH4	X	PDN_CH3	X	PDN_CH2	X	PDN_CH1	X
14	X	X	X	X	X	X	X	X	LFNS_CH4	X	LFNS_CH3	X	X	LFNS_CH2	X	LFNS_CH1
1C	X	EN_ FRAME_ PAT	ADCLKOUT[11:0]												X	X
23	PRBS_SEED[15:0]															
24	PRBS_SEED[22:16]							X	INVERT_ CH4	X	INVERT_ CH3	X	X	INVERT_ CH2	X	INVERT_ CH1
25	HARD_ SYNC_TP	PRBS_ SEED_ FROM_ REG	X	PRBS_ TP_EN	X	X	X	TP_SOFT_ SYNC	X	EN_RAMP	DUAL_ CUSTOM_ PAT	SINGLE_ CUSTOM_ PAT	BITS_CUSTOM2[13:12]		BITS_CUSTOM1[13:12]	
26	BITS_CUSTOM1[9:0]										X	X	X	X	X	X
27	BITS_CUSTOM2[9:0]										X	X	X	X	X	X
28	EN_BIT ORDER	X	X	X	X	X	X	BIT_WISE	EN_WORDWISE_BY_CH[7:0]							
29	X	X	X	X	X	X	X	X	X	X	X	X	X	X	GLOBAL_ EN_FILTER	X
2A	X	X	X	X	GAIN_CH2[3:0]				X	X	X	X	GAIN_CH1[3:0]			
2B	X	X	X	X	GAIN_CH3[3:0]				X	X	X	X	GAIN_CH4[3:0]			
2E	X	HPF_EN_ CH1	HPF_CORNER _CH1[3:0]			FILTER1_COEFF_SET[2:0]			FILTER1_RATE[2:0]				X	ODD_TAP1	X	USE_ FILTER1
30	X	HPF_EN_ CH2	HPF_CORNER _CH2[3:0]			FILTER2_COEFF_SET[2:0]			FILTER2_RATE[2:0]				X	ODD_TAP2	X	USE_ FILTER2
33	X	HPF_EN_ CH3	HPF_CORNER _CH3[3:0]			FILTER3_COEFF_SET[2:0]			FILTER3_RATE[2:0]				X	ODD_TAP3	X	USE_ FILTER3
35	X	HPF_EN_ CH4	HPF_CORNER _CH4[3:0]			FILTER4_COEFF_SET[2:0]			FILTER4_RATE[2:0]				X	ODD_TAP4	X	USE_ FILTER4
38	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DATA_RATE[1:0]	

(1) X = don't care.

Register Maps (continued)

Table 6. Serial Register Memory Map (continued)

ADDRESS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
42	EN_REF_VCM0	X	X	X	X	X	X	X	X	PHASE_DDR[1:0]		X	EN_REF_VCM1	X	X	X
45	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PAT_SYNC	PAT_DESKEW
46	ENABLE 46	X	FALL_SDR	X	EN_16BIT	EN_14BIT	EN_12BIT	X	X	X	X	EN_SDR	MSB_FIRST	BTC_MODE	X	EN_2LANE
50	ENABLE 50	X	X	X	X	X	X	X	MAP_CH12_TO_OUT1B[3:0]				MAP_CH12_TO_OUT1A[3:0]			
51	ENABLE 51	X	X	X	MAP_CH12_TO_OUT2B[3:0]				MAP_CH12_TO_OUT2A[3:0]				X	X	X	X
53	ENABLE 53	X	X	X	MAP_CH34_TO_OUT3B[3:0]				X	X	X	X	X	X	X	X
54	ENABLE 54	X	X	X	X	X	X	X	X	X	X	X	MAP_CH34_TO_OUT3A[3:0]			
55	ENABLE 55	X	X	X	X	X	X	X	MAP_CH34_TO_OUT4A[3:0]				MAP_CH34_TO_OUT4B[3:0]			
F0	EN_EXT_REF	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

7.6.1 Serial Registers

7.6.1.1 Register 00h (offset = 00h) [reset = 0]

This is a general register.

Figure 50. Register 00h

D15	D14	D13	D12	D11	D10	D9	D8
X							
W-0							
D7	D6	D5	D4	D3	D2	D1	D0
X							RST
W-0							W-0

Table 7. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D1	X	W	0	Don't care bits
D0	RST	W	0	Reset 0 = Normal operation (default) 1 = Self-clearing software reset (after reset, this bit is set to 0)

7.6.1.2 Register 01h (offset = 01h) [reset = 0]

This is a general register.

Figure 51. Register 01h

D15	D14	D13	D12	D11	D10	D9	D8
X							
W-0							
D7	D6	D5	D4	D3	D2	D1	D0
X			EN_HIGH_ADDRS	X			READOUT
W-0			W-0	W-0			W-0

Table 8. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D5	X	W	0	Don't care bits
D4	EN_HIGH_ADDRS	W	0	Register F0h access 0 = Disables access to register F0h (default) 1 = Enables access to register F0h
D3-D1	X	W	0	Don't care bits
D0	READOUT	W	0	Register mode readout 0 = Normal operation (default) 1 = Register mode readout

7.6.1.3 Register 02h (offset = 02h) [reset = 0]

This is a general register.

Figure 52. Register 02h

D15	D14	D13	D12	D11	D10	D9	D8
X		EN_SYNC	X				
R/W-0		R/W-0	R/W-0				
D7	D6	D5	D4	D3	D2	D1	D0
X							
R/W-0							

Table 9. Register 02h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D14	X	R/W	0	Don't care bits
D13	EN_SYNC	R/W	0	SYNC enable(1) 0 = Normal operation; SYNC feature disabled (default) 1 = SYNC feature enabled to synchronize test patterns
D12-D0	X	R/W	0	Don't care bits

(1) This bit must be set to 1 when the software or hardware SYNC feature is used; see bits D15 and D8 in the *Register 25h (offset = 25h) [reset = 0]* section.

7.6.1.4 Register 0Ah (offset = 0Ah) [reset = 0]

This is a general register.

Figure 53. Register 0Ah

D15	D14	D13	D12	D11	D10	D9	D8
RAMP_PAT_RESET_VAL							
R/W-0							
D7	D6	D5	D4	D3	D2	D1	D0
RAMP_PAT_RESET_VAL							
R/W-0							

Table 10. Register 0Ah Field Descriptions

Bit	Field	Type	Reset	Description
D15-D0	RAMP_PAT_RESET_VAL	R/W	0	These bits determine the initial value of the ramp pattern after reset.

7.6.1.5 Register 0Fh (offset = 0Fh) [reset = 0]

This is a power-down mode register. All bits default to 0 after reset.

Figure 54. Register 0Fh

D15	D14	D13	D12	D11	D10	D9	D8
X					PDN_PIN_CFG	PDN_ COMPLETE	PDN_PARTIAL
R/W-0					R/W-0	R/W-0	R/W-0
D7	D6	D5	D4	D3	D2	D1	D0
PDN_CH4	X	PDN_CH3	X		PDN_CH2	X	PDN_CH1
R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	R/W-0	R/W-0

Table 11. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
D15-D11	X	R/W	0	Don't care bits
D10	PDN_PIN_CFG	R/W	0	PD pin configuration 0 = PD pin configured for complete power-down mode 1 = PD pin configured for partial power-down mode
D9	PDN_ COMPLETE	R/W	0	Complete power-down 0 = Normal operation 1 = Register mode for complete power-down (slower recovery)
D8	PDN_PARTIAL	R/W	0	Partial power-down 0 = Normal operation 1 = Partial power-down mode (fast recovery from power-down)
D7	PDN_CH4	R/W	0	ADC power-down mode for channel 4 0 = Normal operation 1 = Partial power-down mode (fast recovery from power-down)
D6	X	R/W	0	Don't care bit
D5	PDN_CH3	R/W	0	ADC power-down mode for channel 3 0 = Normal operation 1 = ADC power-down mode for channel 3
D4-D3	X	R/W	0	Don't care bits
D2	PDN_CH2	R/W	0	ADC power-down mode for channel 2 0 = Normal operation 1 = ADC power-down mode for channel 2
D1	X	R/W	0	Don't care bit
D0	PDN_CH1	R/W	0	ADC power-down mode for channel 1 0 = Normal operation 1 = ADC power-down mode for channel 1

7.6.1.6 Register 14h (offset = 14h) [reset = 0]

This is a general register.

Figure 55. Register 14h

D15	D14	D13	D12	D11	D10	D9	D8
X							
R/W-0							
D7	D6	D5	D4	D3	D2	D1	D0
LFNS_CH4	X	LFNS_CH3	X		LFNS_CH2	X	LFNS_CH1
R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	R/W-0	R/W-0

Table 12. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D8	X	R/W	0	Don't care bits
D7	LFNS_CH4	R/W	0	Noise-suppression mode selection for channel 4 0 = LFNS disabled (default) 1 = Low-frequency noise-suppression mode enable for channel 4
D6	X	R/W	0	Don't care bit
D5	LFNS_CH3	R/W	0	Noise-suppression mode selection for channel 3 0 = LFNS disabled (default) 1 = Low-frequency noise-suppression mode enable for channel 3
D4-D3	X	R/W	0	Don't care bits
D2	LFNS_CH2	R/W	0	Noise-suppression mode selection for channel 2 0 = LFNS disabled (default) 1 = Low-frequency noise-suppression mode enable for channel 2
D1	X	R/W	0	Don't care bit
D0	LFNS_CH1	R/W	0	Noise-suppression mode selection for channel 1 0 = LFNS disabled (default) 1 = Low-frequency noise-suppression mode enable for channel 1

7.6.1.7 Register 1Ch (offset = 1Ch) [reset = 0]

This is a test pattern register. All bits default to 0 after reset.

Figure 56. Register 1Ch

D15	D14	D13	D12	D11	D10	D9	D8
X	EN_FRAME_PAT	ADCLKOUT[11:0]					
R/W-0	R/W-0	R/W-0					
D7	D6	D5	D4	D3	D2	D1	D0
ADCLKOUT[11:0]						X	
R/W-0						R/W-0	

Table 13. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
D15	X	R/W	0	Don't care bit
D14	EN_FRAME_PAT	R/W	0	Frame pattern enable 0 = Normal frame clock operation 1 = Enables the output frame clock to be programmed through a pattern
D13-D2	ADCLKOUT[11:0]	R/W	0	ADCLK pin frame clock pattern These bits determine the 12-bit pattern for the frame clock on the ADCLKP and ADCLKN pins.
D1-D0	X	R/W	0	Don't care bits

7.6.1.8 Register 23h (offset = 23h) [reset = 0]

This is a test pattern register.

Figure 57. Register 23h

D15	D14	D13	D12	D11	D10	D9	D8
PRBS_SEED[15:0]							
R/W-0							
D7	D6	D5	D4	D3	D2	D1	D0
PRBS_SEED[15:0]							
R/W-0							

Table 14. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D0	PRBS_SEED[15:0]	R/W	0	PRBS pattern seed value, lower bits These bits determine the PRBS pattern starting seed value of the lower 16 bits. (Default = 0)

7.6.1.9 Register 24h (offset = 24h) [reset = 0]

This is a test pattern register. All bits default to 0 after reset.

Figure 58. Register 24h

D15	D14	D13	D12	D11	D10	D9	D8
PRBS_SEED[22:16]							X
R/W-0							R/W-0
D7	D6	D5	D4	D3	D2	D1	D0
INVERT_CH4	X	INVERT_CH3	X		INVERT_CH2	X	INVERT_CH1
R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	R/W-0	R/W-0

Table 15. Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D9	PRBS_SEED[22:16]	R/W	0	PRBS pattern seed value, upper bits These bits determine the PRBS pattern starting seed value of the upper seven bits.
D8	X	R/W	0	Don't care bit
D7	INVERT_CH4	R/W	0	Analog input pin polarity for channel 4 0 = Normal configuration (default) 1 = Electrically swaps the analog input pin polarity for channel 4
D6	X	R/W	0	Don't care bit
D5	INVERT_CH3	R/W	0	Analog input pin polarity for channel 3 0 = Normal configuration (default) 1 = Electrically swaps the analog input pin polarity for channel 3
D4-D3	X	R/W	0	Don't care bits
D2	INVERT_CH2	R/W	0	Analog input pin polarity for channel 2 0 = Normal configuration (default) 1 = Electrically swaps the analog input pin polarity for channel 2
D1	X	R/W	0	Don't care bit
D0	INVERT_CH1	R/W	0	Analog input pin polarity for channel 1 0 = Normal configuration (default) 1 = Electrically swaps the analog input pin polarity for channel 1

7.6.1.10 Register 25h (offset = 25h) [reset = 0]

This is a test pattern register. All bits default to 0 after reset.

Figure 59. Register 25h

D15	D14	D13	D12	D11	D10	D9	D8
HARD_SYNC_TP	PRBS_SEED_FROM_REG	PRBS_MODE_2	PRBS_TP_EN	X			TP_SOFT_SYNC
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			R/W-0
D7	D6	D5	D4	D3	D2	D1	D0
X	EN_RAMP	DUAL_CUSTOM_PAT	SINGLE_CUSTOM_PAT	BITS_CUSTOM2[13:12]		BITS_CUSTOM1[13:12]	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	

Table 16. Register 25h Field Descriptions

Bit	Field	Type	Reset	Description
D15	HARD_SYNC_TP	R/W	0	Sync test pattern selection 0 = Inactive 1 = External SYNC feature enabled for syncing test patterns
D14	PRBS_SEED_FROM_REG	R/W	0	PRBS seed selection 0 = Disabled 1 = Selection of PRBS seed from registers 23h and 24h enabled
D13	PRBS_MODE_2	R/W	0	PRBS mode selection This bit sets the PRBS mode of the 9-bit LFSR (the 23-bit LFSR is default).
D12	PRBS_TP_EN	R/W	0	PRBS test pattern selection 0 = PRBS test pattern disabled 1 = PRBS test pattern enable bit
D11-D9	X	R/W	0	Don't care bits
D8	TP_SOFT_SYNC	R/W	0	Test pattern software sync 0 = No sync 1 = Software sync bit for test patterns on all eight channels
D7	X	R/W	0	Don't care bit
D6	EN_RAMP	R/W	0	Ramp pattern enable 0 = Normal operation 1 = Enables a repeating full-scale ramp pattern on the outputs. Ensure that bits D4 and D5 are 0.
D5	DUAL_CUSTOM_PAT	R/W	0	Output toggles between two codes 0 = Normal operation 1 = Enables mode where the output toggles between two defined codes. Ensure that bits D4 and D6 are 0.
D4	SINGLE_CUSTOM_PAT	R/W	0	Output is defined code 0 = Normal operation 1 = Enables mode where the output is a constant specified code. Ensure that bits D5 and D6 are 0.
D3-D2	BITS_CUSTOM2[13:12]	R/W	0	MSB selection for dual patterns These bits determine two MSBs for the second code of the dual custom patterns.

Table 16. Register 25h Field Descriptions (continued)

Bit	Field	Type	Reset	Description
D1-D0	BITS_CUSTOM1[13:12]	R/W	0	MSB selection for single patterns These bits define two MSBs for the single custom pattern (and for the first code of the dual custom patterns).

7.6.1.11 Register 26h (offset = 26h) [reset = 0]

This is a test pattern register.

Figure 60. Register 26h

D15	D14	D13	D12	D11	D10	D9	D8
BITS_CUSTOM1[9:0]							
R/W-0							
D7	D6	D5	D4	D3	D2	D1	D0
BITS_CUSTOM1[9:0]		X					
R/W-0		R/W-0					

Table 17. Register 26h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D6	BITS_CUSTOM1[9:0]	R/W	0	Lower single custom pattern bits These bits determine the 10 lower bits for the single custom pattern (and the first code of the dual custom pattern).
D5-D0	X	R/W	0	Don't care bits

7.6.1.12 Register 27h (offset = 27h) [reset = 0]

This is a test pattern register.

Figure 61. Register 27h

D15	D14	D13	D12	D11	D10	D9	D8
BITS_CUSTOM2[9:0]							
R/W-0							
D7	D6	D5	D4	D3	D2	D1	D0
BITS_CUSTOM2[9:0]		X					
R/W-0		R/W-0					

Table 18. Register 27h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D6	BITS_CUSTOM2[9:0]	R/W	0	Lower dual custom pattern bits These bits determine the 10 lower bits for the second code of the dual custom pattern.
D5-D0	X	R/W	0	Don't care bits

7.6.1.13 Register 28h (offset = 28h) [reset = 0]

This is an output interface mode register. All bits default to 0 after reset.

Figure 62. Register 28h

D15	D14	D13	D12	D11	D10	D9	D8
EN_BITORDER	X						BIT_WISE
R/W-0	R/W-0						R/W-0
D7	D6	D5	D4	D3	D2	D1	D0
EN_WORDWISE_BY_CH[7:0]							
R/W-0							

Table 19. Register 28h Field Descriptions

Bit	Field	Type	Reset	Description
D15	EN_BITORDER	R/W	0	Bit order enable(1) This bit enables the bit order output in two-lane mode. 0 = Byte-wise 1 = Word-wise
D14-D9	X	R/W	0	Don't care bit
D8	BIT_WISE	R/W	0	Bit- or byte-wise selection This bit selects between byte-wise and bit-wise format. 0 = Byte-wise, the upper bits come are on one lane and the lower bits are on other lane 1 = Bit-wise, the odd bits come out on one lane and the even bits come out on other lane
D7-D0	EN_WORDWISE_BY_CH[7:0]	R/W	0	Word-wise enable with channels 7 to 0 0 = Data comes out in two-lane mode with the upper set of bits on one channel and the lower set of bits on the other channel 1 = Output format is one sample on one LVDS lane with the next sample on the other LVDS lane

(1) This bit must set 1 to enable bits D[8:0].

7.6.1.14 Register 29h (offset = 29h) [reset = 0]

This is a digital filter mode register. All bits default to 0 after reset.

Figure 63. Register 29h

D15	D14	D13	D12	D11	D10	D9	D8
X							
R/W-0							
D7	D6	D5	D4	D3	D2	D1	D0
X						GLOBAL_EN_FILTER	X
R/W-0						R/W-0	R/W-0

Table 20. Register 29h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D2	X	R/W	0	Don't care bits
D1	GLOBAL_EN_FILTER	R/W	0	Filter block enable 0 = Inactive 1 = Global control filter blocks enabled
D0	X	R/W	0	Don't care bit

7.6.1.15 Register 2Ah (offset = 2Ah) [reset = 0]

This is a digital gain mode register. All bits default to 0 after reset.

Figure 64. Register 2Ah

D15	D14	D13	D12	D11	D10	D9	D8
X				GAIN_CH2[3:0]			
R/W-0				R/W-0			
D7	D6	D5	D4	D3	D2	D1	D0
X				GAIN_CH1[3:0]			
R/W-0				R/W-0			

Table 21. Register 2Ah Field Descriptions

Bit	Field	Type	Reset	Description
D15-D12	X	R/W	0	Don't care bits
D11-D8	GAIN_CH2[3:0]	R/W	0	Channel 2 gain These bits set the programmable gain of channel 2
D7-D4	X	R/W	0	Don't care bits
D3-D0	GAIN_CH3[3:0]	R/W	0	Channel 1 gain These bits set the programmable gain of channel 1

7.6.1.16 Register 2Bh (offset = 2Bh) [reset = 0]

This is a digital gain mode register. All bits default to 0 after reset.

Figure 65. Register 2Bh

D15	D14	D13	D12	D11	D10	D9	D8
X				GAIN_CH3[3:0]			
R/W-0				R/W-0			
D7	D6	D5	D4	D3	D2	D1	D0
X				GAIN_CH4[3:0]			
R/W-0				R/W-0			

Table 22. Register 2Bh Field Descriptions

Bit	Field	Type	Reset	Description
D15-D12	X	R/W	0	Don't care bits
D11-D8	GAIN_CH3[3:0]	R/W	0	Channel 3 gain These bits set the programmable gain of channel 3
D7-D4	X	R/W	0	Don't care bits
D3-D0	GAIN_CH4[3:0]	R/W	0	Channel 4 gain These bits set the programmable gain of channel 4

7.6.1.17 Register 2Eh (offset = 2Eh) [reset = 0]

This is a digital filter mode register. All bits default to 0 after reset.

Figure 66. Register 2Eh

D15	D14	D13	D12	D11	D10	D9	D8
X	HPF_EN_CH1	HPF_CORNER _CH1[3:0]				FILTER1_COEFF_SET[2:0]	
R/W-0	R/W-0	R/W-0				R/W-0	
D7	D6	D5	D4	D3	D2	D1	D0
FILTER1_COEFF_SET[2:0]	FILTER1_RATE[2:0]			X	ODD_TAP1	X	USE_FILTER1
R/W-0	R/W-0			R/W-0	R/W-0	R/W-0	R/W-0

Table 23. Register 2Eh Field Descriptions

Bit	Field	Type	Reset	Description
D15	X	R/W	0	Don't care bit
D14	HPF_EN_CH1	R/W	0	Channel 1 HPF filter enable 0 = Disabled 1 = HPF filter enable for channel 1
D13-D10	HPF_CORNER _CH1[3:0]	R/W	0	HPF corner for channel 1 These bits set the HPF corner in values from 2k to 10k.
D9-D7	FILTER1_COEFF_SET[2:0]	R/W	0	Filter 1 coefficient set These bits select the stored coefficient set for filter 1.
D6-D4	FILTER1_RATE[2:0]	R/W	0	Filter 1 decimation factor These bits set the decimation factor for filter 2.
D3	X	R/W	0	Don't care bit
D2	ODD_TAP1	R/W	0	Filter 1 odd tap This bit uses odd tap filter 1.
D1	X	R/W	0	Don't care bit
D0	USE_FILTER1	R/W	0	Channel 1 filter 0 = Disabled 1 = Enables filter for channel 1

7.6.1.18 Register 30h (offset = 30h) [reset = 0]

This is a digital filter mode register. All bits default to 0 after reset.

Figure 67. Register 30h

D15	D14	D13	D12	D11	D10	D9	D8
X	HPF_EN_CH2	HPF_CORNER _CH2[3:0]				FILTER2_COEFF_SET[2:0]	
R/W-0	R/W-0	R/W-0				R/W-0	
D7	D6	D5	D4	D3	D2	D1	D0
FILTER2_COEFF_SET[2:0]	FILTER2_RATE[2:0]			X	ODD_TAP2	X	USE_FILTER2
R/W-0	R/W-0			R/W-0	R/W-0	R/W-0	R/W-0

Table 24. Register 30h Field Descriptions

Bit	Field	Type	Reset	Description
D15	X	R/W	0	Don't care bit
D14	HPF_EN_CH2	R/W	0	Channel 2 HPF filter enable 0 = Disabled 1 = HPF filter enable for channel 2
D13-D10	HPF_CORNER _CH2[3:0]	R/W	0	HPF corner for channel 2 These bits set the HPF corner in values from 2k to 10k.
D9-D7	FILTER2_COEFF_SET[2:0]	R/W	0	Filter 2 coefficient set These bits select the stored coefficient set for filter 2.
D6-D4	FILTER2_RATE[2:0]	R/W	0	Filter 2 decimation factor These bits set the decimation factor for filter 2.
D3	X	R/W	0	Don't care bit
D2	ODD_TAP2	R/W	0	Filter 2 odd tap This bit uses odd tap filter 2.
D1	X	R/W	0	Don't care bit
D0	USE_FILTER2	R/W	0	Channel 2 filter 0 = Disabled 1 = Enables filter for channel 2

7.6.1.19 Register 33h (offset = 33h) [reset = 0]

This is a digital filter mode register. All bits default to 0 after reset.

Figure 68. Register 33h

D15	D14	D13	D12	D11	D10	D9	D8
X	HPF_EN_CH3	HPF_CORNER _CH3[3:0]				FILTER3_COEFF_SET[2:0]	
R/W-0	R/W-0	R/W-0				R/W-0	
D7	D6	D5	D4	D3	D2	D1	D0
FILTER3_COEFF_SET[2:0]	FILTER3_RATE[2:0]			X	ODD_TAP3		USE_FILTER3
R/W-0	R/W-0			R/W-0	R/W-0	R/W-0	

Table 25. Register 33h Field Descriptions

Bit	Field	Type	Reset	Description
D15	X	R/W	0	Don't care bit
D14	HPF_EN_CH3	R/W	0	Channel 3 HPF filter enable 0 = Disabled 1 = HPF filter enable for channel 3
D13-D10	HPF_CORNER _CH3[3:0]	R/W	0	HPF corner for channel 3 These bits set the HPF corner in values from 2k to 10k.
D9-D7	FILTER3_COEFF_SET[2:0]	R/W	0	Filter 3 coefficient set These bits select the stored coefficient set for filter 3.
D6-D4	FILTER3_RATE[2:0]	R/W	0	Filter 3 decimation factor These bits set the decimation factor for filter 3.
D3	X	R/W	0	Don't care bit
D2	ODD_TAP3	R/W	0	Filter 3 odd tap This bit uses odd tap filter 3.
D1	X	R/W	0	Don't care bit
D0	USE_FILTER3	R/W	0	Channel 3 filter 0 = Disabled 1 = Enables filter for channel 3

7.6.1.20 Register 35h (offset = 35h) [reset = 0]

This is a digital filter mode register. All bits default to 0 after reset.

Figure 69. Register 35h

D15	D14	D13	D12	D11	D10	D9	D8
X	HPF_EN_CH4	HPF_CORNER _CH4[3:0]				FILTER4_COEFF_SET[2:0]	
R/W-0	R/W-0	R/W-0				R/W-0	
D7	D6	D5	D4	D3	D2	D1	D0
FILTER4_COEFF_SET[2:0]	FILTER4_RATE[2:0]			X	ODD_TAP4	X	USE_FILTER4
R/W-0	R/W-0			R/W-0	R/W-0	R/W-0	R/W-0

Table 26. Register 35h Field Descriptions

Bit	Field	Type	Reset	Description
D15	X	R/W	0	Don't care bit
D14	HPF_EN_CH4	R/W	0	Channel 4 HPF filter enable 0 = Disabled 1 = HPF filter enable for channel 4
D13-D10	HPF_CORNER _CH4[3:0]	R/W	0	HPF corner for channel 4 These bits set the HPF corner in values from 2k to 10k.
D9-D7	FILTER4_COEFF_SET[2:0]	R/W	0	Filter 4 coefficient set These bits select the stored coefficient set for filter 4.
D6-D4	FILTER4_RATE[2:0]	R/W	0	Filter 4 decimation factor These bits set the decimation factor for filter 4.
D3	X	R/W	0	Don't care bit
D2	ODD_TAP4	R/W	0	Filter 4 odd tap This bit uses odd tap filter 4.
D1	X	R/W	0	Don't care bit
D0	USE_FILTER4	R/W	0	Channel 4 filter 0 = Disabled 1 = Enables filter for channel 4

7.6.1.21 Register 38h (offset = 38h) [reset = 0x0000]

This is an output interface mode register.

Figure 70. Register 38h

D15	D14	D13	D12	D11	D10	D9	D8
X							
R/W-							
D7	D6	D5	D4	D3	D2	D1	D0
X						DATA_RATE[1:0]	
R/W-						R/W-	

Table 27. Register 38h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D2	X	R/W	0	Don't care bits
D1-D0	DATA_RATE[1:0]	R/W	0	Clock rate selection These bits select the output frame clock rate. (Default = 0)

7.6.1.22 Register 42h (offset = 42h) [reset = 0]

This is an output interface mode register.

Figure 71. Register 42h

D15	D14	D13	D12	D11	D10	D9	D8
EN_REF_VCM 0	X						
R/W-0	R/W-0						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	PHASE_DDR[1:0]		X	EN_REF_VCM 1	X		
R/W-0	R/W-0		R/W-0	R/W-0	R/W-0		

Table 28. Register 42h Field Descriptions

Bit	Field	Type	Reset	Description
D15	EN_REF_VCM0	R/W	0	To enable the external reference mode, the EN_EXT_REF register bit (register F0h) must be set to 1. 00 = In external reference mode, apply the reference on the REFT, REFB pins 01, 10 = Don't use 11 = In external reference mode, apply the reference on the VCM pin
D14-D7	X	R/W	0	Don't care bits
D6-D5	PHASE_DDR[1:0]	R/W	0	These bits control the LCLK output phase relative to data. (Default = 10)
D4	X	R/W	0	Don't care bit
D3	EN_REF_VCM1	R/W	0	To enable the external reference mode, the EN_EXT_REF register bit (register F0h) must be set to 1. 00 = In external reference mode, apply the reference on the REFT, REFB pins 01, 10 = Don't use 11 = In external reference mode, apply the reference on the VCM pin
D2-D0	X	R/W	0	Don't care bits

7.6.1.23 Register 45h (offset = 45h) [reset = 0]

This is a test pattern register. All bits default to 0 after reset.

Figure 72. Register 45h

D15	D14	D13	D12	D11	D10	D9	D8
X							
R/W-0							
D7	D6	D5	D4	D3	D2	D1	D0
X						PAT_SYNC	PAT_DESKEW
R/W-0						R/W-0	R/W-0

Table 29. Register 45h Field Descriptions

Bit	Field	Type	Reset	Description
D15-D2	X	R/W	0	Don't care bits
D1	PAT_SYNC	R/W	0	Sync pattern enable 0 = Inactive 1 = Sync pattern mode enabled; ensure that D0 is 0
D0	PAT_DESKEW	R/W	0	Deskew pattern enable 0 = Inactive 1 = Deskew pattern mode enabled; ensure that D1 is 0

7.6.1.24 Register 46h (offset = 46h) [reset = 0]

This is an output interface mode register. All bits default to 0 after reset.

Figure 73. Register 46h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 46	X	FALL_SDR	X	EN_16BIT	EN_14BIT	EN_12BIT	X
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
D7	D6	D5	D4	D3	D2	D1	D0
X			EN_SDR	MSB_FIRST	BTC_MODE	X	EN_2LANE
R/W-0			R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 30. Register 46h Field Descriptions

Bit	Field	Type	Reset	Description
D15	ENABLE 46	R/W	0	Enable register 46(1) This bit enables register 46.
D14	X	R/W	0	Don't care bit
D13	FALL_SDR	R/W	0	SDR output mode 0 = At data window edge 1 = The LCLK rising or falling edge control comes in the middle of the data window when operating in SDR output mode
D12	X	R/W	0	Don't care bit
D11	EN_16BIT	R/W	0	16-bit mode enable 0 = Inactive 1 = 16-bit serialization mode enabled; ensure bits D[10:9] are 0

(1) This bit must be set to 1 to enable bits D[13:0].

Table 30. Register 46h Field Descriptions (continued)

Bit	Field	Type	Reset	Description
D10	EN_14BIT	R/W	0	14-bit mode enable 0 = Inactive 1 = 14-bit serialization mode enabled; ensure bits D11 and D9 are 0
D9	EN_12BIT	R/W	0	12-bit mode enable 0 = Inactive 1 = 12-bit serialization mode enabled; ensure bits D[11:10] are 0
D8-D5	X	R/W	0	Don't care bits
D4	EN_SDR	R/W	0	Bit clock selection 0 = DDR bit clock 1 = SDR bit clock
D3	MSB_FIRST	R/W	0	MSB first selection 0 = LSB first 1 = MSB first
D2	BTC_MODE	R/W	0	Binary mode selection 0 = Binary offset (ADC data output format) 1 = Binary twos complement (ADC data output format)
D1	X	R/W	0	Don't care bit
D0	EN_2LANE	R/W	0	LVDS output lane selection 0 = One-lane LVDS output 1 = Two-lane LVDS output

7.6.1.25 Register 50h (offset = 50h) [reset = 0]

This is a programmable LVDS mapping mode register. All bits default to 0 after reset.

Figure 74. Register 50h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 50	X						
R/W-0	R/W-0						
D7	D6	D5	D4	D3	D2	D1	D0
MAP_CH12_TO_OUT1B[3:0]				MAP_CH12_TO_OUT1A[3:0]			
R/W-0				R/W-0			

Table 31. Register 50h Field Descriptions

Bit	Field	Type	Reset	Description
D15	ENABLE 50	R/W	0	Enable for register 50h(1) This bit enables register 50h.
D14-D8	X	R/W	0	Don't care bits
D7-D4	MAP_CH12_TO_OUT1B[3:0]	R/W	0	OUT1B pin to channel mapping These bits select the OUT1B pin pair to channel data mapping.
D3-D0	MAP_CH12_TO_OUT1A[3:0]	R/W	0	OUT1A pin to channel mapping These bits select the OUT1A pin pair to channel data mapping.

(1) This bit must be set to 1 to enable bits D[7:0].

7.6.1.26 Register 51h (offset = 51h) [reset = 0]

This is a programmable LVDS mapping mode register. All bits default to 0 after reset.

Figure 75. Register 51h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 51	X			MAP_CH12_TO_OUT2B[3:0]			
R/W-0	R/W-0			R/W-0			
D7	D6	D5	D4	D3	D2	D1	D0
MAP_CH12_TO_OUT2A[3:0]				X			
R/W-0				R/W-0			

Table 32. Register 51h Field Descriptions

Bit	Field	Type	Reset	Description
D15	ENABLE 51	R/W	0	Enable for register 51h(1) This bit enables register 51h.
D14-D12	X	R/W	0	Don't care bits
D11-D8	MAP_CH12_TO_OUT2B[3:0]	R/W	0	OUT2B pin to channel mapping These bits select the OUT2B pin pair to channel data mapping.
D7-D4	MAP_CH12_TO_OUT2A[3:0]	R/W	0	OUT2A pin to channel mapping These bits select the OUT2A pin pair to channel data mapping.
D3-D0	X	R/W	0	Don't care bits

(1) This bit must be set to 1 to enable bits D[7:0].

7.6.1.27 Register 53h (offset = 53h) [reset = 0]

This is a programmable LVDS mapping mode register. All bits default to 0 after reset.

Figure 76. Register 53h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 53	X			MAP_CH34_TO_OUT3B[3:0]			
R/W-0	R/W-0			R/W-0			
D7	D6	D5	D4	D3	D2	D1	D0
X							
R/W-0							

Table 33. Register 53h Field Descriptions

Bit	Field	Type	Reset	Description
D15	ENABLE 53	R/W	0	Enable register 53h(1) This bit enables register 53h.
D14-D12	X	R/W	0	Don't care bits
D11-D8	MAP_CH34_TO_OUT3B[3:0]	R/W	0	OUT3B pin to channel mapping These bits select the OUT3B pin pair to channel data mapping.
D7-D0	X	R/W	0	Don't care bits

(1) This bit must be set to 1 to enable bits D[7:0].

7.6.1.28 Register 54h (offset =) [reset = 0]

This is a programmable LVDS mapping mode register. All bits default to 0 after reset.

Figure 77. Register 54h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 54	X						
R/W-0	R/W-0						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X				MAP_Ch34_to_OUT3A[3:0]			
R/W-0				R/W-0			

Table 34. Register 54h Field Descriptions

Bit	Field	Type	Reset	Description
D15	ENABLE 54	R/W	0	Enable register 54h(1) This bit enables register 54h.
D14-D4	X	R/W	0	Don't care bits
D3-D0	MAP_Ch34_to_OUT3A[3:0]	R/W	0	OUT3A pin to channel mapping These bits select the OUT3A pin pair to channel data mapping.

(1) This bit must be set to 1 to enable bits D[7:0].

7.6.1.29 Register 55h (offset = 55h) [reset = 0]

This is a programmable LVDS mapping mode register. All bits default to 0 after reset.

Figure 78. Register 55h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 55	X						
R/W-0	R/W-0						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MAP_CH34_TO_OUT4A[3:0]				MAP_CH34_TO_OUT4B[3:0]			
R/W-0				R/W-0			

Table 35. Register 55h Field Descriptions

Bit	Field	Type	Reset	Description
D15	ENABLE 55	R/W	0	Enable register 55h(1) This bit enables register 55h.
D14-D8	X	R/W	0	Don't care bits
D7-D4	MAP_CH34_TO_OUT4A[3:0]	R/W	0	OUT4A pin to channel mapping These bits select the OUT4A pin pair to channel data mapping.
D3-D0	MAP_CH34_TO_OUT4B[3:0]	R/W	0	OUT4B pin to channel mapping These bits select the OUT4B pin pair to channel data mapping.

(1) This bit must be set to 1 to enable bits D[7:0].

7.6.1.30 Register F0h (offset = F0h) [reset = 0]

This is a general register.

NOTE

The EN_HIGH_ADDRS bit (register 01h, bit D4) must be set to 1 in order to access this register.

Figure 79. Register F0h

D15	D14	D13	D12	D11	D10	D9	D8
EN_EXT_REF	X						
R/W-0	R/W-0						
D7	D6	D5	D4	D3	D2	D1	D0
X							
R/W-0							

Table 36. Register F0h Field Descriptions

Bit	Field	Type	Reset	Description
D15	EN_EXT_REF	R/W	0	Reference mode selection 0 = Internal reference mode enabled (default) 1 = External reference mode enabled. The voltage reference can be applied on either the REFP and REFB pins or the VCM pin.
D7-D0	X	R/W	0	Don't care bits

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The VSP5324-Q1 device is a low power 12-bit, 4-channel ADC customized for time-of-flight applications. The device accepts four single-ended or differential analog inputs and can be configured to output the digitized data on 4 or 8 LVDS lanes as per the requirements of the external host receiver. The sampling clock can be fed to the device using a single-ended or a differential signal. High-speed sampling rates of up to 80 MSPS can be used to speed up the sensor readout and therefore use longer sensor exposure times without taking a hit on the frame-rate. The device is controlled using a simple 4-wire SPI. Power constrained systems can additionally make use of the power-down pin (PD) to take the device quickly in and out of low-power mode. The device uses an internal reference and internal common-mode voltage by default and has a provision for the use of external reference and external common-mode voltage inputs.

8.2 Typical Application

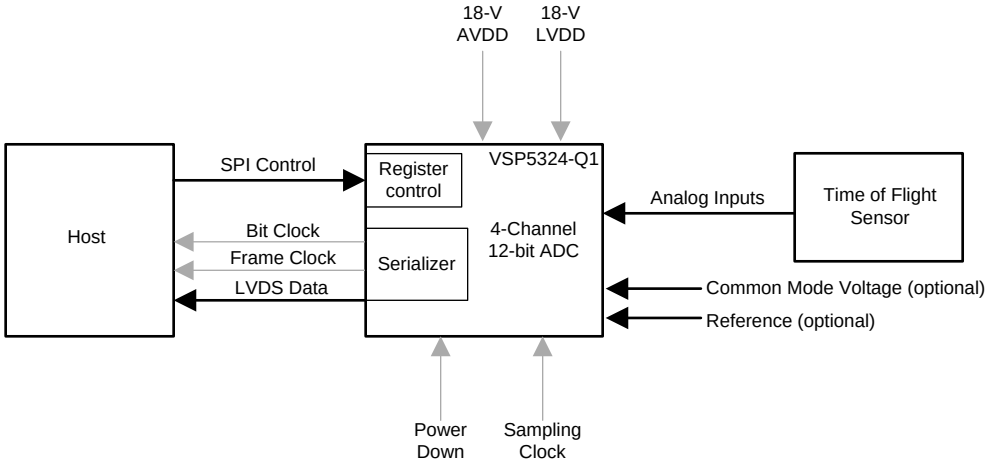


Figure 80. Application Schematic

8.2.1 Design Requirements

For optimum performance, the analog inputs must be driven differentially. If the inputs are driven in a single-ended manner, capacitors must be placed on the INx_M signals and close to the INx_M pins. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitics. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

8.2.2 Detailed Design Procedure

8.2.2.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially, as shown in Figure 81. This architecture improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitic. The drive circuit shows an R-C filter across the analog input pins. The purpose of the filter is to absorb glitches caused by the sampling capacitors opening and closing.

Typical Application (continued)

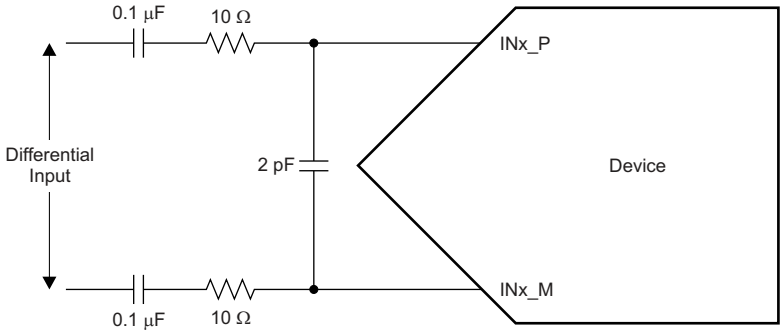


Figure 81. Analog Input Drive Circuit

8.2.2.2 Clock Input

The VSP5324-Q1 device can function with either single-ended or differential clock inputs. The device can automatically detect if a single-ended or differential clock is applied. To operate with a single-ended input clock, CLKP must be driven by a CMOS clock with CLKM tied to GND. Figure 82 and Figure 83 show the typical single-ended and differential clock termination schemes (respectively).

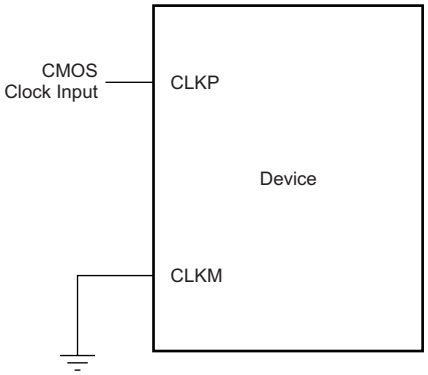
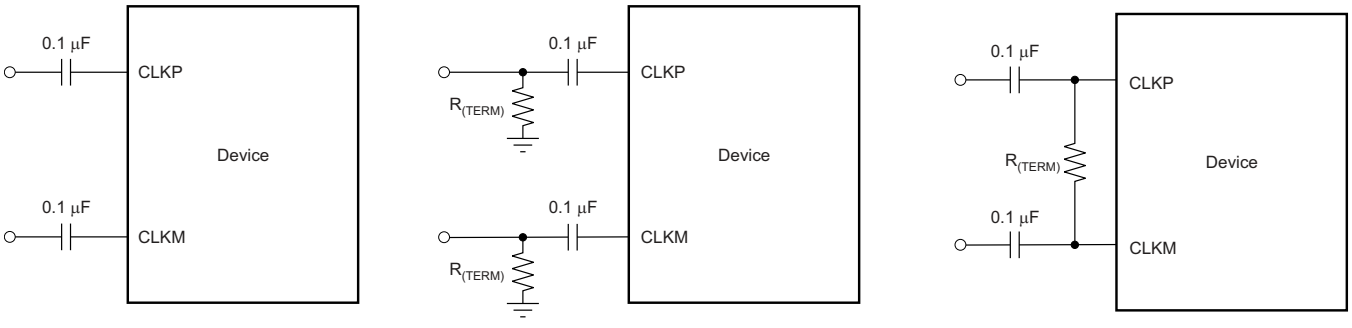


Figure 82. Single-Ended Clock Driving Circuit



a) Differential Sine-Wave Clock Input

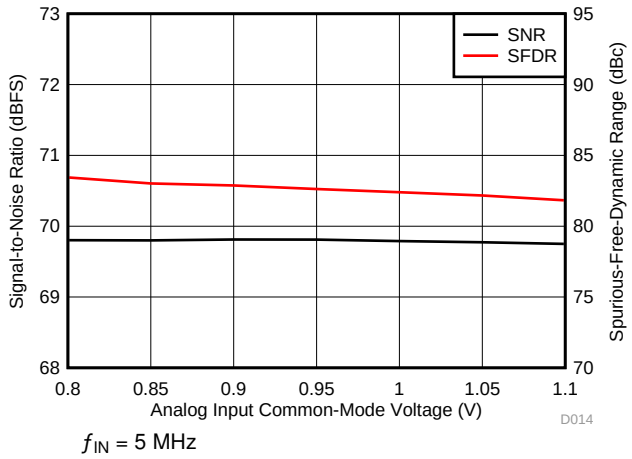
b) Differential LVPECL Clock Input

c) Differential LVDS Clock Input

Figure 83. Differential Clock Driving Circuit

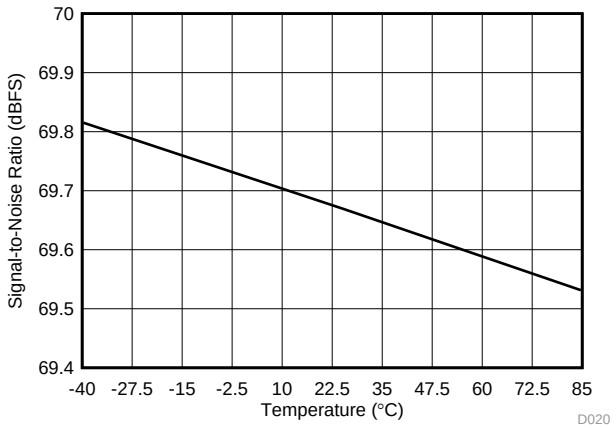
Typical Application (continued)

8.2.3 Application Curves



f_{IN} = 5 MHz

Figure 84. Performance vs Input Common-Mode



A 0.7-V_{PP} 5-MHz sine-wave input is applied on the INx_P pin
The INx_M pin is connected to the device VCM pin

Figure 85. SNR vs Temperature For Single-Ended Input

9 Power Supply Recommendations

Using an LDO supply with minimal noise on the AVDD supply is recommended. The LVDD supply can be connected to an LDO or a DC-DC converter. A capacitor with a value of 100 nF per supply pin is recommended in addition to a 1-µF common decoupling capacitor per rail.

10 Layout

10.1 Layout Guidelines

10.1.1 General Guidelines

The following list includes general layout guidelines. Refer to Figure 86 as needed.

- Route the clock input as a differential pair when a differential clock input is used.
- When single ended inputs are used, place 100-nF capacitors close to the pins on the INx_M inputs to ensure that the reference rail is stable. When differential inputs are used, the inputs must be routed as differential pairs.
- Route the LVDS clock and data output pairs with 100-Ω differential impedance and length matched as per the sampling frequency.

10.1.2 Grounding

A single ground plane is sufficient to provide good performance, provided that the analog, digital, and clock sections of the board are cleanly partitioned.

10.1.3 Supply Decoupling

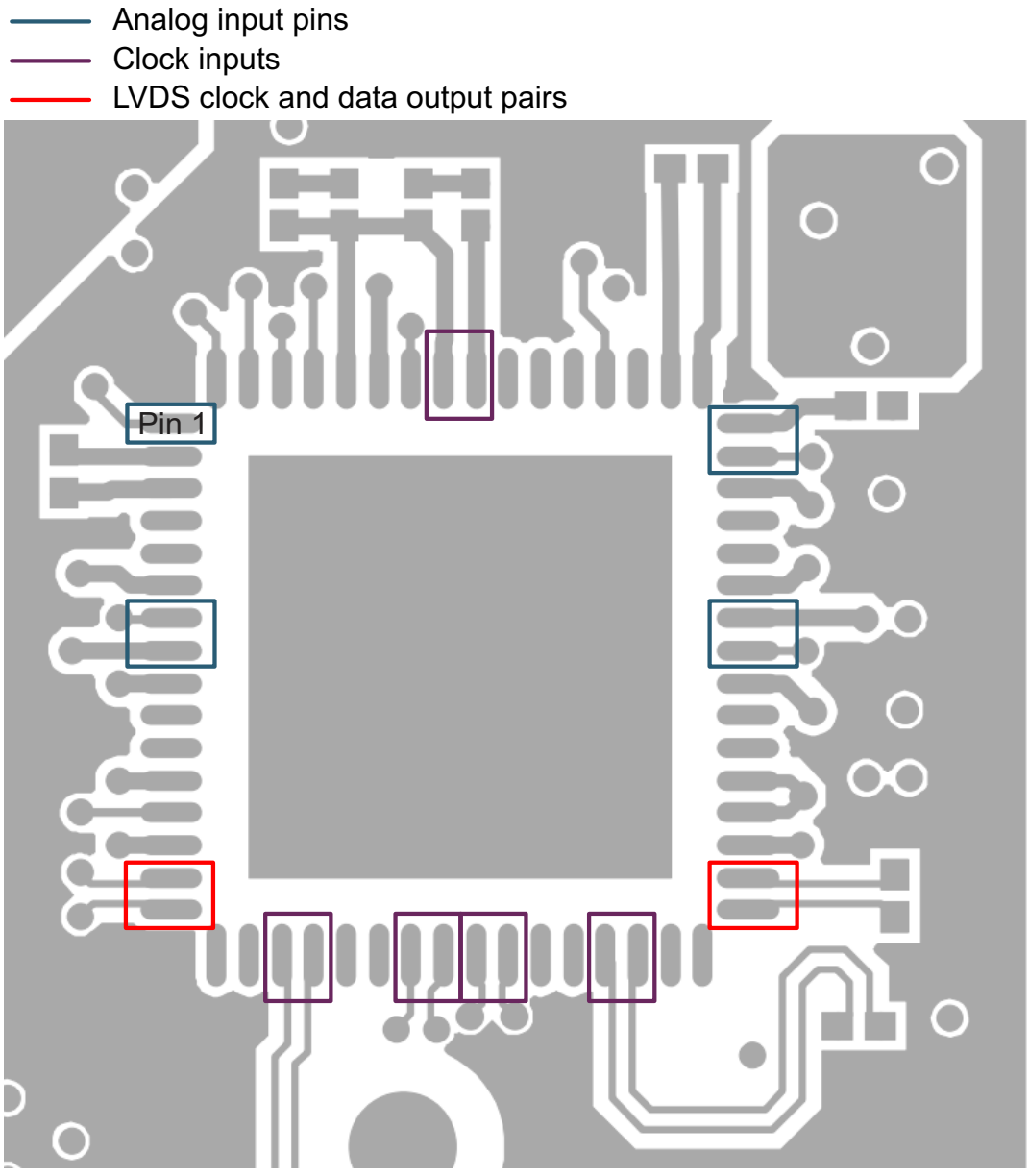
Minimal external decoupling can be used without loss in performance because the VSP5324-Q1 device already includes internal decoupling. Note that decoupling capacitors can help filter external power-supply noise, thus the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

Layout Guidelines (continued)

10.1.4 Exposed Pad

In addition to providing a path for heat dissipation, the pad is also electrically connected to the digital ground internally. Therefore, soldering the exposed pad to the ground plane is necessary to achieve the best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* and *QFN/SON PCB Attachment*.

10.2 Layout Example



The layout in this example uses four single-ended inputs and four LVDS-data outputs. The components that require special layout attention are shown and are listed in the *General Guidelines* section. For the two-lane output option, eight LVDS data pairs are used.

Figure 86. VSP5324-Q1 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Analog bandwidth The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture delay The delay in time between the input sampling clock rising edge and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture uncertainty (jitter) The sample-to-sample variation in aperture delay.

Clock pulse width and duty cycle The clock signal duty cycle is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum conversion rate The maximum sampling rate at which the specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum conversion rate The minimum sampling rate at which the ADC functions.

Differential nonlinearity (DNL) An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral nonlinearity (INL) INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function, measured in units of LSBs.

Gain error Gain error is the deviation of the ADC actual input full-scale range from its ideal value. Gain error is given as a percentage of the ideal input full-scale range and has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as $E_{G(REF)}$ and $E_{G(CHAN)}$. To a first-order approximation, the total gain error is (E_{tot} ~ $E_{G(REF)}$ + $E_{G(CHAN)}$). For example, if E_{tot} = ±0.5%, the full-scale input varies from [(1 – 0.5 / 100) × $f_{S(ideal)}$] to [(1 + 0.5 / 100) × $f_{S(ideal)}$].

Offset error Offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature drift The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum parameter deviation across the T_{MIN} to T_{MAX} range by the difference of $T_{MAX} – T_{MIN}$.

Signal-to-noise ratio (SNR) SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first nine harmonics. SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

$$SNR = 10\ Log^{10} \frac{P_S}{P_N} \quad (3)$$

Signal-to-noise and distortion (SINAD) SINAD is the ratio of the power of the fundamental (P_S) to the power of all other spectral components including noise (P_N) and distortion ($P_{(HD)}$), but excluding dc. SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

$$SINAD = 10\ Log^{10} \frac{P_S}{P_N + P_{(HD)}} \quad (4)$$

Device Support (continued)

Effective number of bits (ENOB) ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (5)$$

Total harmonic distortion (THD) THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics ($P_{(HD)}$). THD is typically given in units of dBc (dB to carrier).

$$\text{THD} = 10\ \text{Log}^{10}\frac{P_S}{P_N} \quad (6)$$

Spurious-free dynamic range (SFDR) The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-tone intermodulation distortion (IMD3) IMD3 is the ratio of the power of the fundamental (at frequencies $f1$ and $f2$) to the power of the worst spectral component at either frequency ($2\ f1 - f2$ or $2\ f2 - f1$). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC power-supply rejection ratio (DC PSRR) DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC power-supply rejection ratio (ac PSRR) AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If $\Delta V_{(AVDD)}$ is the change in supply voltage and ΔV_O is the resultant change of the ADC output code (referred to input), then:

$$\text{PSRR} = 20\ \text{Log}^{10}\frac{\Delta V_O}{\Delta V_{(AVDD)}} \quad \text{(Expressed in dBc)} \quad (7)$$

Voltage overload recovery The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This recovery is tested by separately applying a sine-wave signal with a 6-dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-mode rejection ratio (CMRR) CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{IC} is the change in the common-mode voltage of the input pins and ΔV_O is the resulting change of the ADC output code (referred to input), then:

$$\text{CMRR} = 20\ \text{Log}^{10}\frac{\Delta V_O}{\Delta V_{IC}} \quad \text{(Expressed in dBc)} \quad (8)$$

Crosstalk (only for multichannel ADCs) Crosstalk is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *QFN Layout Guidelines*
- *QFN/SON PCB Attachment*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP5324TRGCRQ1	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	VSP5324T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

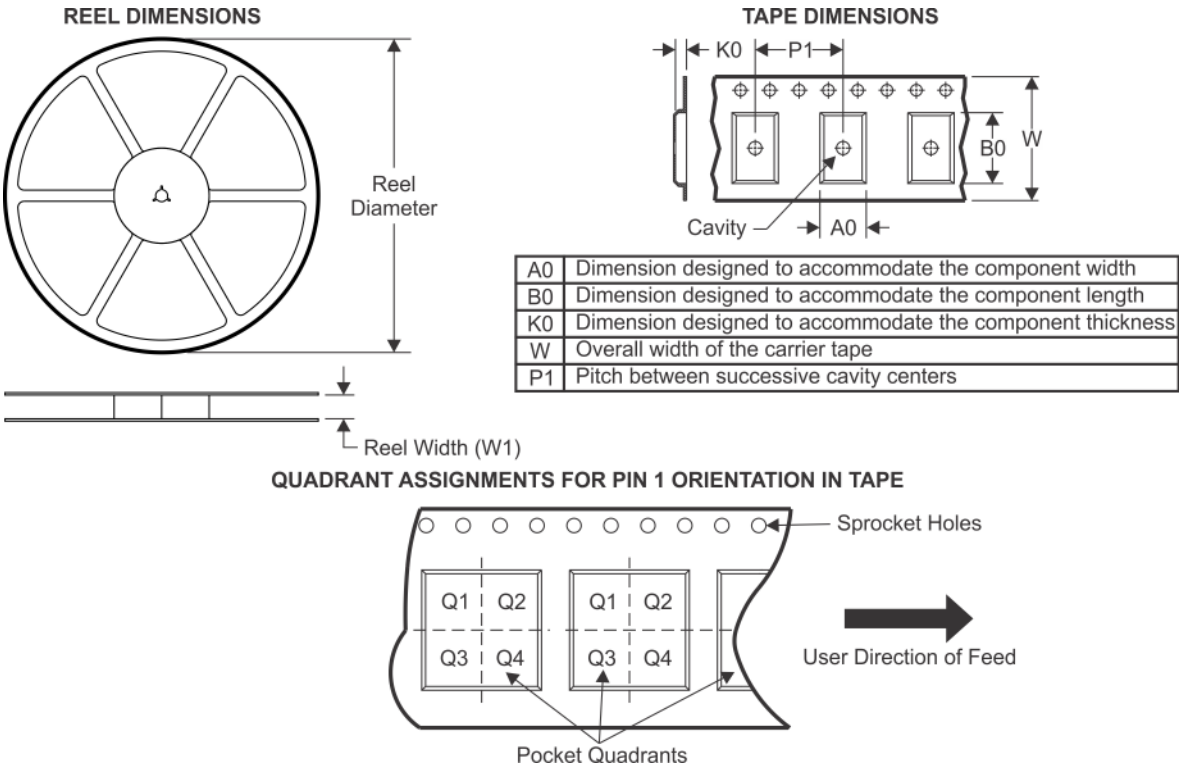
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

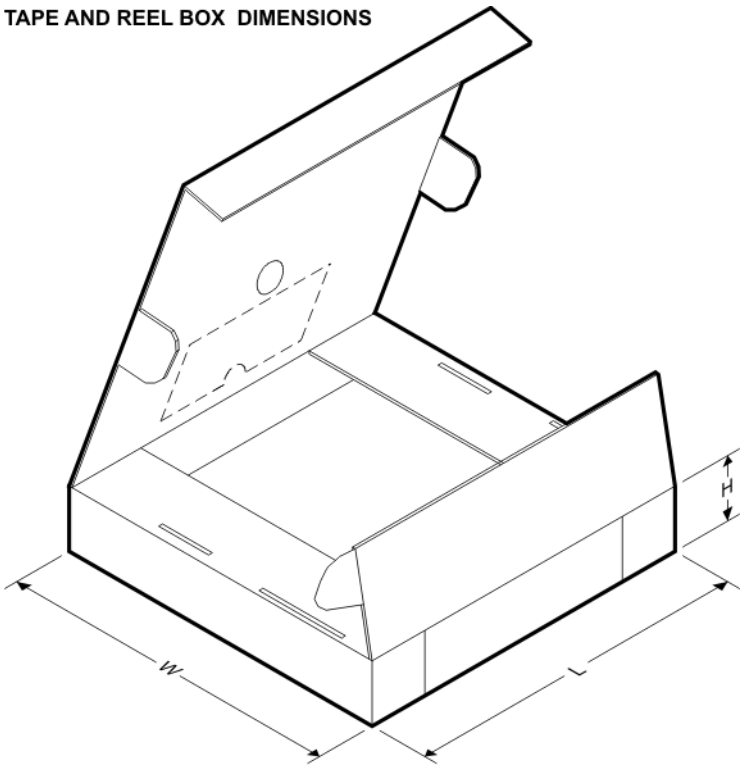


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP5324TRGCRQ1	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP5324TRGCRQ1	VQFN	RGC	64	2000	350.0	350.0	43.0

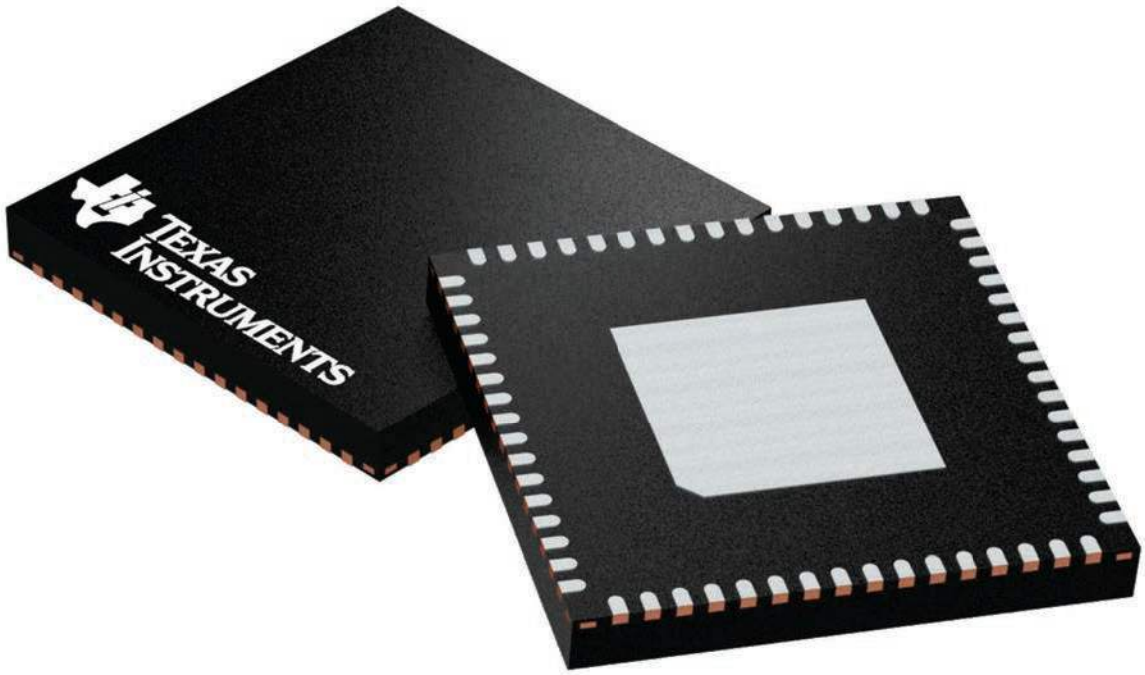
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

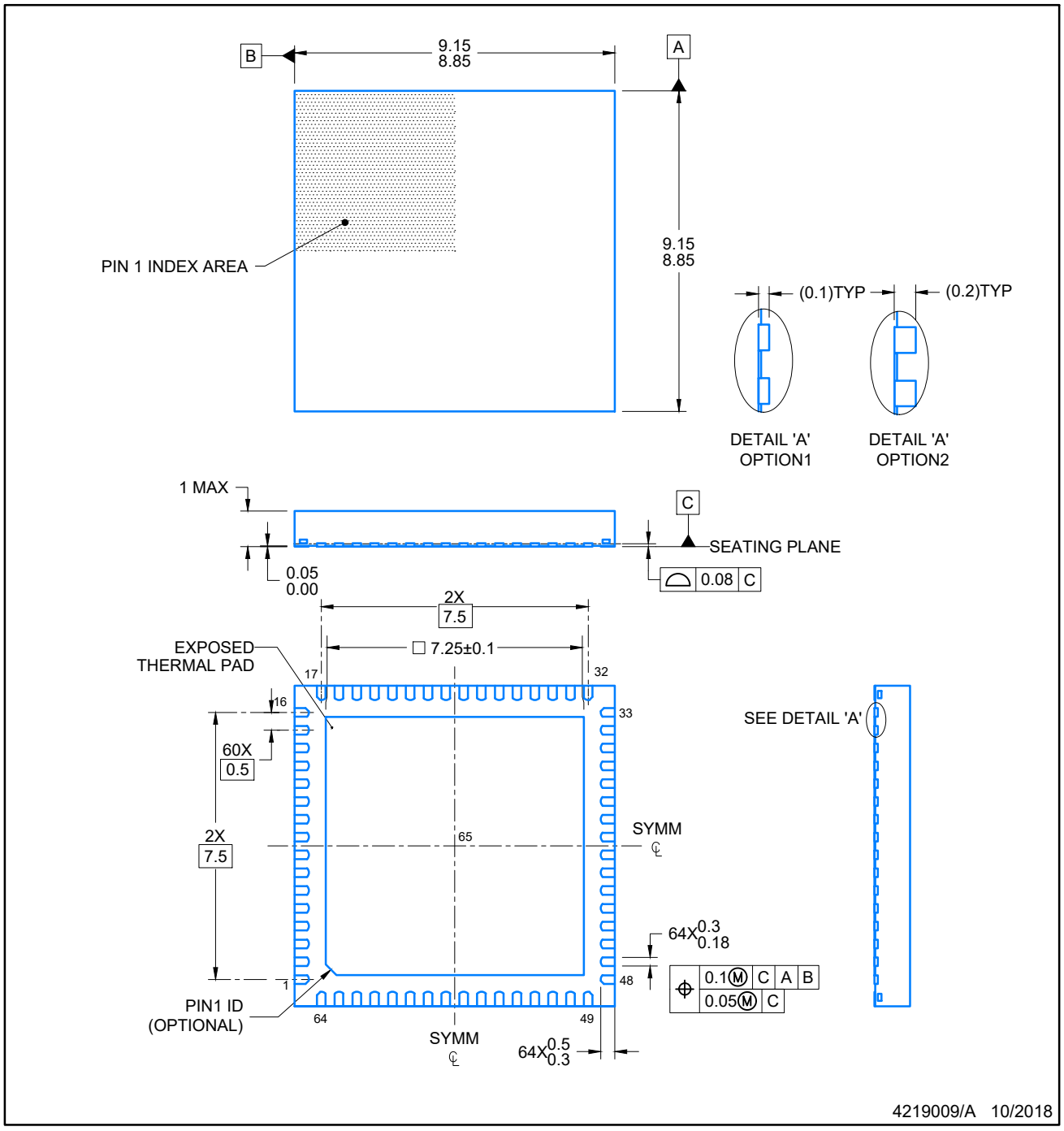
4224597/A

PACKAGE OUTLINE

RGC0064A

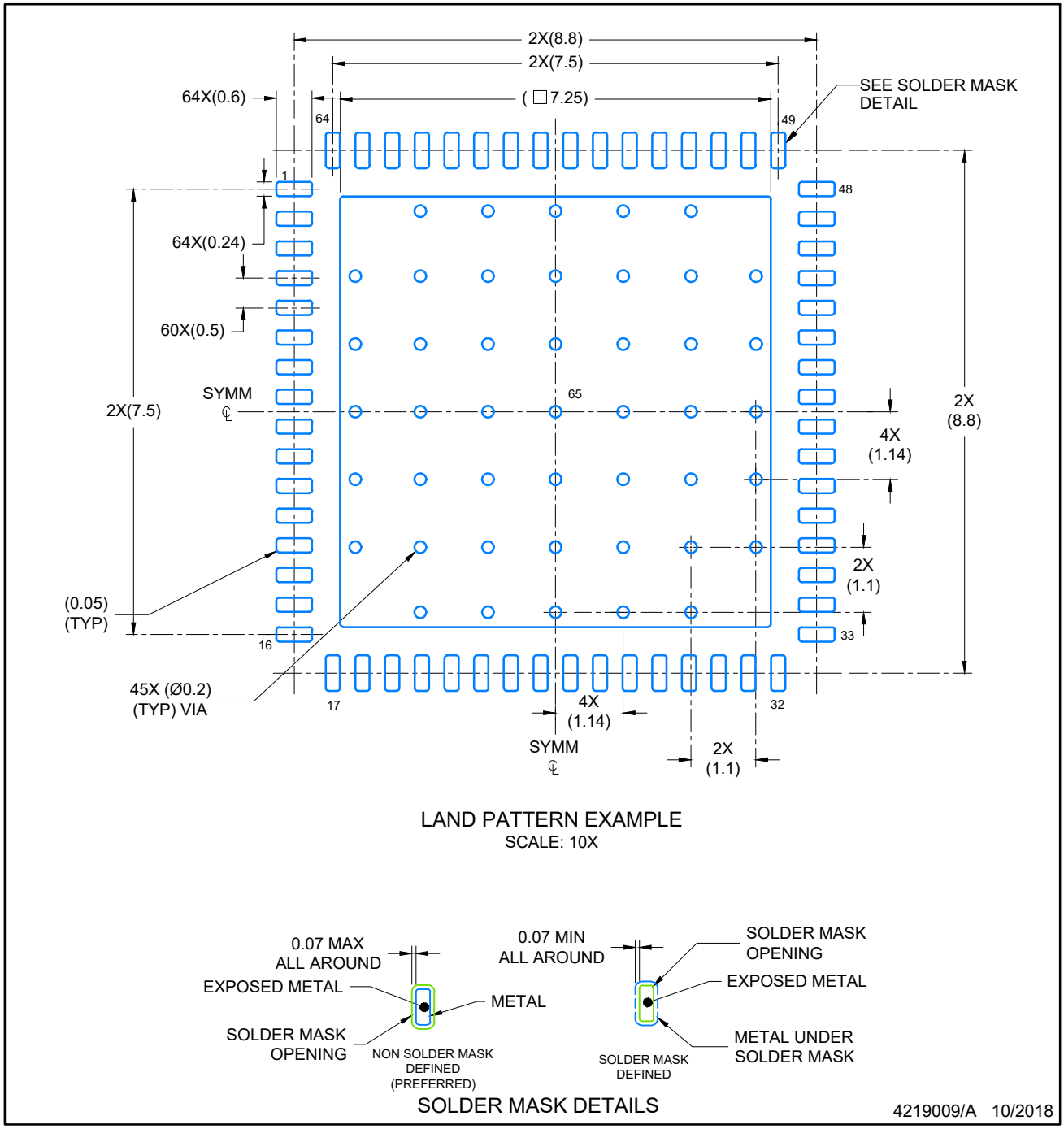
VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

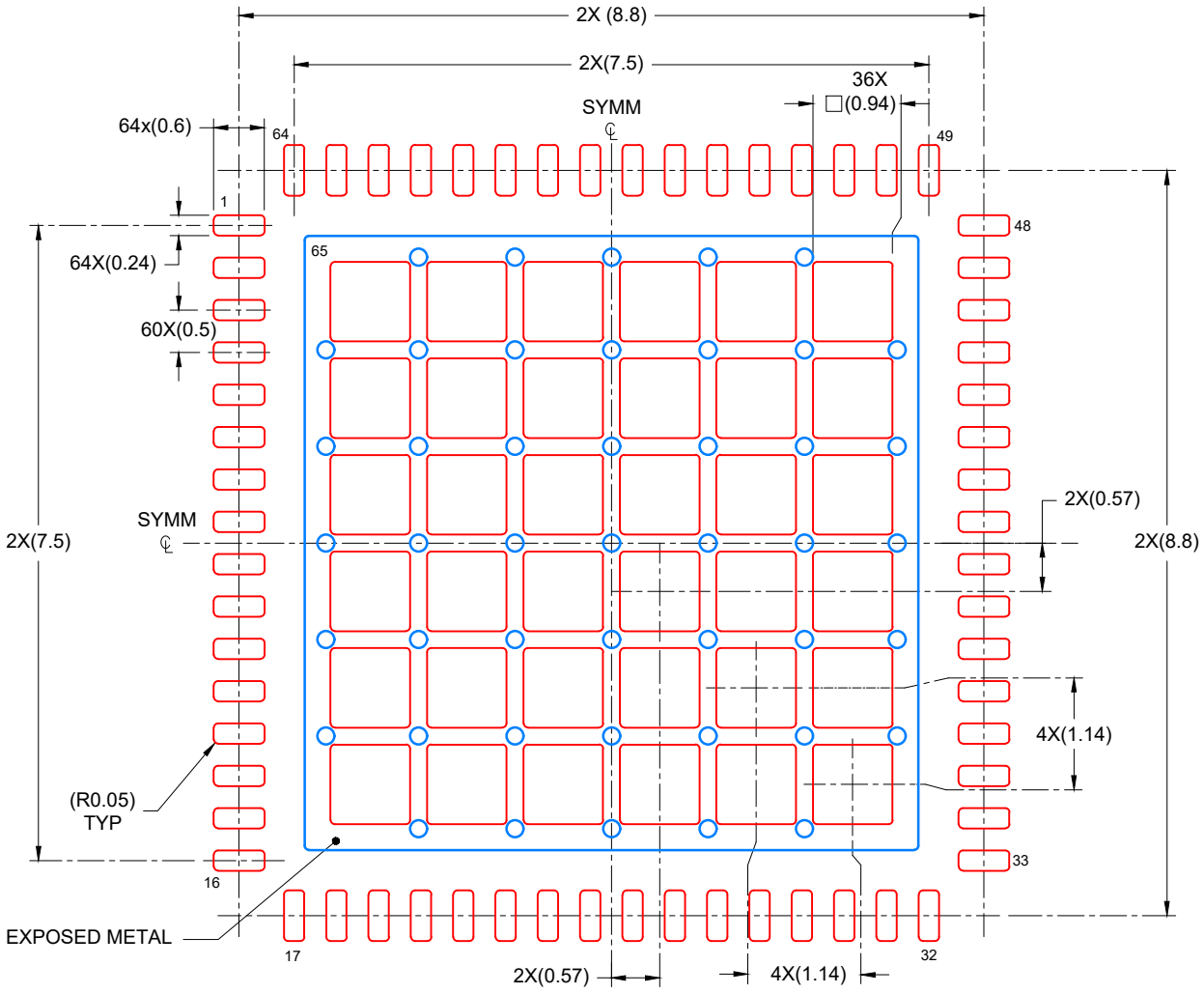
SCALE: 10X

SOLDER MASK DETAILS

4219009/A 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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