# QUICKSWITCH® PRODUCTS HIGH-SPEED CMOS 20-BIT BUS SWITCH WITH FLOW-THRU PINOUT

*IDTQS32X861*

## FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay, zero ground bounce
- Undershoot clamp diodes on all switch and control inputs
- Available in 48-pin QVSOP package

## APPLICATIONS:

- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Power conservation
- Capacitance reduction and isolation
- Bus isolation
- Clock gating

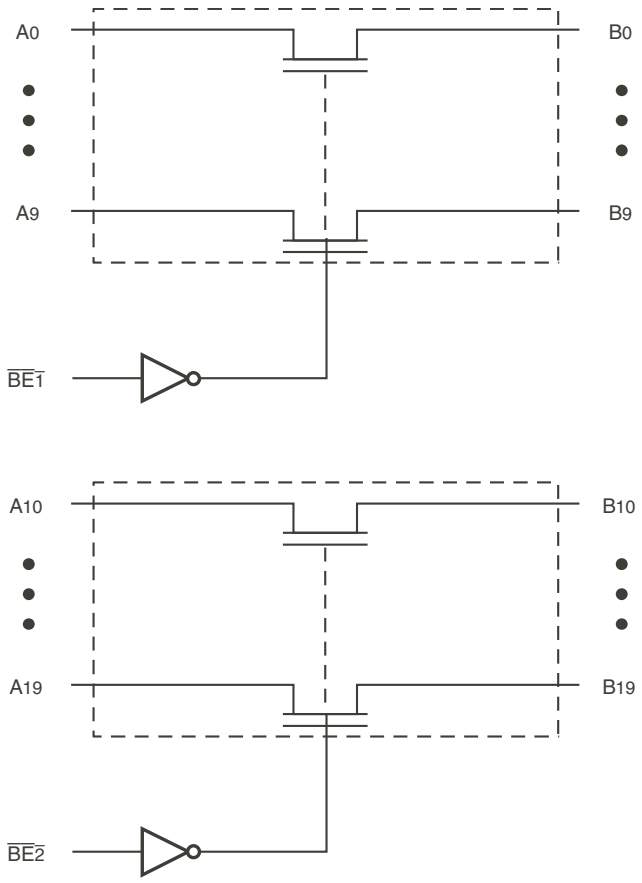
## DESCRIPTION:

The QS32X861 provides two sets of ten high-speed CMOS TTL-compatible bus switches. The low ON resistance of the QS32X861 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable ($\overline{BEn}$) signals turn the switches on.

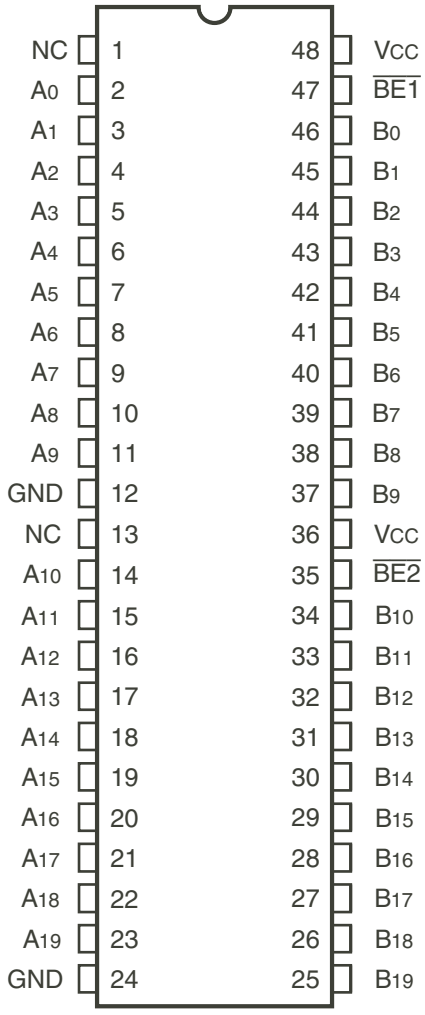
The QS32X861 bus switch is ideal for switching digital buses, as well as for hotplug buffering and 5V to 3V conversion.

The QS32X861 is characterized for operation at -40°C to +85°C.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**QVSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Supply Voltage to Ground | –0.5 to +7 | V |
| $V_{TERM}$(3) | DC Switch Voltage Vs | –0.5 to +7 | V |
| $V_{TERM}$(3) | DC Input Voltage $V_{IN}$ | –0.5 to +7 | V |
| $V_{AC}$ | AC Input Voltage (pulse width ≤ 20ns) | –3 | V |
| $I_{OUT}$ | DC Output Current | 120 | mA |
| $P_{MAX}$ | Maximum Power Dissipation ($T_A$ = 85°C) | 0.5 | W |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. All terminals except Vcc.

## CAPACITANCE

($T_A$ = +25°C, f = 1.0MHz, $V_{IN}$ = 0V, $V_{OUT}$ = 0V)

| Pins | Typ. | Max.(1) | Unit |
|---|---|---|---|
| Control Pins | 3 | 5 | pF |
| Quickswitch Channels (Switch OFF) | 5 | 7 | pF |

**NOTE:**
1. This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

| Pin Names | I/O | Description |
|---|---|---|
| $A_0$ - $A_{19}$ | I/O | Bus A |
| $B_0$ - $B_{19}$ | I/O | Bus B |
| $\overline{BE}n$ | I | Bus Enable |

## FUNCTION TABLE(1)

| $\overline{BE1}$ | $\overline{BE2}$ | $A_0$ - $A_9$ | $A_{10}$ - $A_{19}$ | Function |
|---|---|---|---|---|
| L | L | $B_0$ - $B_9$ | $B_{10}$ - $B_{19}$ | Connect |
| L | H | $B_0$ - $B_9$ | Z | Connect |
| H | L | Z | $B_{10}$ - $B_{19}$ | Connect |
| H | H | Z | Z | Disconnect |

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   Z = High-Impedance

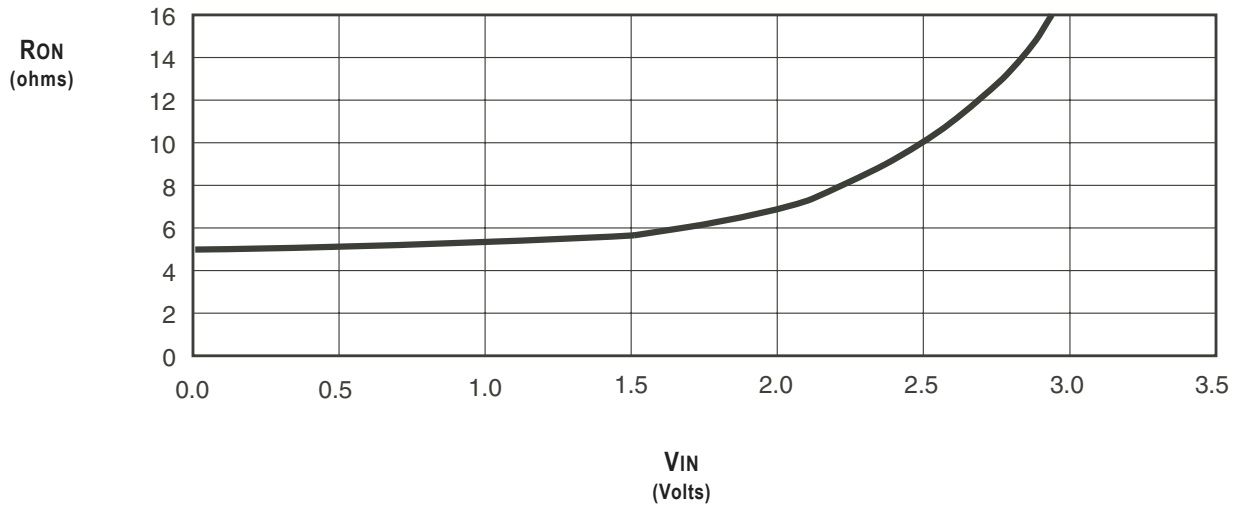
## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: $T_A$ = –40°C to +85°C, $V_{CC}$ = 5.0V ±5%

| Symbol | Parameter | Test Conditions | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH for Control Pins | 2 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW for Control Pins | — | — | 0.8 | V |
| $I_{IN}$ | Input LeakageCurrent (Control Inputs) | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | ±0.01 | ±1 | µA |
| $I_{OZ}$ | Off-State Output Current (Hi-Z) | 0V ≤ $V_{OUT}$ ≤ $V_{CC}$, Switches OFF | — | ±0.01 | ±1 | µA |
| $R_{ON}$ | Switch ON Resistance | $V_{CC}$ = Min., $V_{IN}$ = 0V, $I_{ON}$ = 30mA | — | 5 | 7 | Ω |
| | | $V_{CC}$ = Min., $V_{IN}$ = 2.4V, $I_{ON}$ =15mA | — | 10 | 15 | |
| $V_P$ | Pass Voltage[2] | $V_{CC}$ = 5V, $I_{OUT}$ = -5µA | 3.7 | 4 | 4.2 | V |

**NOTES:**
1. Typical values are at $V_{CC}$ = 5.0V, $T_A$ = 25°C.
2. Pass Voltage is guaranteed but not production tested.

## TYPICAL ON RESISTANCE vs $V_{IN}$ AT $V_{CC}$ = 5V



## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | Typ[2] | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CCQ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or Vcc, f = 0 | 0.2 | 6 | µA |
| $\Delta I_{CC}$ | Power Supply Current per Control Input HIGH[3] | $V_{CC}$ = Max., $V_{IN}$ = 3.4V, f = 0 | — | 2.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current per MHz[4] | $V_{CC}$ = Max., A and B pins open<br>$\overline{BE}n$ Control Input Toggling at 50% Duty Cycle | — | 0.25 | mA/MHz |

**NOTES:**
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Typical values are at $V_{CC}$ = 5.0V, 25°C ambient.
3. Per TLL driven input ($V_{IN}$ = 3.4V, control inputs only). A and B pins do not contribute to ΔIcc.
4. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B pins generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

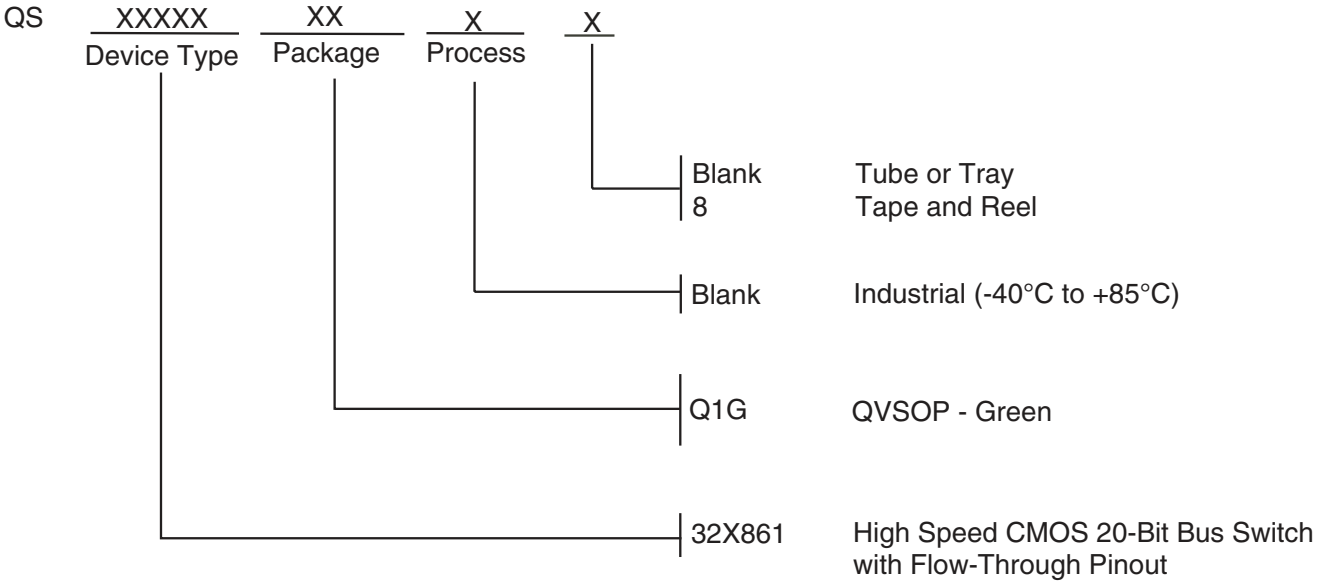
$T_A$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 5%;

$C_{LOAD}$ = 50pF, $R_{LOAD}$ = 500Ω unless otherwise noted.

| Symbol | Parameter | Min.[1] | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Data Propagation Delay[2,3]<br>An to/from Bn | — | 0.25 | — | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Switch Turn-on Delay<br>$\overline{BE}n$ to An/Bn | 1.5 | — | 6.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Switch Turn-off Delay[2]<br>$\overline{BE}n$ to An/Bn | 1.5 | — | 5.5 | ns |

**NOTES:**
1. Minimums are guaranteed but not production tested.
2. This parameter is guaranteed but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for $C_L$ = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

## ORDERING INFORMATION



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