To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

MOS FIELD EFFECT POWER TRANSISTOR

Phase-out/Discontinued

2SJ133,133-Z

P-CHANNEL POWER MOSFET FOR SWITCHING

FEATURES

- Gate drive available at logic level (V_{GS} = –4 V)
- High current control available in small dimension due to low $R_{DS(on)}$ (≅ 0.45 Ω)
- 2SJ133-Z is a lead process product and is ideal for mounting a hybrid IC.

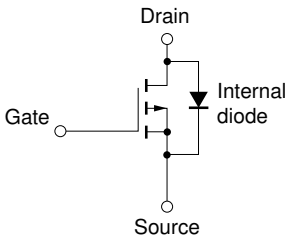
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Drain to Source Voltage	V_{DSS}	V_{GS} = 0 V	–60	V
Gate to Source Voltage	V_{GSS}	V_{DS} = 0 V	∓20	V
Drain Current (DC)	$I_{D(DC)}$	T_C = 25°C	∓2.0	A
Drain Current (pulse)	$I_{D(pulse)}$	PW ≤ 300 μs duty cycle ≤ 10%	∓8.0	A
Total Power Dissipation	P_{T1}	T_C = 25°C	20	W
Total Power Dissipation	P_{T2}	T_A = 25°C	1.0 Note 1, 2.0 Note 2	W
Channel Temperature	T_{ch}		150	°C
Storage Temperature	T_{stg}		–55 to +150	°C

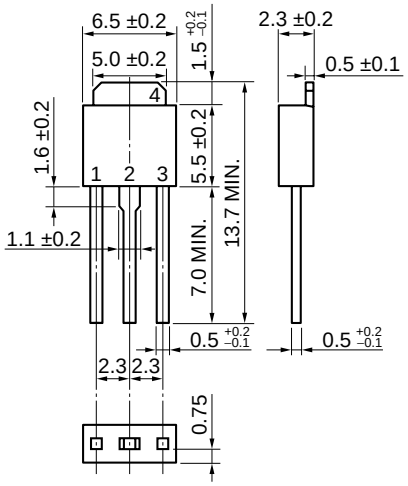
Note 1. Printing board mounted

2. 7.5 cm^2 × 0.7 mm ceramic board mounted

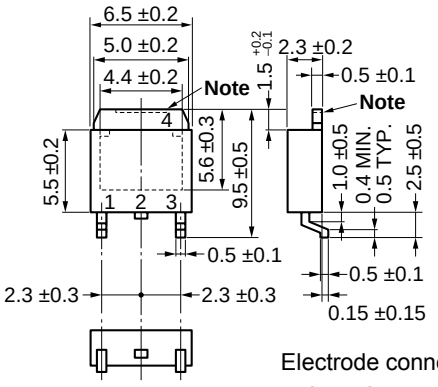
EQUIVALENT CIRCUIT



PACKAGE DRAWING (UNIT: mm)



<R> TO-251 (MP-3)



TO-252 (MP-3Z)

Electrode connection
1. Gate (G)
2. Drain (D)
3. Source (S)
4. Fin (drain)

Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

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Date Published January 2007 NS CP(K)
Printed in Japan

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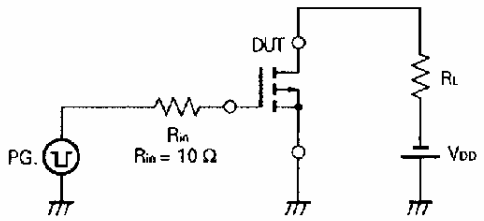
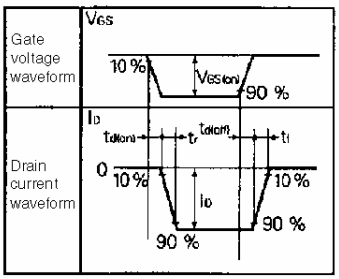
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

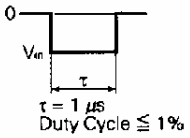
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Drain cutoff current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0 V			–10	μA
Gate cutoff current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓100	nA
Gate cutoff voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1.0 mA	–1.0	–2.0	–3.0	V
Forward transfer admittance	$\|y_{ts}\|$	V_{DS} = –10 V, I_D = –1.0 A	1.0	1.8		S
Drain to source on-state resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –1.0 A		0.45	0.8	Ω
Drain to source on-state resistance	$R_{DS(on)2}$	V_{GS} = –4 V, I_D = –0.8 A		0.7	1.3	Ω
Input capacitance	C_{iss}	V_{DS} = –10 V, V_{GS} = 0 V f = 1 MHz		660		pF
Output capacitance	C_{oss}			250		pF
Reverse transfer capacitance	C_{rss}			50		pF
Turn-on delay time	$t_{d(on)}$	I_D = –1.0 A, $V_{GS(on)}$ = –10 V V_{DD} ≅ –30 V, R_L = 30 Ω, R_{in} = 10 Ω		30		ns
Rise time	t_r			30		ns
Turn-off delay time	$t_{d(off)}$			110		ns
Fall time	t_f			40		ns

SWITCHING TIME TEST CIRCUIT, TEST CONDITION (RESISTANCE LOAD)



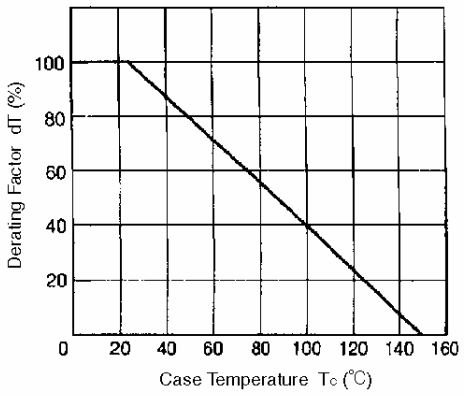




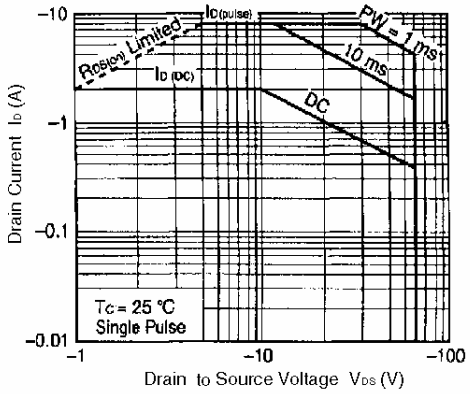
Phase-out/Discontinued

TYPICAL CHARACTERISTICS (T_A = 25°C)

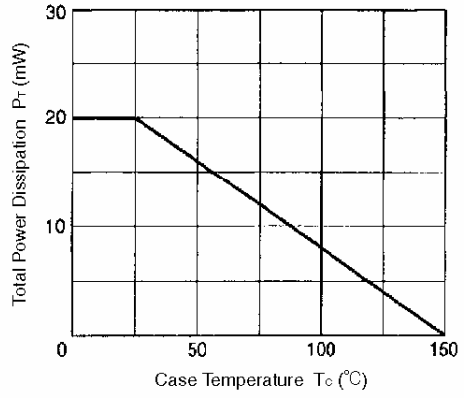
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



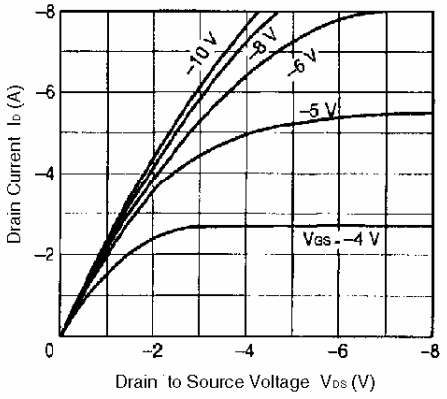
FORWARD BIAS SAFE OPERATING AREA



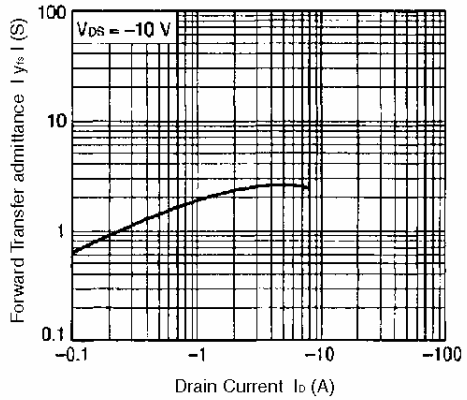
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



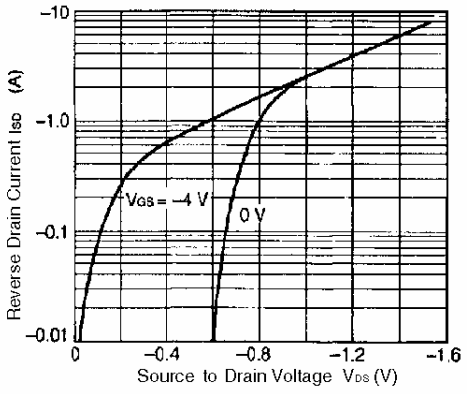
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

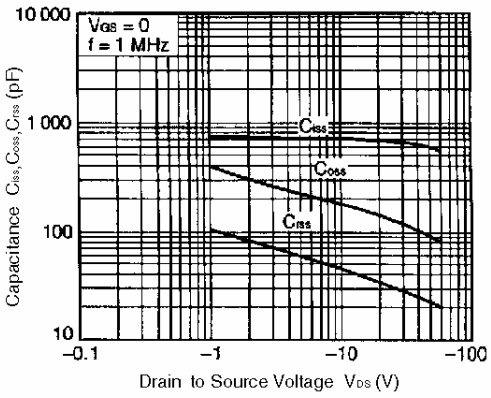


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

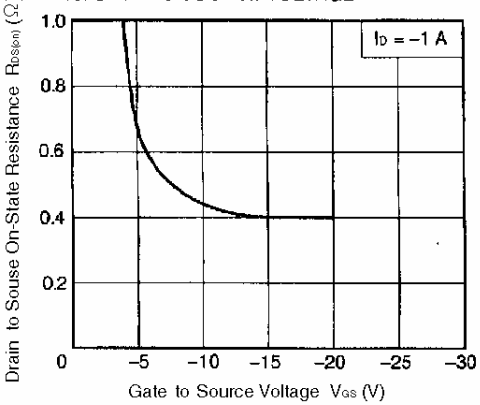


Phase-out/Discontinued

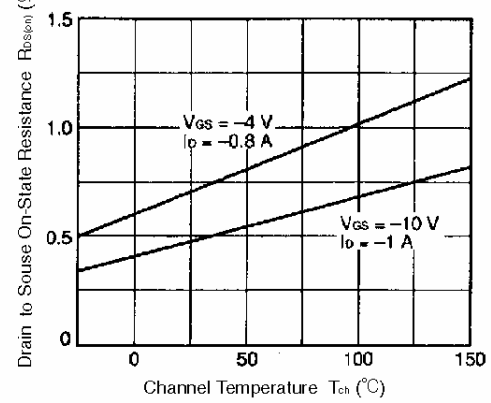
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



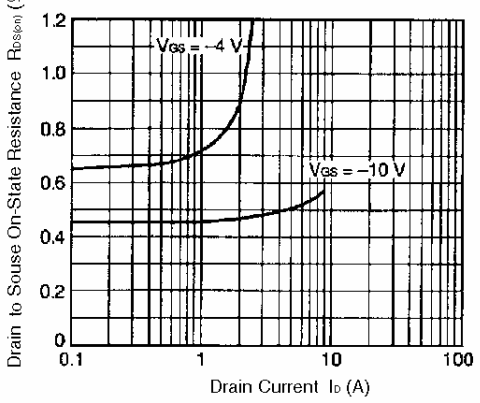
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



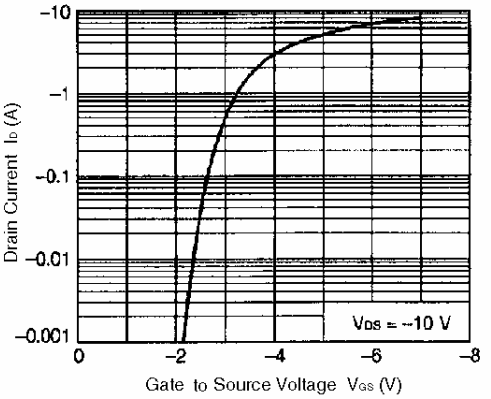
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



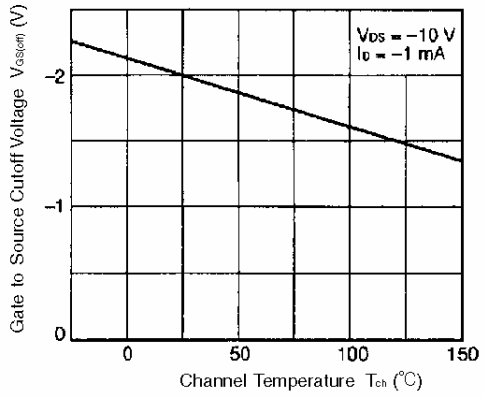
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



TRANSFER CHARACTERISTIC



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



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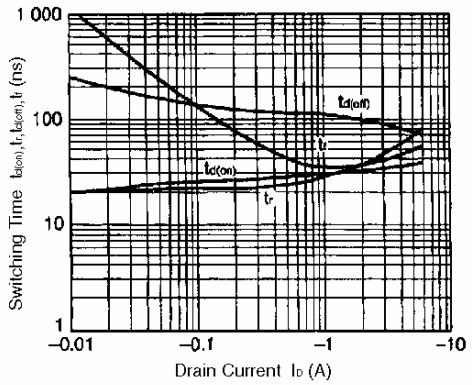
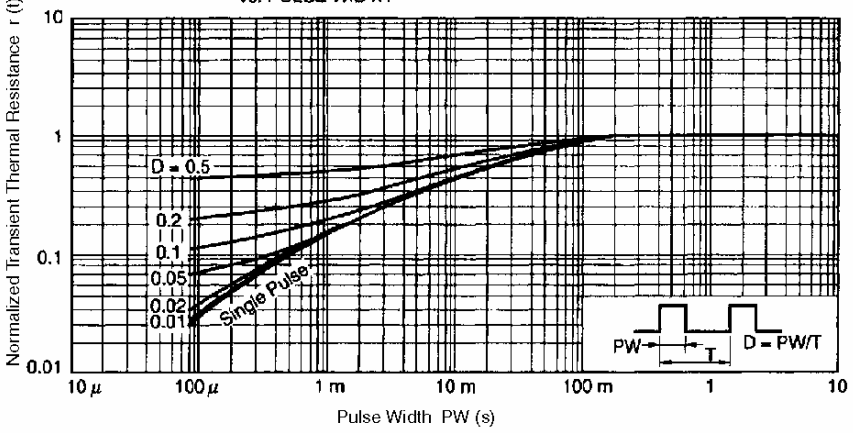
SWITCHING TIME vs. DRAIN CURRENT



NORMALIZED TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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