TS3A227E Autonomous Audio Accessory Detection and Configuration Switch

1 Features

- Supple Range of 2.5 V to 4.5 V
- Accessory Insertion/Removal Detection with Adjustable De-bounce Timings
- Accessory Configuration Detection:
  - Stereo 3-pole Headphone
  - 4-pole Standard Headset with MIC on Sleeve
  - 4-pole OMTP Headset with MIC on Ring2
- Key Press Detection for Up to 4 Keys
- Ultra Low Ground FET R_{ON} of 60 mΩ
- Power Off Noise Removal
- Isolation of MICBIAS From Audio Jack to Remove Click/Pop Noise
- Integrated Codec Sense Line
- Manual I^2C Control
- FM Transmission Capability
- Dual Small Package Options
  - 16 Pin DSBGA
  - 16 Pin QFN

2 Applications

- Mobile Phones
- Tablets
- Notebooks and Ultrabooks
- Anywhere a 3.5 mm Audio Jack is Used

3 Description

The TS3A227E is an autonomous audio accessory detection and configuration switch that detects 3-pole or 4-pole audio accessories and configures internal switches to route the signals accordingly.

The internal ground FETS of the TS3A227E have an ultra-low R_{ON} of 60 mΩ to minimize crosstalk impact. The ground FETs are also designed to pass FM signals, making it possible to use the ground line of the accessory as an FM antenna in mobile audio applications.

Internal isolation switches allow the TS3A227E to remove the click/pop noise that can be generated during and insertion or removal of an audio accessory. In addition depletion FETs prevent a floating ground while the device is unpowered, removing the humming noise present when leaving accessories plugged into an unpowered system.

A low-power sleep mode is provided which shuts down internal circuitry to achieve very low quiescent current draw when no headset is inserted.

The TS3A227E features integrated key press detection for detecting up to 4 keys with press and release support.

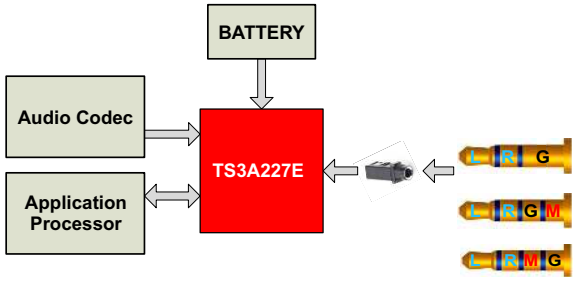
Manual I2C control allows the TS3A227E to adapt to application needs by providing control over de-bounce settings and switch states.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A227E	QFN (16)	3.50 mm × 3.50 mm
	DSBGA (16)	1.79 mm × 1.79 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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Changes from Original (July 2014) to Revision A — **Page**

- Initial release of full version document. ... 1

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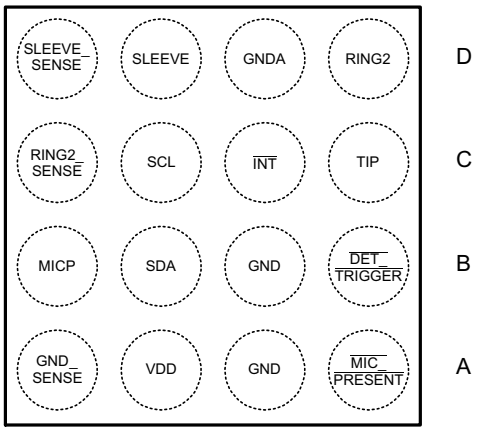
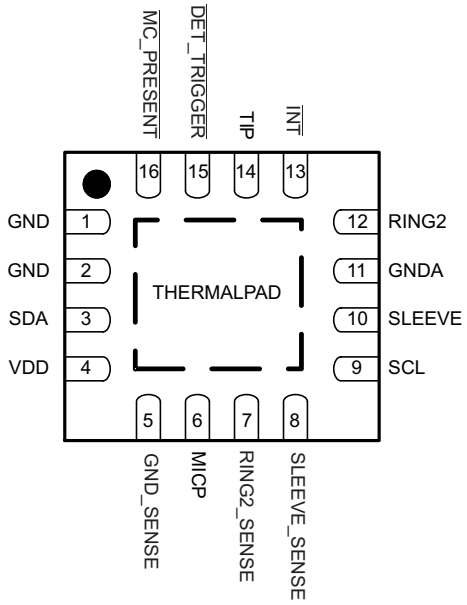
6 Pin Configuration and Functions

DSBGA – YFF
Top View



QFN – RVA
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	RVA	YFF		
$\overline{\text{DET\_TRIGGER}}$	15	B1	I/O	A falling edge from high to low on this pin triggers accessory detection. This pin can be connected the headset jack to allow automatic pull-down to ground after headset insertion to initialize detection.
GND	1, 2	A2, B2	GND	Primary ground connection for the TS3A227E. Must be connected to system ground.
GNDA	11	D2	I/O	Ground connection for the internal ground FETs of the TS3A227E. If FM is being supported connect this pin to the FM matching network. If FM is not being support connect this pin to system ground.
GND_SENSE	5	A4	I/O	Ground sense line for the codec.
$\overline{\text{INT}}$	13	C2	GND	Open drain interrupt output from the TS3A227E to notify the host that an event has occurred. If I^2C is not used this pin must be grounded.
$\overline{\text{MIC\_PRESENT}}$	16	A1	I/O	Open drain output to indicate to the host that a headset with a microphone is inserted..
MICP	6	B4	I/O	Microphone signal connection to the codec. Microphone bias is applied to this pin.
RING2	12	D1	O	Headset current return path if RING2 is ground for the headset. Connect to 3.5 mm jack RING2 connection with low DC resistance trace.
RING2_SENSE	7	C4	GND	Connected to the RING2 pin of the 3.5 mm jack. If RING2 pin on plug in is MIC signal, this is connected to MICP. If not, this is connected to GND_SENSE and becomes the ground sensing feedback for the accessory
SCL	9	C3	I	Clock from I^2C bus. This can be connected to VDD if I2C is not used.
SDA	3	B3	I/O	Bidirectional data from/to I^2C bus. This can be connected to VDD if I^2C is not used.
SLEEVE	10	D3	O	Headset current return path if SLEEVE is GND for headset. Connect to 3.5 mm jack SLEEVE connection with low DC resistance trace.
SLEEVE_SENSE	8	D4	GND	Connected to the SLEEVE pin of the 3.5 mm jack. If SLEEVE pin on plug in is MIC signal, this is connected to MICP. If not, this is connected to GND_SENSE and becomes the ground sensing feedback for the accessory
THERMAL PAD			GND	The THERMAL PAD of the RVA – QFN package must be connected to any internal PCB ground plane using multiple vias for best thermal performance.
TIP	14	C1	I/O	Connect to the TIP pin of the 3.5 mm jack.
VDD	4	A3	PWR	Power input to the TS3A227E. External de-coupling capacitors are required on this pin.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltage	VDD	–0.3	5	V
	SDA, SCL, $\overline{\text{INT}}$, $\overline{\text{MIC\_PRESENT}}$	–0.3	V_{DD} + 0.5	V
	TIP	–3.3	V_{DD} + 0.5	V
	$\overline{\text{DET\_TRIGGER}}$	–2.2	V_{DD} + 0.5	V
	GND_SENSE, RING2, SLEEVE, RING2_SENSE, SLEEVE_SENSE, MICP, GNDA	–0.3	3.6(2) and V_{DD} + 0.5	V
ON-state switch current	Combined continuous current through R2GNDFET and SLV GNDFET		500	mA
	Continuous current through R2DFET and SLV DFET		50	
	Continuous current through S1		20	
	Continuous current through S2		20	
	Continuous current through S3PR		50	
	Continuous current through S3PS		50	
	Continuous current through S3GR		100	
	Continuous current through S3GS		100	
Operating ambient temperature range		–40	85	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This rating is exclusive and the voltage on the pins must not exceed either 3.6 and V_{DD}. E.g. if V_{DD} = 4.5 V the voltage on the pin must not exceed 3.6 V and if V_{DD} is = 2.5 V the voltage on the pin must not exceed 3.0 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), ESD stress voltagenew note #1 to the ESD Ratings table and combined MIN MAX column to VALUE (1) (2)	±2000	V
		Charged device model (CDM), ESD stress voltage(1) (3)	±500	V
		Contact discharge model (IEC) ESD stress voltage on TIP, $\overline{\text{DET\_TRIGGER}}$, RING2_SENSE, SLEEVE_SENSE, RING2, SLEEVE(1)	±8000	V

(1) Electrostatic Discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
VDD	Power supply voltage range		2.5	4.5	V
V_I	Digital input voltage range	SDA, SCL	0	V_{DD}	V
		$\overline{\text{DET\_TRIGGER}}$	–2.2	V_{DD}	V
V_{IO}	Input/output voltage range	RING2_SENSE, SLEEVE_SENSE, RING2, SLEEVE, GND_SENSE, MICP	0	3.3[1] and VDD	V
		TIP	–3	V_{DD}	
V_O	Output voltage range	$\overline{\text{INT}}$, $\overline{\text{MIC\_PRESENT}}$	0	V_{DD}	V
V_{IH}	Input logic high	SDA, SCL	1.2	V_{DD}	V
		$\overline{\text{DET\_TRIGGER}}$	0.65 × V_{DD}	V_{DD}	V
V_{IL}	Input logic low	SDA, SCL	0	0.4	V
		$\overline{\text{DET\_TRIGGER}}$	0	0.4 × V_{DD}	V
T_A	Operating ambient temperature		–40	85	°C

(1) This rating is exclusive and the voltage on the pins must not exceed either 3.3 and V_{DD}. E.g. if V_{DD} = 4.5 V the voltage on the pin must not exceed 3.3 V and if V_{DD} is = 2.5 V the voltage on the pin must not exceed 2.5 V.

7.4 Thermal Information

THERMAL METRIC[1]		TS3A227E RTE 16 PINS	TS3A227E YFF 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.9	77.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.6	0.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.2	12.5	
ψ_{JT}	Junction-to-top characterization parameter	0.9	2.3	
ψ_{JB}	Junction-to-board characterization parameter	21.2	12.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	-	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Unless otherwise noted the specification applies over the VDD and ambient operating temperature range.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VDD	Supply voltage		2.5	3.3	4.5	V
I_{DD}	Quiescent current	No accessory inserted. I^2C bus inactive(1) V_{DD} = 2.5 V to 4.5 V		0.5	10	µA
		Manual switch control = '1' , I^2C bus inactive,(1) V_{DD} = 2.5 V to 4.5 V, Depletion FETs on		7	15	µA
		Manual switch control = '1' , I^2C bus inactive, V_{DD} = 2.5 V to 4.5 V Depletion FETs off		20	40	µA
		3-pole accessory inserted. I^2C bus inactive(1), FM Support = '0' V_{DD} = 2.5 V to 4.5 V		11	20	µA
		3-pole accessory inserted. I^2C bus inactive,(1) FM Support = '1' V_{DD} = 2.5 V to 4.5 V		25	45	µA
		4-pole Accessory inserted. I^2C bus inactive,(1) V_{DD} = 2.5 V to 4.5 V		25	40	µA
		4-pole Accessory inserted. KP detection enabled I^2C bus inactive,(1) V_{DD} = 2.5 V to 4.5 V		30	45	µA
$I_{DD\_1.8}$	Quiescent current addition from using a 1.8 V I2C bus.(2)	No accessory inserted. I^2C bus inactive at 1.8 V,(3) V_{DD} = 2.5 V to 4.5 V		1	8	µA
SWITCH RESISTANCE						
$R_{R2GNDFT}$	RING2 GNDFET on resistance (DSBGA Package)	V_{DD} = 3.3 V, V_{GND} = 0V, I_{GNDA} = 75 mA		40	85	mΩ
	RING2 GNDFET on resistance (QFN Package)			60	95	
$R_{SLVGNDFT}$	SLEEVE GNDFET on resistance (DSBGA Package)			40	85	
	SLEEVE GNDFET on resistance (QFN Package)			60	95	
R_{S3PS}	S3PS on resistance	V_{DD} = 3.3 V, $V_{SLEEVE\_SENSE/RING2\_SENSE}$ = 0 V to 2.7 V, I_{MICP} = ±10 mA		3	6.5	Ω
R_{S3PR}	S3PR on resistance			3	6.5	
R_{S3GS}	S3GS on resistance	V_{DD} = 3.3 V, $V_{SLEEVE\_SENSE/RING2\_SENSE}$ = 0 V to 2.7 V, I_{GND_SENSE} = ±75 mA		0.5	1	Ω
R_{S3GR}	S3GR on resistance			0.5	1	
R_{S1}	Switch 1 on resistance	V_{DD} = 3.3 V, I_{GND} = 10 mA		15	30	Ω
R_{S2}	Switch 2 on resistance			15	30	
R_{R2DFET}	RING2 depletion FET on resistance			75	150	Ω
$R_{SLVDFET}$	SLEEVE depletion FET on resistance			75	150	
SWITCH LEAKAGE CURRENT						
I_{OFF}	RING2 pin off leakage	V_{IN} = 0 V to 3.3 V, V_{DD} = 3.3 V			1	µA
	SLEEVE pin off leakage				1	
	RING2_SENSE pin off leakage				1	
	SLEEVE_SENSE pin off leakage				1	
	MICP pin off leakage				1	
	GND_SENSE pin off leakage				1	
I_{ON}	S2PS, S3PR, S3GS, S3GR on leakage	$V_{SLEEVE/RING2}$ = 0V, V_{DD} = 3.3 V			1	µA

(1) The I^2C bus is inactive if both the SDA and SCL lines are tied to V_{DD}.
(2) If the I^2C bus is operating at 1.8 V the $I_{DD\_1.8}$ current number will be in addition to the other current consumption numbers specified.
(3) The I^2C bus is inactive if both the SDA and SCL lines are tied to 1.8 V.

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Electrical Characteristics (continued)

Unless otherwise noted the specification applies over the VDD and ambient operating temperature range.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCH TIMING						
t_{OFF}	Turn off time for S3PS, S3PR, S3GS, S3GR	V_{DD} = 2.5 V, 3.3 V, 4.5 V, R_L = 300 Ω, C_L = 50 pF $V_{SLEEVE\_SENSE/RING2\_SENSE}$ = 2.5 V (V_{DD} = 2.5 V), 3.3 V (V_{DD} = 3.3 V, V_{DD} = 4.5 V)			5	µs
	Turn off time for S1, S2, RING2 GNDFET, SLEEVE GNDFET	V_{DD} = 2.5 V, 3.3 V, 4.5 V R_{PU} = 1500 Ω, C_L = 50 pF V_{PU} = 2.5 V (V_{DD} = 2.5 V), 3.3 V (V_{DD} = 3.3 V, V_{DD} = 4.5 V)			5	µs
	Turn off time for RING2 DFET and SLEEVE DFET	V_{DD} = 2.5 V, 3.3 V, 4.5 V R_{PU} = 1500 Ω, C_L = 50 pF V_{PU} = 2.5 V (V_{DD} = 2.5 V), 3.3 V (V_{DD} = 3.3 V, V_{DD} = 4.5 V)			500	µs
t_{ON}	Turn on time for S3PS, S3PR, S3GS, S3GR	V_{DD} = 2.5 V, 3.3 V, 4.5 V R_L = 300 Ω, C_L = 50 pF $V_{SLEEVE\_SENSE/RING2\_SENSE}$ = 2.5 V (V_{DD} = 2.5 V), 3.3 V (V_{DD} = 3.3 V, V_{DD} = 4.5 V)			1	µs
	Turn on time for S1, S2, RING2 GNDFET, SLEEVE GNDFET	V_{DD} = 2.5 V, 3.3 V, 4.5 V R_{PU} = 1500 Ω, C_L = 50 pF V_{PU} = 2.5 V (V_{DD} = 2.5 V), 3.3 V (V_{DD} = 3.3 V, V_{DD} = 4.5 V)			35	µs
	Turn on time for RING2 DFET and SLEEVE DFET	V_{DD} = 2.5 V, 3.3 V, 4.5 V R_{PU} = 1500 Ω, C_L = 50 pF V_{PU} = 2.5 V (V_{DD} = 2.5 V), 3.3 V (V_{DD} = 3.3 V, V_{DD} = 4.5 V)			1	µs
DIGITAL I/O						
V_{OL}	$\overline{\text{MIC\_PRESENT}}$ low level output voltage	V_{DD} = 3.3 V, I_{OL} = 10 mA	0		0.4	V
	$\overline{\text{INT}}$ low level output voltage		0		0.4	
	SDA low level output voltage	V_{DD} = 3.3 V, I_{OLMAX} = 3 mA	0		0.4	
V_{IH}	Input logic high	SDA, SCL	1.2		V_{DD}	V
		$\overline{\text{DET\_TRIGGER}}$	V_{DD} x 0.65		V_{DD}	
V_{IL}	Input logic low	SDA, SCL	0		0.4	
		$\overline{\text{DET\_TRIGGER}}$	0		V_{DD} x 0.4	
$R_{PU/DT}$	Internal $\overline{\text{DET\_TRIGGER}}$ pull-up resistance	V_{DD} = 3.3 V, $I_{/DET\_TRIGGER}$ = 1 µA	0.5	1	1.85	MΩ

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Electrical Characteristics (continued)

Unless otherwise noted the specification applies over the VDD and ambient operating temperature range.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS						
PSR_{217}	Power supply rejection	V_{DD} = 3.3 V ± 200 mV_{PP}, f = 217 Hz, R_L at RING2= 50 Ω	–95	–120		dB
PSR_{1k}		V_{DD} = 3.3 V ± 200 mV_{PP}, f = 1 kHz, R_L at RING2= 50 Ω	–85	–110		
PSR_{20k}		V_{DD} = 3.3 V ± 200 mV_{PP}, f = 20 kHz, R_L at RING2= 50 Ω	–70	–90		
ISO_{S3}	SLEEVE_SENSE or RING2_SENSE to MICP Isolation	V_{IN} = 200 mV_{PP}, f = 20 Hz – 20 kHz, R_L = 50 Ω		–90		dB
SEP_{S3}	SLEEVE_SENSE to RING2_SENSE Separation	V_{IN} = 200 mV_{PP}, f = 20 Hz – 20 kHz, R_L = 50 Ω		–75		dB
BW	Bandwidth through GNDFETs	V_{IN} = 60 mV_{PP}, I_{BIAS} = 10 mA	120	150		MHz
THD_{200}	MICP to RING2_SENSE or SLEEVE_SENSE total harmonic distortion	V_{IN} = 1.5 V + 200 mV_{PP}, f = 20 Hz – 20 kHz, R_S = 600 Ω, R_L = 600 Ω		0.003 %		
THD_{500}		V_{IN} = 1.5 V + 500 mV_{PP}, f = 20 Hz – 20 kHz, R_S = 600 Ω, R_L = 600 Ω		0.002%		
SNR	MICP to RING2_SENSE or SLEEVE_SENSE signal to noise ratio	V_{IN} = 1 V_{RMS}, f = 20 Hz – 20 kHz, R_S = 600 Ω, R_L = 600 Ω	–90	–110		dB
t_{DET}	Detection sequence duration	Time between $\overline{DET\_TRIGGER}$ transition from high to low and $\overline{INT}$ transition from high to low. Default 90 ms insertion debounce.		175	210	ms
$T_{power-up}$	Power up time Power-up time	Time from V_{DD} > 2.5 V till I^2C communication is ready		20	25	ms
$t_{REMOVAL}$	Removal wait period	Time between $\overline{DET\_TRIGGER}$ transition from low to high and RING2/SLEEVE DFETs turning on		50	65	ms

7.6 I^2C Interface Timing Characteristics

Unless otherwise noted the specification applies over the VDD and ambient operating temperature range

PARAMETER		STANDARD MODE I^2C BUS		FAST MODE I^2C BUS		UNIT
		MIN	MAX	MIN	MAX	
f_{scl}	I^2C clock frequency	0	100	0	400	kHz
t_{sch}	I^2C clock high time	4		0.6		µs
t_{scl}	I2C clock low time	4.7		1.3		µs
t_{sp}	I2C spike time		50		50	ns
t_{sds}	I2C serial data setup time	250		100		ns
t_{sdh}	I2C serial data hold time	0		0		ns
t_{icr}	I2C input rise time		1000	21	300	ns
t_{icf}	I2C input fall time		300	21	300	ns
t_{ocf}	I2C output fall time; 10 pF to 400 pF bus		300	20 + 0.1 Cb	300	µs
t_{buf}	I2C bus free time between Stop and Start	4.7		1.3		µs
t_{sts}	I2C Start or repeater Start condition setup time	4.7		0.6		µs
t_{sth}	I2C Start or repeater Start condition hold time	4		0.6		µs
t_{sps}	I2C Stop condition setup time	4		0.6		µs
$t_{vd(data)}$	Valid data time; SCL low to SDA output valid		3.45	0.3	0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		3.45	0.3	0.9	µs
C_b	I2C bus capacitive loading	0	400	0	400	pF

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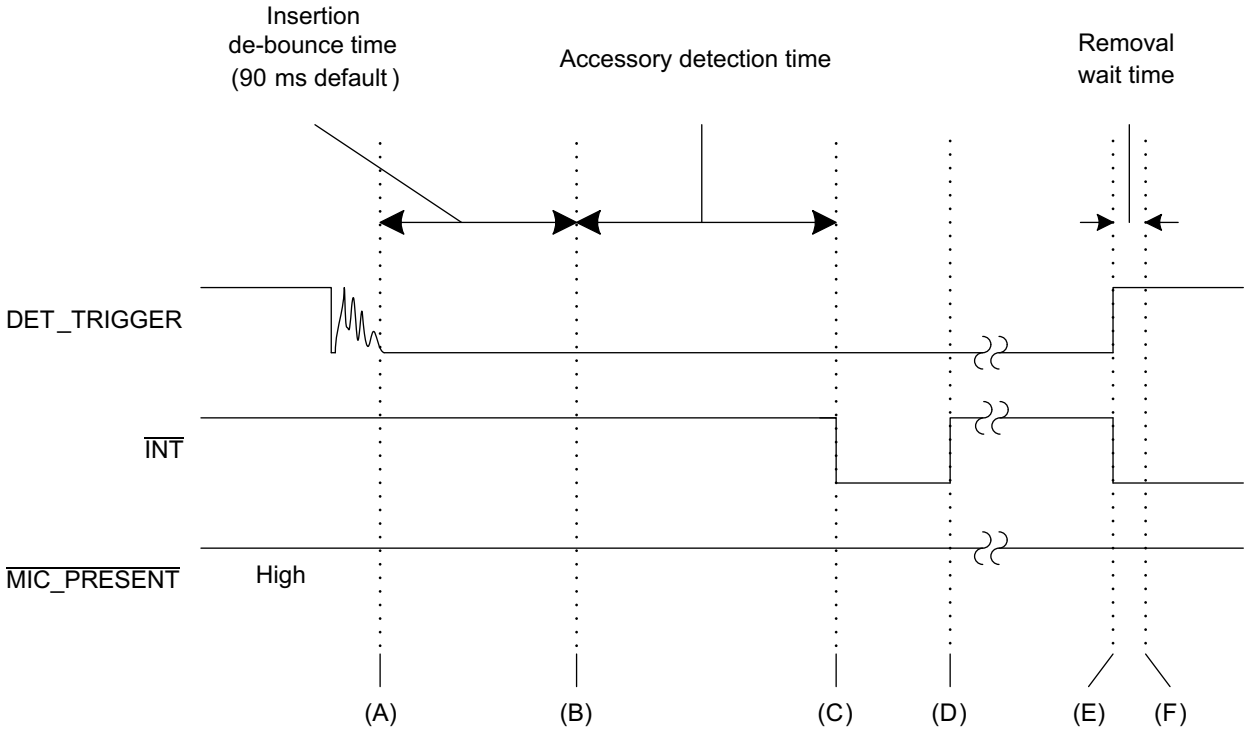
7.7 Timing Diagrams



A. (This is the point that DET_TRIGGER has stopped glitching and is fully low. The de-bounce time of 90 ms starts from the point that the pin is constantly below the V_{IL} level. Any time the DET_TRIGGER pin cross the V_{IH} level the de-bounce timer will restart.

B. Point B is the end of the insertion de-bounce time and the beginning of accessory detection.

C. Detection has completed at this point. The switches will be routed before the INT pin is pulled low.

D. INT is cleared after the host reads the interrupt register.

E. The headset is removed here. The switch states will change immediately and INT will be pulled low.

F. After a 50 ms removal de-bounce timer the TS3A227E will go back into sleep mode if manual switch control is not enabled

Figure 1. 3-Pole Accessory

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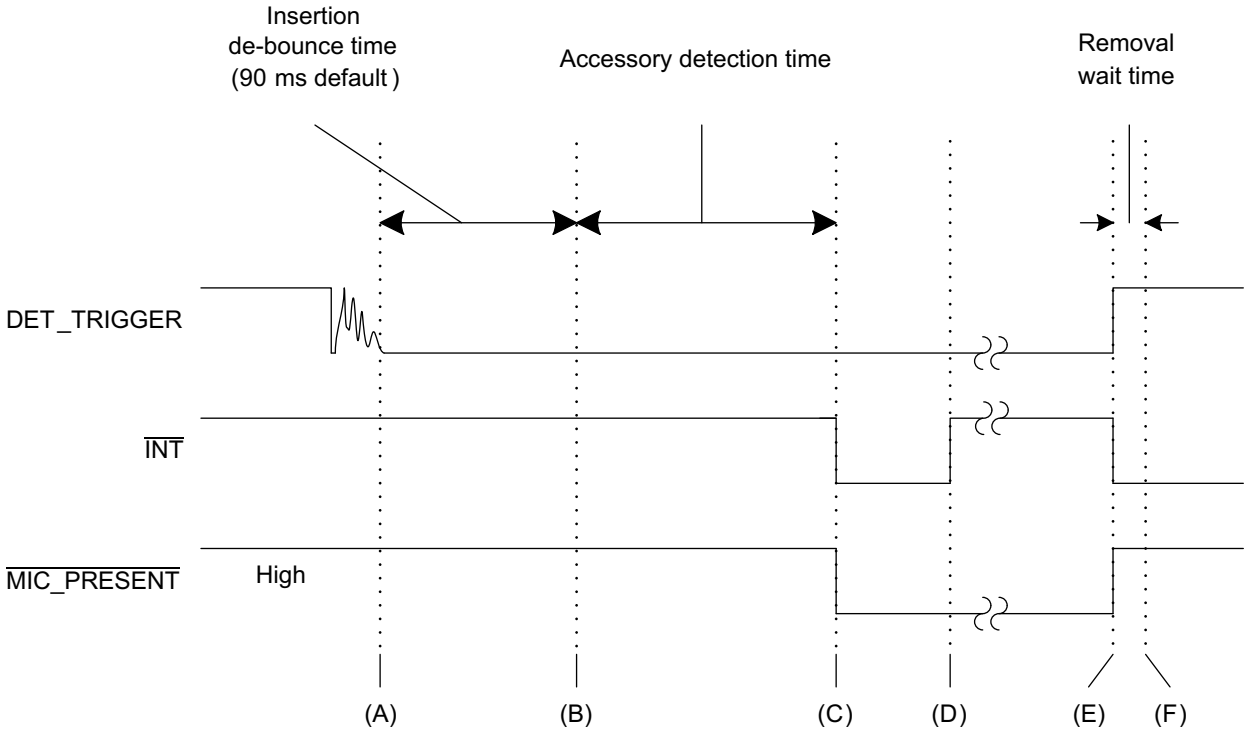
Timing Diagrams (continued)



A. This is the point that DET_TRIGGER has stopped glitching and is fully low. The de-bounce time of 90 ms starts from the point that the pin is constantly below the V_{IL} level. Any time the DET_TRIGGER pin cross the VIH level the de-bounce timer will restart.

B. Point B is the end of the insertion de-bounce time and the beginning of accessory detection.

C. Detection has completed at this point. The switches will be routed before the INT and MIC_PRESENT pins are pulled low.

D. INT is cleared after the host reads the interrupt register.

E. The headset is removed here. The switch states will change immediately and INT will be pulled low. The MIC_PRESENT pin will be released.

F. After a 50 ms removal de-bounce timer the TS3A227E will go back into sleep mode if manual switch control is not enabled

Figure 2. 4-Pole Accessory

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Timing Diagrams (continued)

7.7.1 Removal

A removal event will interrupt any on-going process in the TS3A227E. The following diagram depicts how the device “jumps” during a removal.

If the removal event occurs during the insertion de-bounce period the TS3A227E will jump to the (A) point of the diagram depicted by the green arrow and line.

Any time after point (B) has been reached and the accessory is removed the device jumps to point (E), which includes key press detection. Under Manual Switch Control the switch states will not change.

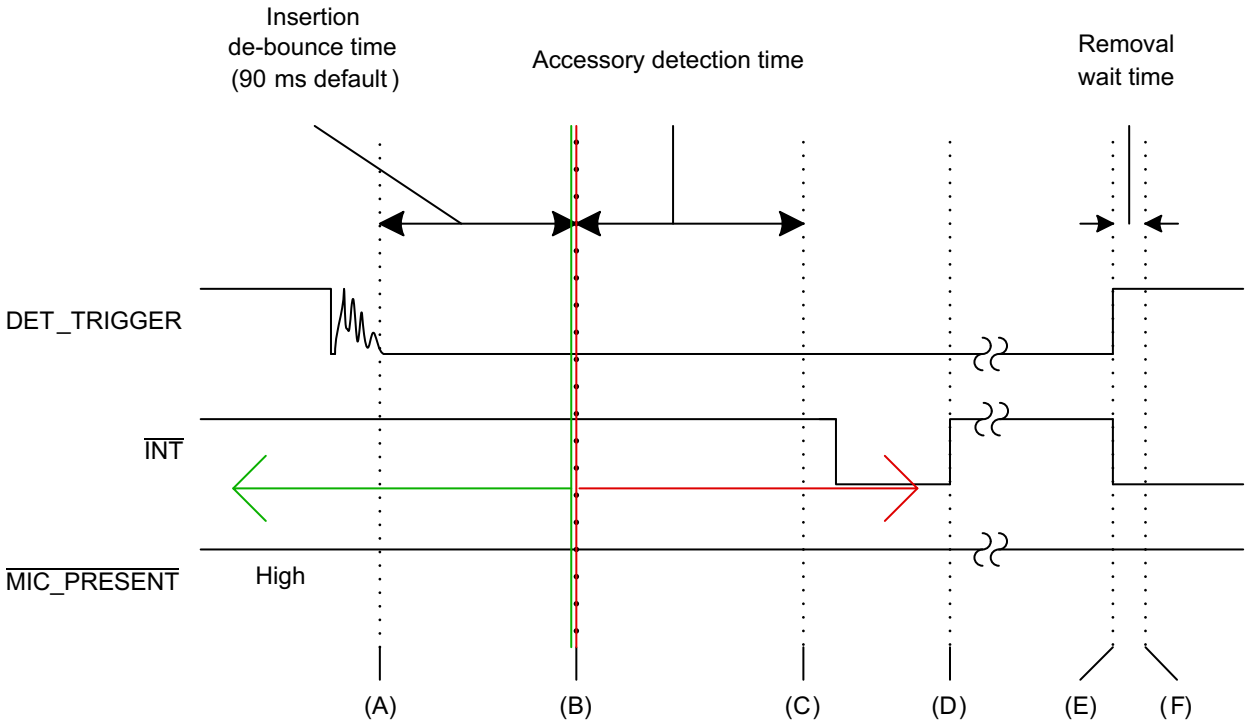

Figure 3. Removal Timing During Insertion

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7.8 Typical Characteristics

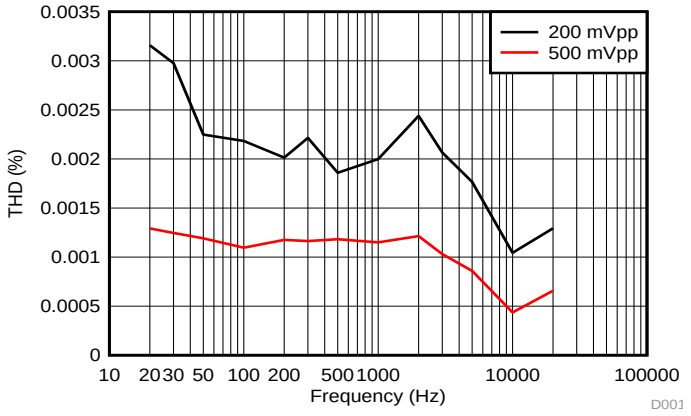

Figure 4. S3PX THD

8 Parameter Measurement Information

Channel ON
$R_{ON} = V_{SLEEVE/RING2} / I_{GNDA}$

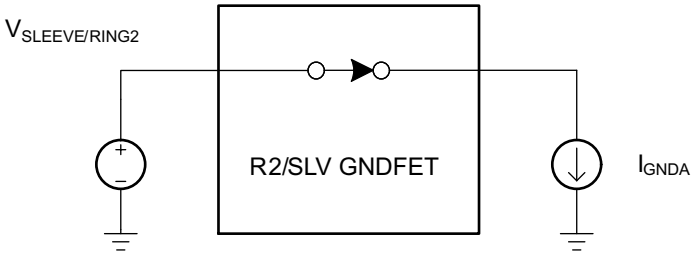

Figure 5. RING2/SLEEVE GNDFET On Resistance Measurement

Channel ON
$R_{ON} = V_{SLEEVE/RING2} / I_{GND}$

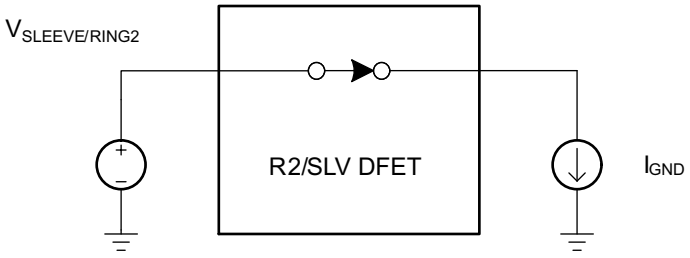

Figure 6. RING2/SLEEVE DFET On Resistance Measurement

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Parameter Measurement Information (continued)

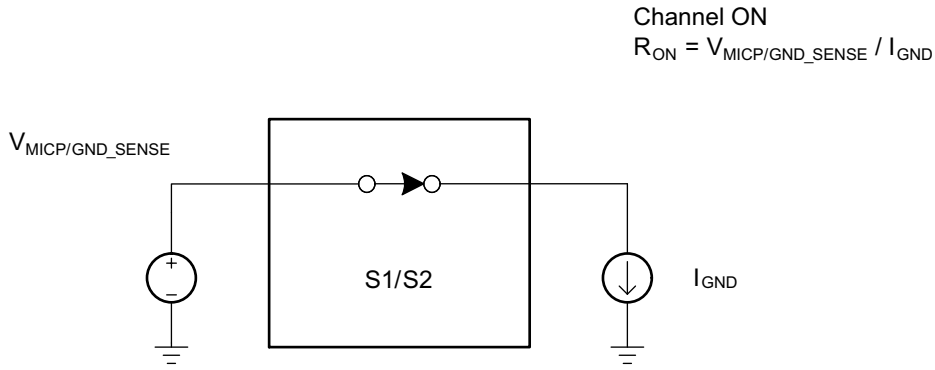

Figure 7. S1/S2 On Resistance Measurement

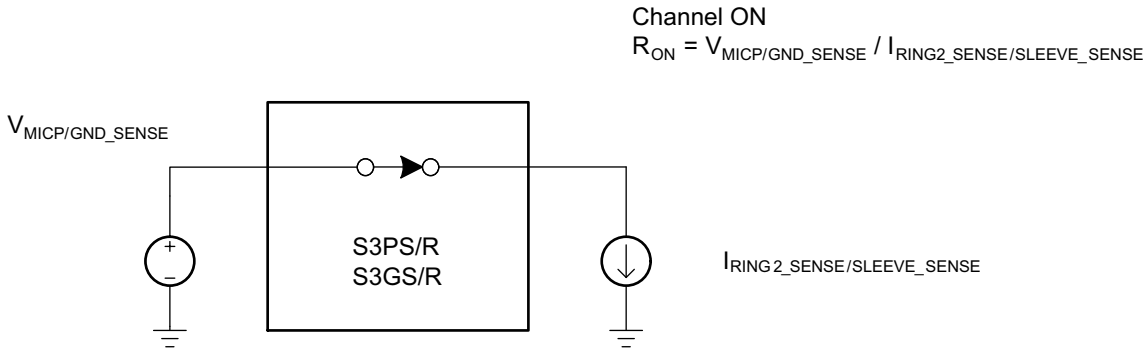

Figure 8. S3PS, S3PR, S3GS, S3GR On Resistance Measurement

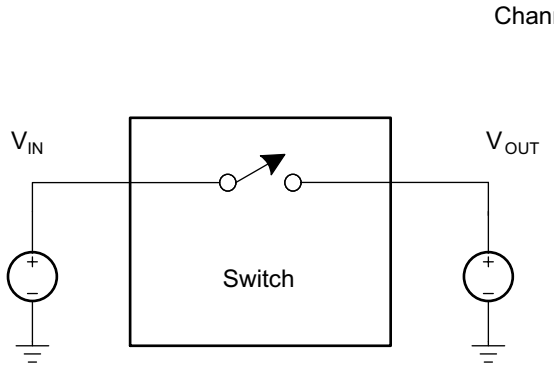

Figure 9. Switch Off Leakage Current

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Parameter Measurement Information (continued)

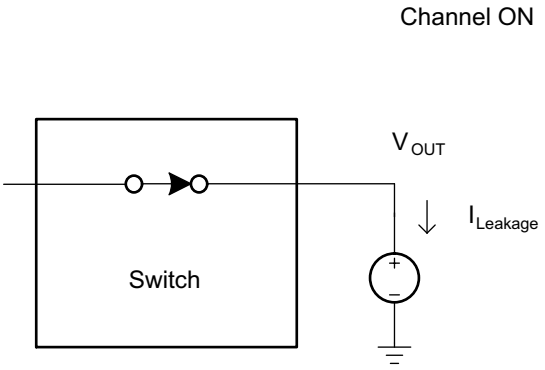

Figure 10. Switch On Leakage Current

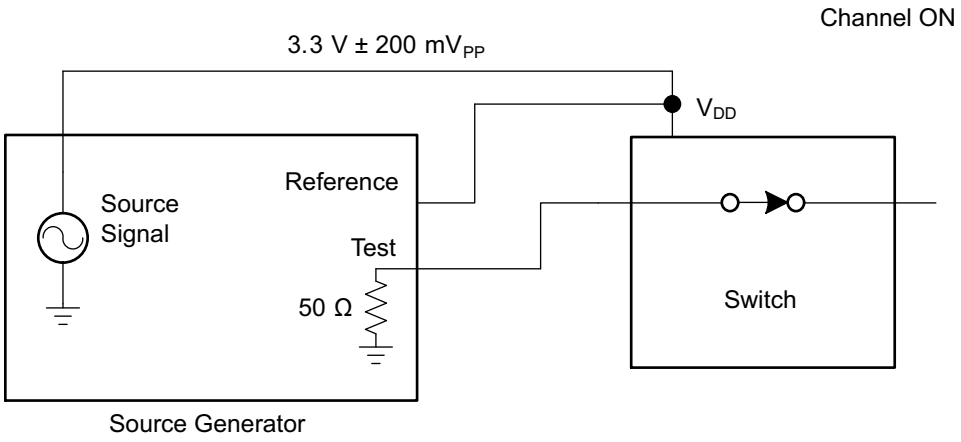

Figure 11. Power Supply Rejection Ratio (PSRR)

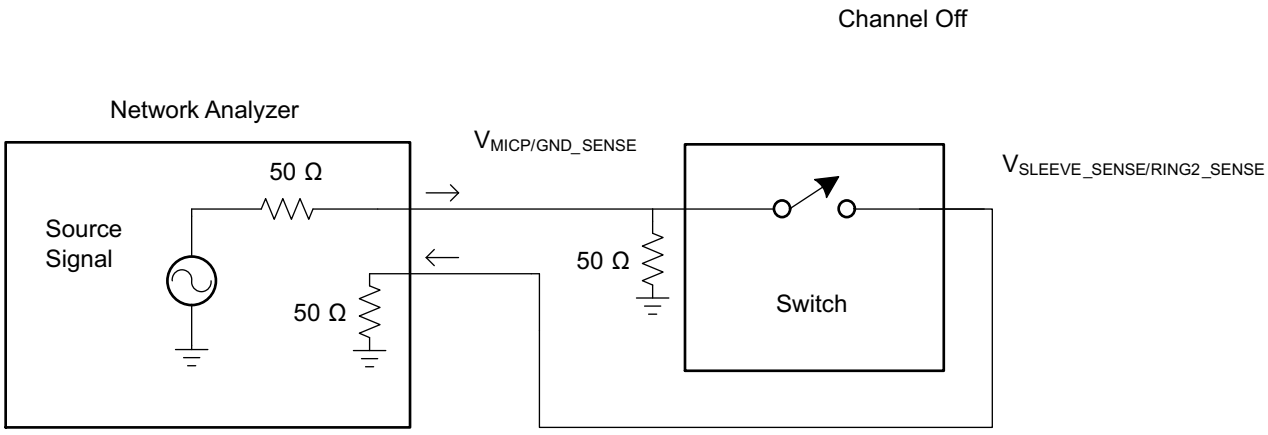

Figure 12. Switch Off Isolation

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Parameter Measurement Information (continued)

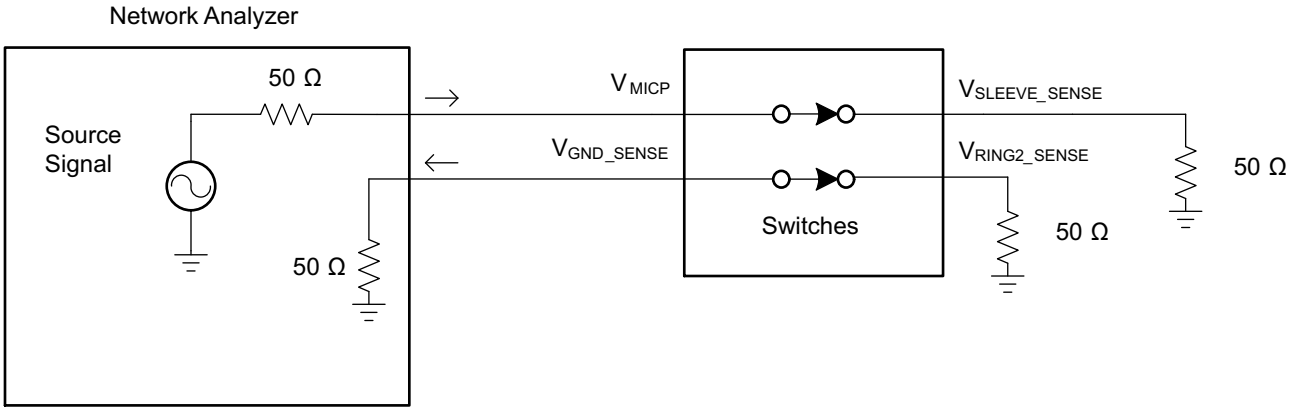

Figure 13. Channel Separation

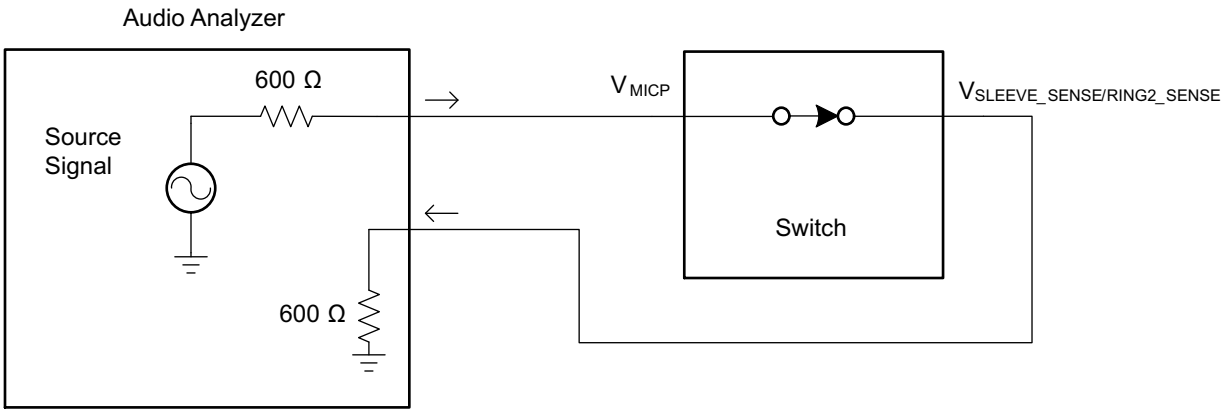

Figure 14. Total Harmonic Distortion (THD) and SNR

Parameter Measurement Information (continued)

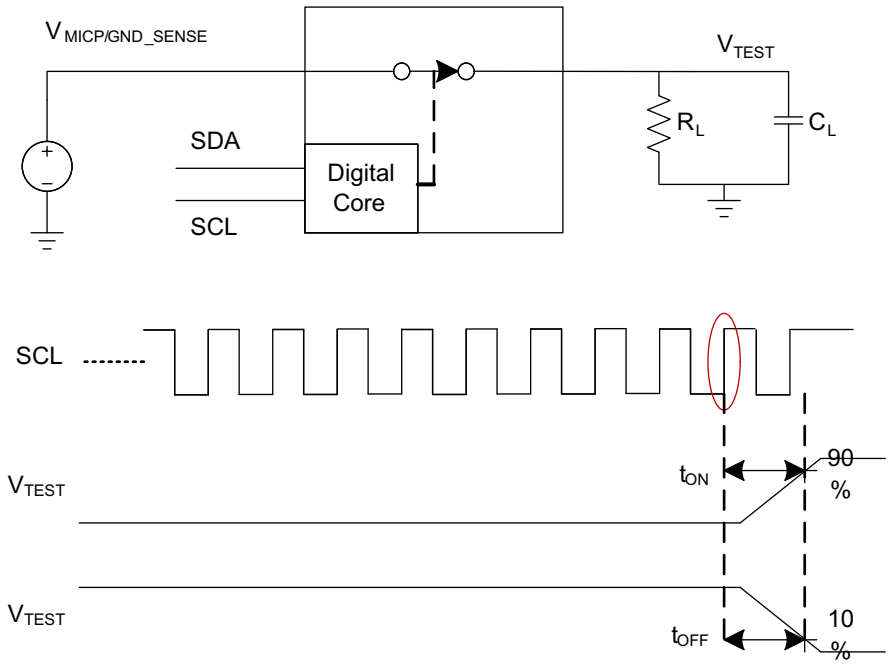

Figure 15. S3 t_{OFF}/t_{ON}

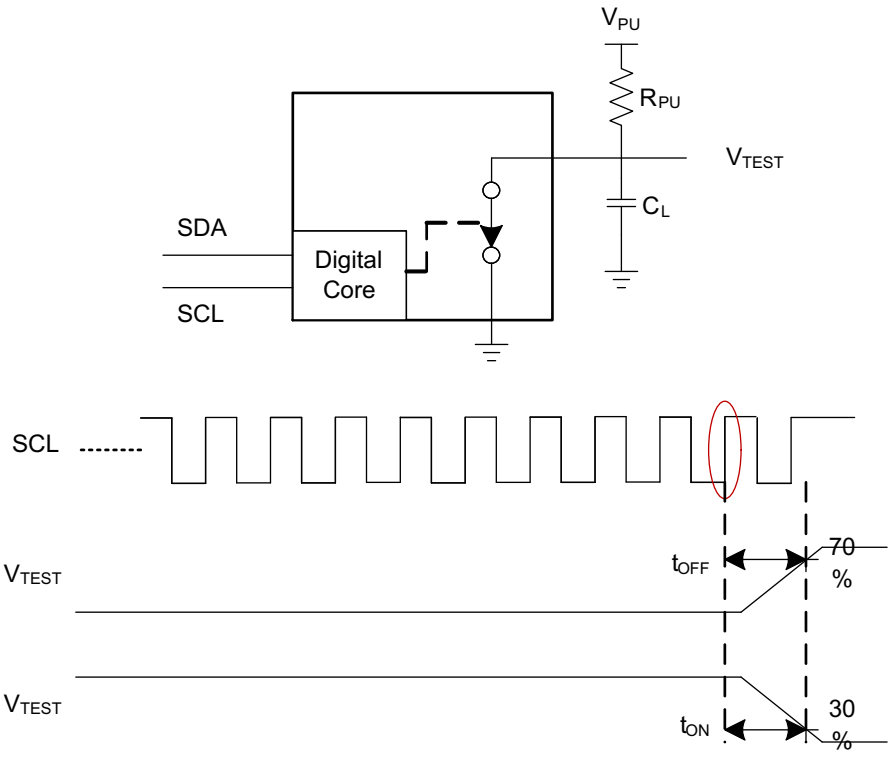

Figure 16. S1, S2, GNDFET and DFET t_{ON}/t_{OFF}

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9 Detailed Description

9.1 Overview

The TS3A227E is an autonomous audio accessory switch with adjustable de-bounce settings, ultra-low RON ground FETs, depletion FETs and manual I^2C control.

The detection sequence is initiated via the external $\overline{\text{DET\_TRIGGER}}$ pin or via I2C command. The device incorporates internal de-bounce timings that remove the need for external RC circuits, reducing cost and overall PCB footprint. Additionally all switches of the TS3A227E and the internal de-bounce timings can be controlled through I^2C.

Before an insertion, TS3A227E isolates the MICBIAS voltage output from the audio jack to remove click/pop noise that can be created during an insertion event. In addition the device also includes depletion FETs to ground the accessory SLEEVE and RING2 pins when VDD is not powered. This removes the humming noise that can be created when plugging an accessory into and unpowered system.

The TS3A227E detects the presence and configuration of the microphone in an attached headset upon insertion. Upon detection of a microphone the TS3A227E automatically connects a system analog microphone pin (MICP) to the appropriate audio jack connection. The device also automatically routes the device GNDA pin to the headset ground. After a 4-pole headset insertion the host can enable the Key Press detection feature of the TS3A227E.

The device also features an ultra-low power sleep mode to conserve battery life when an accessory is not inserted.

For FM transmission the ground FETs of the device can be used as an FM transmission path by placing the FM receiver and matching network on the GNDA pin. The FM support bit must be set to ‘1’ through I^2C for FM transmission to pass.

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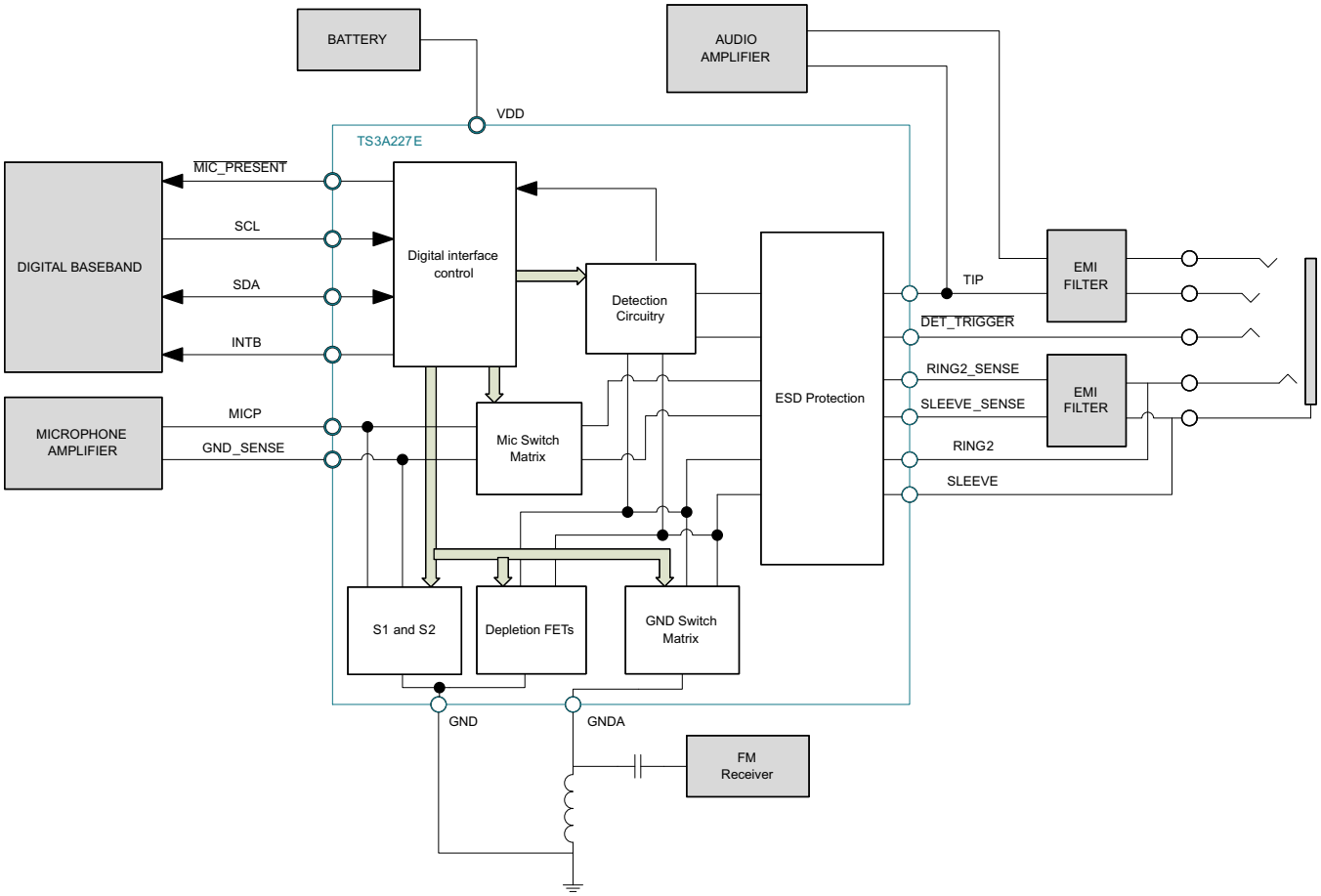
9.2 Functional Block Diagram



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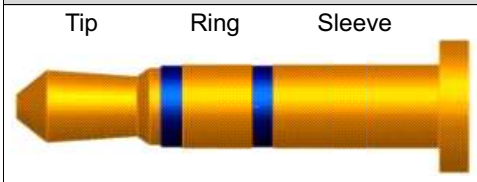
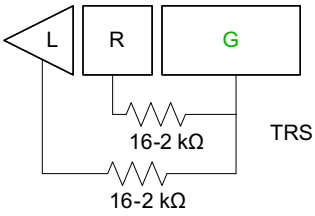
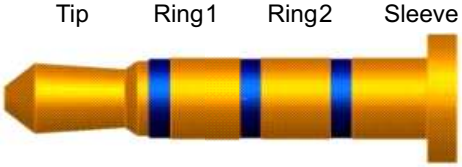
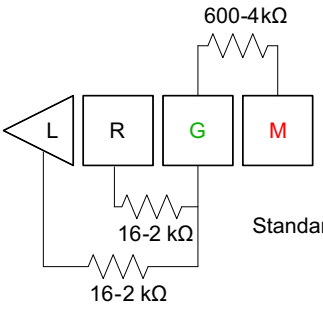
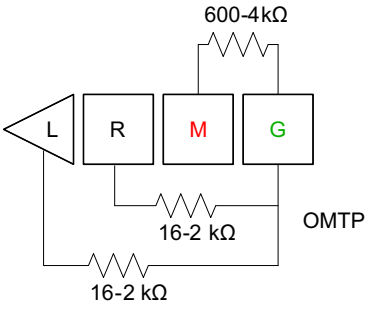
9.3 Feature Description

9.3.1 Accessory Configuration Detection

There are currently two difference configurations for headsets with microphones as shown in Table 1. Many codecs requires that the system designer make a tough decision via a hardware connection which headset they would like to support. This is done by directly connecting the microphone bias and the ground connections to the sleeve and ring2 pins of the audio jack. For the end user this leaves a headset standard as fully unsupported.

Table 1. Two Difference Configurations for Headsets

PHYSICAL CONNECTOR	INTERNAL IMPEDANCE NETWORK	PIN NAME	CONFIGURATION
 3-pole TRS		**Tip**	Audio Left
		Ring	Audio Right
		Sleeve	Ground
 4-pole TRRS		**Tip**	Audio Left
		Ring1	Audio Right
		Ring2	Ground
		Sleeve	Microphone
		**Tip**	Audio Left
		Ring1	Audio Right
		Ring2	Microphone
		Sleeve	Ground

The TS3A227E fills this system gap by detecting the presence and location of the microphone and automatically routing the MICBIAS and ground lines to support each headset. This enhances the overall user experience by allowing headsets from all manufacturers.

9.3.2 Optional Manual I²C Control

The TS3227E also features optional manual I²C control for enhanced system flexibility. This allows the system designer to manually control the switches and de-bounce settings at their discretion enabling the TS3A227E to adapt to unique use cases.

This is an optional feature that does not need to be used for the device to operate autonomously.

9.3.3 Adjustable De-bounce Timings

The TS3A227E features manual control of the insertion de-bounce timer with selectable values. The default insertion de-bounce timer is 90 ms.

This eliminates the need for external RC components which reduces BOM cost, the PCB footprint of the external RC components. Further information on how to select an appropriate de-bounce timer can be found in the application and implementation section.

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9.3.4 Key Press Detection

After a headset is inserted, the host can enable Key Press detection through the I^2C registers. This will configure the TS3A227E to detect up to 4 different keys and report when the key is pressed and released.

9.3.5 Click Pop Noise Reduction

During an accessory insertion and removal event the TS3A227E use special techniques to remove the click/pop noise that can occur with a traditional implementation creating a better user experience.

9.3.6 Power off Noise Removal

In a system that intends to support both headset types, the end user can place the system into sleep mode and leave a headset/speaker plugged into the audio jack. If the audio jack switch is turned off to conserve power in the sleep mode this would typically mean the headset/speaker ground would not be connected because there is no power to turn on the ground FETs. This creates an audible humming noise at the speaker/headset output that can be discomforting to listen to.

By utilizing always on depletion FETs this issue can be removed and the headset/speaker can be connected to ground even with the device unpowered.

9.3.7 Sleep Mode

The TS3A227E will automatically enter a low power sleep when no accessory is inserted and manual switch control is not enabled. After an accessory is inserted the device will wake, run detection, and configure the switches as necessary.

9.3.8 Codec Sense Line

In the complex systems of today, there is an increasing amount of ICs on any given board. The issue this creates is that a codec can be far away from the audio jack and there is a potential difference between the grounding of the codec and the grounding of the headset.

By incorporating a ground sense line into the TS3A227E the codec can compensate for this offset and create a higher quality audio experience.

9.3.9 FM Support

FM can be picked up using the headset ground line and passed through the ground FETs of the TS3A227E. By having a bandwidth of 200 MHz the full FM band can be passed through these FETs to a FM matching network and the FM receiver.

9.4 Device Functional Modes

9.4.1 Sleep Mode

The device will realize a sleep mode of 1 µA if the following are true:

- No accessory is inserted
- Manual Switch Control = ‘0’

The TS3A227E will respond to I2C communication and insertion events while in sleep mode. The user can set the de-bounce settings and device configuration as desired while in the sleep mode. If the user sets the Manual Switch Control bit to ‘1’ the device will turn on all blocks and come out of sleep mode.

If there is no accessory inserted and the users exits manual switch control, the switches will revert to the no-insertion state and all unnecessary blocks of the TS3A227E will turn off and enter the sleep mode.

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Device Functional Modes (continued)

9.4.2 Manual Switch Control

The TS3A227E supports manual switch control that can be utilized by setting Bit6 of the Device Settings 1 register to '1'.

Key operational characteristics of manual switch control are below.

1. Enabling the manual switch control does not disable automatic insertion and accessory type detection.
2. Manual Switch Control is blocked during accessory type detection which includes an automatic detection sequence or a manual SW triggered detection sequence. Any changes to the switch control registers, or setting the device to manual switch control will not update the switches until after the accessory type detection has completed.
3. Manual Switch Control is also blocked during de-bounce periods.
4. Excluding items 2 and 3 above, immediately after the system enables manual switch control the switch states will change to reflect the switch control registers. It is advised to set the desired state of the switches before enabling manual switch control.
5. Turning off the depletion FETs of the device will result in increased power consumption as defined in the electrical characteristics table.
6. Immediately upon setting Manual Switch Control = '0' the device will automatically configure the switches to the latest detection state. If an accessory is inserted but the TS3A227E has not run detection due to Auto_Det_EN = '0', the switch status will revert to the no insertion state.
7. The device cannot be in sleep mode and utilize manual switch control at the same time.

9.4.3 Manual Switch Control Use Cases

The table below captures what occurs after a 3-pole insertion with the Manual Switch Control, Auto DET Enable, and DET Trigger bits set to the following before an insertion.

MANUAL SWITCH CONTROL	AUTO DET EN	DET TRIGGER (SW)		DOES TYPE DETECTION RUN	SWITCH STATUS AFTER INSERTION	DET TRIGGER (SW) AFTER INSERTION
0	0	0		no	No-insertion	0
0	0	1		yes	3-pole config	0
0	1	0		yes	3-pole config	0
0	1	1		yes	3-pole config	0
1	0	0		no	Switch control registers	0
1	0	1		yes	Switch control registers	0
1	1	0		yes	Switch control registers	0
1	1	1		yes	Switch control registers	0

The table below captures the switch and relevant register outputs for sequence 1.

EVENT NO.	EVENT DESCRIPTION		SWITCH STATUS	3-POLE BIT	4-POLE STANDARD BIT	4-POLE OMTP BIT
1	Device powers up		No-insertion	0	0	0
2	User sets Auto DET Enable = '0'		No-insertion	0	0	0
3	3-pole accessory is inserted		No-insertion	0	0	0
4	System sets Manual Switch Control = '1'		System controlled	0	0	0
5	System sets switch control registers = 0xFF		System controlled	0	0	0
6	System sets Manual Switch Control = '0'		No-insertion	0	0	0

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In sequence 1 at event 3 the switch status does not change because the system set the Auto DET Enable = '0'. When the accessory is inserted we will not run detection and not change the switches because of this.

At event 6 the system turns off manual switch control, the switch state reverts back to the No-insertion state because the TS3A227E has not ran detection.

The table below captures the switch and relevant register outputs for sequence 2.

EVENT NO.	EVENT DESCRIPTION		SWITCH STATUS AFTER EVENT	3-POLE BIT	4-POLE STANDARD BIT	4-POLE OMTP BIT
1	Device powers up		No-insertion	0	0	0
2	User sets Auto DET Enable = '0'		No-insertion	0	0	0
3	3-pole accessory is inserted		No-insertion	0	0	0
4	System sets Manual Switch Control = '1'		System controlled	0	0	0
5	System sets switch control registers = 0xFF		System controlled	0	0	0
6	System sets DET Trigger = '1'		System controlled	1	0	0
7	System sets Manual Switch Control = '0'		3-pole configuration	1	0	0

In sequence 2 at event 3 the switch status does not change because the system set the Auto DET Enable = '0'. When the accessory is inserted we will not run detection and not change the switches because of this.

At event 6 the system turns triggers a manual type detection and the TS3A227E detects a 3-pole accessory. The switch state will remain in the system controlled state.

At event 7 the system exits manual switch control. The switch status will then change back to the last detection state. Because detection was ran at event 6 and a 3-pole was detected, the switch state will reflect that of the 3-pole switch configuration.

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9.4.4 FM Support Mode

FM support mode needs to be entered via I2C through the Device Settings register. This will turn off the depletion switches when an accessory is inserted, eliminating the extra ground path. The ground line of the headset/headphone is used for FM transmission. This signal must pass through the TS3A227E ground FETs as shown in Figure 17 where the red line indicates the transmission path.

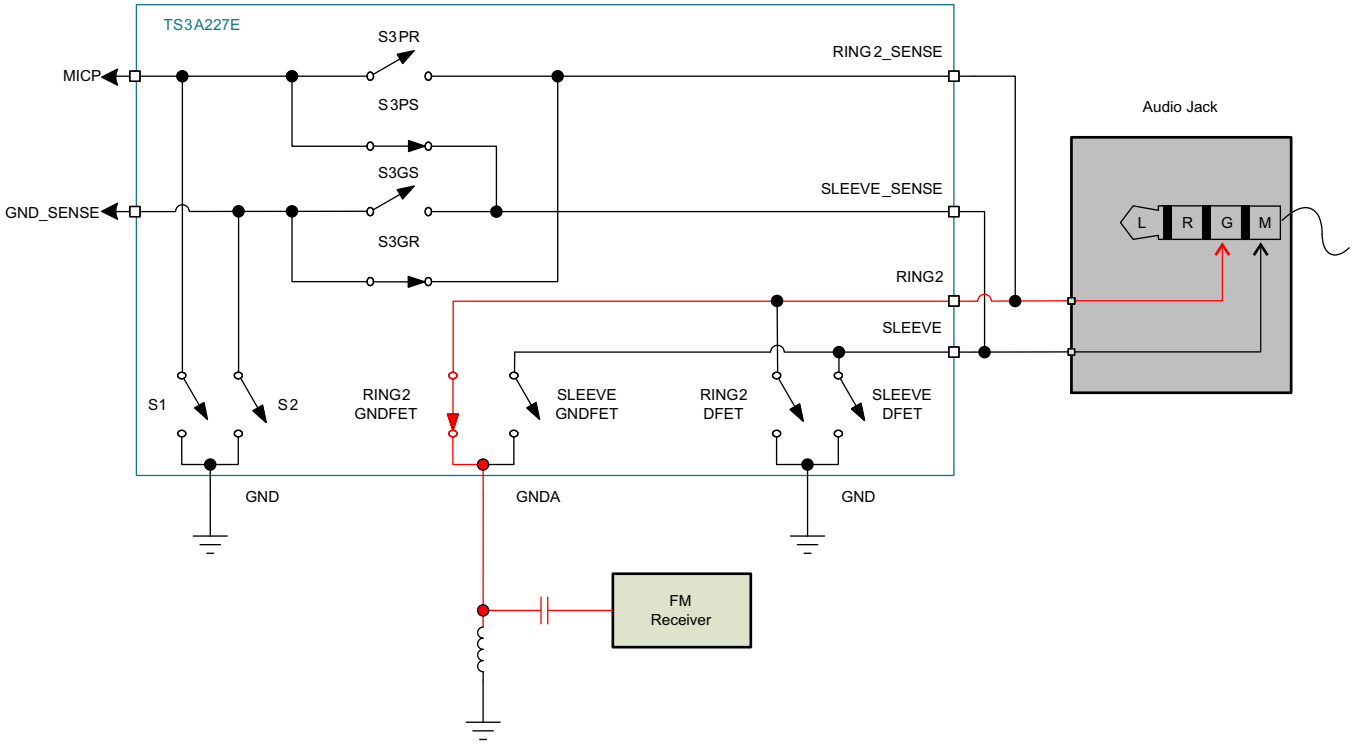

Figure 17. FM Support Transmission Path

NOTE

FM support should be enabled before an accessory is inserted. Toggling the FM support bit after a headset is inserted can cause a pop noise to be heard by the end user.

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9.5 Register Maps

The I^2C address of the TS3A227E is b'0111011X or 77h read and 76h write.

Addr (xxh)	Name	Type	Reset	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	Device ID	R	11h	0	0	0	1	0	0	0	1
01h	Interrupt	R	00h	Reserved					ADC Conversion	DC	Ins/Rem Event
02h	Key Press Interrupts	R	00h	Key 4 Release	Key 4 Press	Key 3 Release	Key 3 Press	Key 2 Release	Key 2 Press	Key 1 Release	Key 1 Press
03h	Interrupt Disable	R/W	08h	Reserved				$\overline{INT}$ Disable	ADC Conversion $\overline{INT}$ Disable	DC $\overline{INT}$ Disable	Ins/Rem Event $\overline{INT}$ Disable
04h	Device Settings	R/W	23h	Reset	Manual Switch Control	Auto DET Enable	DET Trigger	FM Support	Insertion De-bounce Time		
05h	Device Setting 1	R/W	00h	Reserved					Key Press Enable	Raw Data En	ADC Trigger
06h	Device Setting 2	R/W	0Eh	Reserved		MICBIAS Setting			Key Release De-bounce	Key Press De-bounce	
07h	Switch Control 1	R/W	00h	Reserved		SLEEVE GNDFET	RING2 GNDFET	SLEEVE DFET	RING2 DFET	Switch 2	Switch 1
08h	Switch Control 2	R/W	00h	Reserved				S3PS	S3PR	S3GS	S3GR
09h	Switch Status 1	R	0Ch	Reserved		SLEEVE GNDFET	RING2 GNDFET	SLEEVE DFET	RING2 DFET	Switch 2	Switch 1
0Ah	Switch Status 2	R	00h	Reserved				S3PS	S3PR	S3GS	S3GR
0Bh	Accessory Status	R	00h	Reserved				Insertion Status	4-Pole Standard	4-pole OMTP	3-pole
0Ch	ADC Output	R	00h	ADC							
0Dh	Threshold 1	R/W	20h	KP Threshold 1							
0Eh	Threshold 2	R/W	40h	KP Threshold 2							
0Fh	Threshold 3	R/W	68h	KP Threshold 3							

Interrupt and Key Press Interrupt register notes:

- The device will continue to automatically run type detection and key press detection even if the host has not serviced the interrupts.
- Consecutive reads of an interrupt register at 400 kHz will not allow time for the internal registers to clear and will appear. The internal digital core requires 200 µs to clear the register after it has been read.

9.6 Register Field Descriptions

9.6.1 Device ID Register Field Descriptions (Address 00h)

Figure 18. Device ID Register Field Descriptions (Address 00h)

Bit	Field	Type	Reset	Description
7-0	Device ID	R	11h	Unique Revision number

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9.6.2 Interrupt Register Field Descriptions (Address 01h)

Table 2. Interrupt Register Field Descriptions (Address 01h)

Bit	Field	Type	Reset	Description
7-3	Reserved	R	0h	
2	ADC Conversion	R	0h	ADC Conversion complete Interrupt. Flagged after a manual ADC conversion is complete. Interrupt bit is cleared after being read through I2C or after a removal event. 0h = Default state 1h = ADC Conversion Complete
1	DC	R	0h	Detection Complete interrupt. Flagged after detection is completed for an insertion sequence. This bit is also flagged after completion of a manually triggered detection. Interrupt bit is cleared after being read through I2C or after a removal event. 0h = Default state 1h = Detection Completed
0	Ins/Rem Event	R	0h	Insertion or removal interrupt indicator. This bit is set if there is an insertion or removal event. The Insertion status bit of the Accessory Status register (0Bh) must be checked if this bit is set. Interrupt bit is cleared after being read through I2C 0h = Default state 1h = Accessory has been inserted or removed

9.6.3 Key Press Interrupt Register Field Descriptions (Address 02h)

Table 3. Key Press Interrupt Register Field Descriptions (Address 02h)

Bit	Field	Type	Reset	Description
7	Key 4 Release	R	0h	This interrupt bit is set after the user has released key 4 on the accessory for a duration longer than the Key Release De-bounce timer. This bit will auto-clear on the following conditions: • Host reads the register through I^2C • The KP Enable bit is set to ‘0’ — The KP Enable bit is set to ‘0’ automatically after a removal • The Key 4 press bit is set ot '1' 0h = Default State 1h = Key 4 was released
6	Key 4 Press	R	0h	This interrupt bit is set after the user has pressed key 4 on the accessory for a duration longer than the Key Press De-bounce timer. This bit will auto-clear on the following conditions: • Host reads the register through I^2C • The KP Enable bit is set to ‘0’ — The KP Enable bit is set to ‘0’ automatically after a removal 0h = Default State 1h = Key 4 was released
5	Key 3 Release	R	0h	This interrupt bit is set after the user has pressed Key 3 on the accessory for a duration longer than the Key Release De-bounce timer. This bit will auto-clear on the following conditions: • Host reads the register through I^2C • The KP Enable bit is set to ‘0’ — The KP Enable bit is set to ‘0’ automatically after a removal • The Key 3 Press bit is set to ‘1’ 0h = Default State 1h = Key 3 was released

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Table 3. Key Press Interrupt Register Field Descriptions (Address 02h) (continued)

Bit	Field	Type	Reset	Description
4	Key 3 Press	R	0h	This interrupt bit is set after the user has pressed Key 3 on the accessory for a duration longer than the Key Press De-bounce timer. This bit will auto-clear on the following conditions: • Host reads the register through I^2C • The KP Enable bit is set to '0' — The KP Enable bit is set to '0' automatically after a removal 0h = Default State 1h = Key 3 was released
3	Key 2 Release	R	0h	This interrupt bit is set after the user has pressed Key 2 on the accessory for a duration longer than the Key Release De-bounce timer. This bit will auto-clear on the following conditions: • Host reads the register through I^2C • The KP Enable bit is set to '0' — The KP Enable bit is set to '0' automatically after a removal • The Key 2 Press bit is set to '1' 0h = Default State 1h = Key 2 was released
2	Key 2 Press	R	0h	This interrupt bit is set after the user has pressed Key 2 on the accessory for a duration longer than the Key Press De-bounce timer. This bit will auto-clear on the following conditions: • Host reads the register through I^2C • The KP Enable bit is set to '0' — The KP Enable bit is set to '0' automatically after a removal 0h = Default State 1h = Key 2 was released
1	Key 1 Release	R	0h	This interrupt bit is set after the user has pressed Key 1 on the accessory for a duration longer than the Key Release De-bounce timer. This bit is used for raw data release events. This bit will auto-clear on the following conditions: • Host reads the register through I^2C • The KP Enable bit is set to '0' — The KP Enable bit is set to '0' automatically after a removal • The Key 1 Press bit is set to '1' 0h = Default State 1h = Key 1 was released
0	Key 1 Press	R	0h	This interrupt bit is set after the user has pressed Key 1 on the accessory for a duration longer than the Key Press De-bounce timer. This bit is used for raw data press events. This bit will auto-clear on the following conditions: • Host reads the register through I^2C • The KP Enable bit is set to '0' — The KP Enable bit is set to '0' automatically after a removal 0h = Default State 1h = Key 1 was released

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9.6.4 Interrupt Disable Register Field Descriptions (Address 03h)

Table 4. Interrupt Disable Register Field Descriptions (Address 03h)

Bit	Field	Type	Reset	Description
7-3	Reserved	R	0h	
+3	$\overline{\text{INT}}$ Disable	R/W	1h	Enables or disables all interrupts. Disabling the interrupts will cause the $\overline{\text{INT}}$ to not assert but the bits will still populate. 0h = interrupts are enabled 1h = interrupts are disabled
2	ADC Conversion $\overline{\text{INT}}$ Disable	R/W	0h	Enables or disables the ADC conversion interrupt. Disabling the interrupt will cause $\overline{\text{INT}}$ to not assert but the interrupt bit will still be set . In the use case that this bit is == '1' and a key is pressed, the Key Press interrupt will still assert the $\overline{\text{INT}}$ pin. If the host issues a software ADC trigger after the key has been pressed, the interrupt will not assert as that ADC conversion is the only interrupt present. 0h = ADC Conversion interrupt is enabled 1h = ADC Conversion interrupt is disabled
1	DC $\overline{\text{INT}}$ Disable	R/W	0h	Enables or disables the DC interrupt. Disabling the interrupt will cause $\overline{\text{INT}}$ to not assert but the interrupt bit will still be set. 0h = DC interrupt is enabled 1h = DC interrupt is disabled
0	Ins/Rem Event $\overline{\text{INT}}$ Disable	R/W	0h	Enables or disables the Ins/Rem Event interrupt. Disabling the interrupt will cause $\overline{\text{INT}}$ to not assert but the interrupt bit will still be set. 0h = Ins/Rem Event interrupt is enabled 1h = Ins/Rem Event interrupt is disabled

9.6.5 Device Settings Field Descriptions (Address 04h)

Table 5. Device Settings Field Descriptions (Address 04h)

Bit	Field	Type	Reset	Description
7	Reset	R/W	0h	Initiates software reset of the TS3A227E. This will interrupt any on-going operation internal to the device. 0h = Default state 1h = Initiates a reset
6	Manual Switch Control	R/W	0h	Enables Manual control of the TS3A227E switches. After enabling manual switch control the switch status will immediately reflect the values in the switch control registers provided accessory type. 0h = Manual switch control disabled 1h = Manual switch control enabled
5	Auto DET Enable	R/W	1h	Controls whether detection is automatically ran after an insertion. 0h = Auto accessory detection is disabled 1h = Auto accessory detection is enabled
4	DET Trigger	R/W	0h	Manually triggers detection. This bit is auto cleared after detection is completed. A DET Trigger request will be ignored in the following cases: • A detection event is currently being service. • The interrupt register is not cleared (Register 02h must be = 00h) • There is no accessory inserted (/DET_TRIGGER is high) 0h = Default value 1h = Manually trigger detection
3	FM Support	R/W	0h	Turns on FM support. This will turn off the depletion FETs if any accessory is inserted allowing FM transmission through the ground FETs at the cost of increased current consumption. 0h = FM not supported and depletion FETs are on after an insertion 1h = FM supported and depletion FETs are off after an insertion

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Table 5. Device Settings Field Descriptions (Address 04h) (continued)

Bit	Field	Type	Reset	Description
2.0	Insertion De-bounce Time	R/W	3h	Controls the insertion de-bounce timer. Values below are typical values that have ±30% variation. Values in addition have a ±1 ms variation though this will only really affect the 2 ms timer. 0h = 2 ms 1h = 30 ms 2h = 60 ms 3h = 90 ms 4h = 120 ms 5h = 150 ms 6h = 1 s 7h = 2 s

9.6.6 Key Press Settings 1 Field Descriptions (Address 05h)

Table 6. Device Settings 1 Field Descriptions (Address 05h)

Bit	Field	Type	Reset	Description
7-3	Reserved	R	0h	
2	Key Press Enable	R/W	0h	Enables the Key Press detection of the TSA227E. This bit auto clears after a removal event. If the Key Press Enable bit is set '1' and the Manual Switch Control bit is set to '1', the S3 matrix must be in one of the two correct position as described in the Key Press Detection section for the TS3A227E to run key press detection. 0h = Default state 1h = Enables Key Press detection
1	Raw Data En	R/W	0h	Enables the Raw data mode for Key Press Detection. This bit auto clears if the Key Press Enable bit is set to '0'. Enabling raw data mode will not clear the KP interrupt register. After enabling Raw Data any key press and release event is recorded using the Key 1 Press and Key 2 Press Release event. The ADC conversion will be recorded in the ADC output register. 0h = Raw Data is not enabled 1h = Raw Data is enabled
0	ADC Trigger	R/W	0h	Causes a manual ADC trigger if the Key Press Enable and Raw Data EN bits are both set to '1'. After the ADC conversion is complete the ADC Conversion interrupt will be set and the ADC Output register will be populated. This bit auto clears after the ADC Conversion is complete. A new ADC Conversion can be initiated even if the ADC Conversion interrupt has not been serviced. 0h = Default State 1h = Triggers ADC conversion

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9.6.7 Key Press Settings 2 Field Descriptions (Address 06h)

Table 7. Device Settings 2 Field Descriptions (Address 06h)

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	
5-3	MICBIAS Setting	R/W	1h	This controls the key press threshold. Set this setting closest to the intended MICBIAS voltage 0h = 2.1 V 1h = 2.2 V (Default) 2h = 2.3 V 3h = 2.4 V 4h = 2.5 V 5h = 2.6 V 6h = 2.7 V 7h = 2.8 V
2	Key Release De-bounce	R/W	1h	Controls the Key-Release de-bounce timer. Values below are typical values that have ±30% variation. Values in addition have a ±1 ms variation though this will only really affect the 2 ms timer. 0h = 2 ms 1h = 20 ms (Default)
1-0	Key Press De-bounce	R/W	2h	Controls the key press de-bounce timer. Values below are typical values that have ±30% variation. Values in addition have a ±1 ms variation though this will only really affect the 2 ms timer. 0h = 2 ms 1h = 40 ms 2h = 80 ms (Default) 3h = 120 ms

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9.6.8 Switch Control 1 Field Descriptions (Address 07h)

Table 8. Switch Control 1 Field Descriptions (Address 07h)

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	
5	SLEEVE GNDFET	R/W	0h	Configures the state of the SLEEVE GNDFET if manual switch control is enabled. If manual switch control is not enabled this bit is ignored. 0h = SLEEVE GNDFET switch off 1h = SLEEVE GNDFET switch on
4	RING2 DFET	R/W	0h	Configures the state of the RING2 GNDFET if manual switch control is enabled. If manual switch control is not enabled this bit is ignored. 0h = RING2 GNDFET switch off 1h = RING2 GNDFET switch on
3	SLEEVE DFET	R/W	0h	Configures the state of the SLEEVE DFET if manual switch control is enabled. If manual switch control is not enabled this bit is ignored. 0h = SLEEVE DFET switch off 1h = SLEEVE DFET switch on
2	RING2 DFET	R/W	0h	Configures the state of the RING2 DFET if manual switch control is enabled. If manual switch control is not enabled this bit is ignored. 0h = RING2 DFET switch off 1h = RING2 DFET switch on
1	Switch 2	R/W	0h	Configures the state of the Switch 2 if manual switch control is enabled. If manual switch control is not enabled this bit is ignored. 0h = Switch 2 off 1h = Switch 2 on
0	Switch 1	R/W	0h	Configures the state of the Switch 1 if manual switch control is enabled. If manual switch control is not enabled this bit is ignored. 0h = Switch 1 off 1h = Switch 1 on

9.6.9 Switch Control 2 Field Descriptions (Address 08h)

Table 9. Switch Control 2 Field Descriptions (Address 08h)

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0h	
3	S3PS	R/W	0h	Configures the state of the S3PS if manual switch control is enabled. If manual switch control is not enabled this bit is ignored. 0h = S3PS switch off 1h = S3PS switch on
2	S3PR	R/W	0h	Configures the state of the S3PR if manual switch control is enabled. If manual switch control is not enabled this bit is ignored. 0h = S3PR switch off 1h = S3PR switch on
1	S3GS	R/W	0h	Configures the state of the S3GS if manual switch control is enabled. If manual switch control is not enabled this bit is ignored. 0h = S3GS off 1h = S3GS on
0	S3GR	R/W	0h	Configures the state of the S3GR if manual switch control is enabled. If manual switch control is not enabled this bit is ignored. 0h = S3GR off 1h = S3GR on

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9.6.10 Switch Status 1 Field Descriptions (Address 09h)

Table 10. Switch Status 1 Field Descriptions (Address 09h)

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	
5	SLEEVE GNDFET	R	0h	Indicates the status of SLEEVE GNDFET 0h = SLEEVE GNDFET switch is off 1h = SLEEVE GNDFET switch is on
4	RING2 GNDFET	R	0h	Indicates the status of RING2 GNDFET 0h = RING2 GNDFET switch is off 1h = RING2 GNDFET switch is on
3	SLEEVE DFET	R	1h	Indicates the status of SLEEVE DFET 0h = SLEEVE DFET switch is off 1h = SLEEVE DFET switch is on
2	RING2 DFET	R	1h	Indicates the status of RING2 DFET 0h = RING2 DFET switch is off 1h = RING2 DFET switch is on
1	Switch 2	R	0h	Indicates the status of Switch 2 0h = Switch 2 is off 1h = Switch 2 is on
0	Switch 1	R	0h	Indicates the status of Switch 1 0h = Switch 1 is off 1h = Switch 1 is on

9.6.11 Switch Status 2 Field Descriptions (Address 0Ah)

Table 11. Switch Status 2 Field Descriptions (Address 0Ah)

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0h	
3	S3PS	R	0h	Indicates the status of S3PS 0h = S3PS switch is off 1h = S3PS switch is on
2	S3PR	R	0h	Indicates the status of S3PR 0h = S3PR switch is off 1h = S3PR switch is on
1	S3GS	R	0h	Indicates the status of S3GS 0h = S3GS is off 1h = S3GS is on
0	S3GR	R	0h	Indicates the status of S3GR 0h = S3GR is off 1h = S3GR is on

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9.6.12 Detection Results Field Descriptions (Address 0Bh)

Table 12. Detection Results Field Descriptions (Address 0Bh)

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0h	
3	Insertion Status	R	0h	Indicates if an accessory is inserted the jack or not. This bit is set to the corresponding state after an accessory is inserted or removed and should be read after the Ins/Rem Event interrupt has been set to '1'. 0h = An accessory is not in the jack 1h = An accessory is in the jack
2	4-pole Standard	R	0h	Indicates if a 4-pole Standard headset is detected. Bit is set after a completed detection sequence. 0h = Default state 1h = 4-pole standard headset detected
1	4-pole OMTP	R	0h	Indicates if a 4-pole OMTP headset is detected. Bit is set after a completed detection sequence. 0h = Default state 1h = 4-pole OMTP headset detected
0	3-pole	R	0h	Indicates if a 3-pole headphone is detected. Bit is set after a completed detection sequence. 0h = Default state 1h = 3-pole headphone detected

9.6.13 ADC Output Field Descriptions (Address 0Ch)

Table 13. ADC Output Field Descriptions (Address 0Ch)

Bit	Field	Type	Reset	Description
7-1	ADC	R/W	00h	This field contains the output of the key press detection ADC as described in the key press detection register
0	Reserved	R	0h	

9.6.14 Threshold 1 Field Descriptions (Address 0Dh)

Table 14. Threshold 1 Field Descriptions (Address 0Dh)

Bit	Field	Type	Reset	Description
7-01	KP Threshold 1	R/W	20h	This field sets the key 1 and key 2 boundary threshold. This value must always be lower than the Threshold 2 register for proper operation.
0	Reserved	R	0h	

9.6.15 Threshold 2 Field Descriptions (Address 0Eh)

Table 15. Threshold 2 Field Descriptions (Address 0Eh)

Bit	Field	Type	Reset	Description
7-1	KP Threshold 2	R/W	40h	This field sets the key 2 and key 3 boundary threshold. This value must always be lower than the Threshold 3 register and higher than the threshold 2 register for proper operation.
0	Reserved	R	0h	

9.6.16 Threshold 3 Field Descriptions (Address 0Fh)

Table 16. Threshold 3 Field Descriptions (Address 0Fh)

Bit	Field	Type	Reset	Description
7-1	KP Threshold 3	R/W	68h	This field sets the key 3 and key 4 boundary threshold. This value must always be higher than the Threshold 2 register for proper operation.
0	Reserved	R	0h	

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10 Application and Implementation

10.1 Application Information

Figure 19 shows how a standard application schematic for the TS3A227E. The DSBGA package pin connections will be the same except for the lack of thermal pad. The following sections discuss how the TS3A227E works with different headsets and how the key press detection operates.

10.2 Typical Application

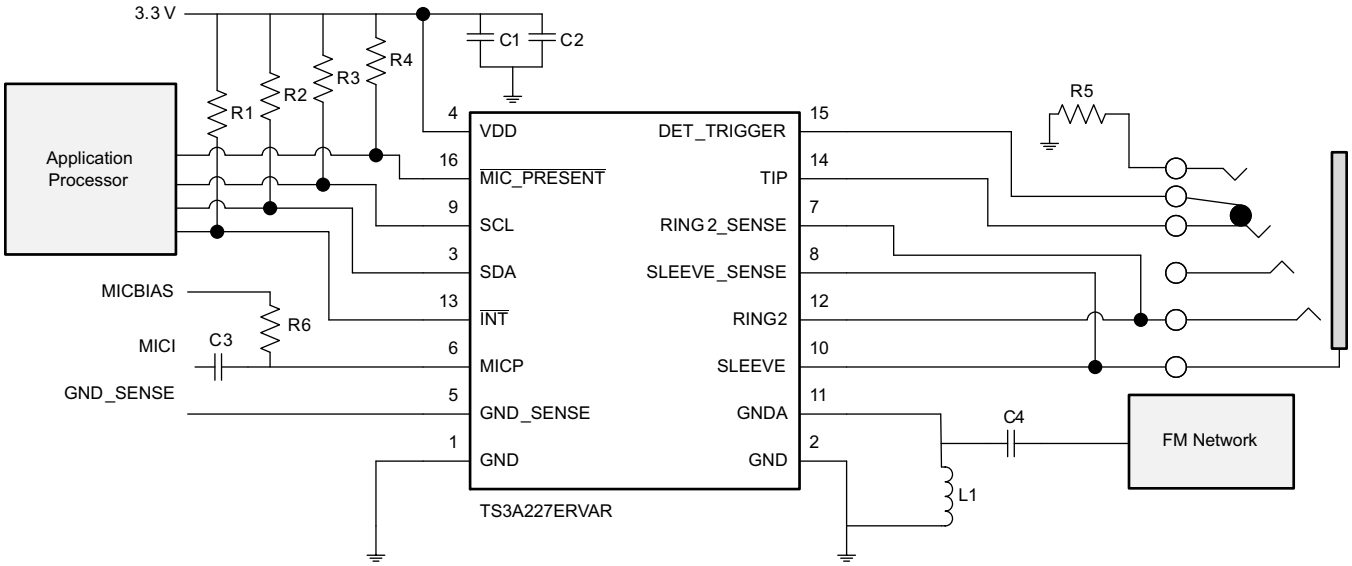

Figure 19. Typical Application Schematic

Table 17. Component List

COMPONENT	VALUE	NOTES
R1	4.7 kΩ	Pullup resistor must be sized to not exceed max IOL specification for $\overline{INT}$ pin
R2	4.7 kΩ	Pullup resistor must be sized to not exceed max IOL specification for $\overline{INT}$ pin
R3	4.7 kΩ	Pullup resistor must be sized to not exceed max IOL specification for $\overline{INT}$ pin
R4	4.7 kΩ	Pullup resistor must be sized to not exceed max IOL specification for $\overline{INT}$ pin
R5	10 kΩ	Pulldown resistor for high to low transition on $\overline{DET\_TRIGGER}$
R6	2.2 kΩ ±1%	MICBIAS pullup resistor must be ±1% for Key Press Detection to function properly
C1	10 µF	De-coupling capacitor for V_{DD}
C2	100 nF	De-coupling capacitor for V_{DD}
C3	1 µF	Value can vary depending on codec needs
C4	47 nF	Value can vary depending on FM matching network needs. If FM transmission is not being supported by the application this capacitor is not needed
L1	180 nF	Value can vary depending on FM matching network needs. If FM transmission is not being supported by the application this inductor is not needed and GNDA must be shorted to GND

10.2.1 Design Requirements

10.2.1.1 Standard I²C Interface Details

The bi-directional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

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I²C communication with this device is initiated by the master sending a START condition, a high-to-low transition on the SDA line while the SCL line is high. After the start condition, the device address byte is send, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte (0x77 read, 0x76 write), this device responds with an ACK, a low on the SDA line during the high of the ACK-related clock pulse.

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP).

A Stop condition, a low-to-high transition on the SDA line while the SCL line is high, is sent by the master. The number of data bytes transferred between the start and the stop conditions from the transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period. Setup and fold times must be taken into account.

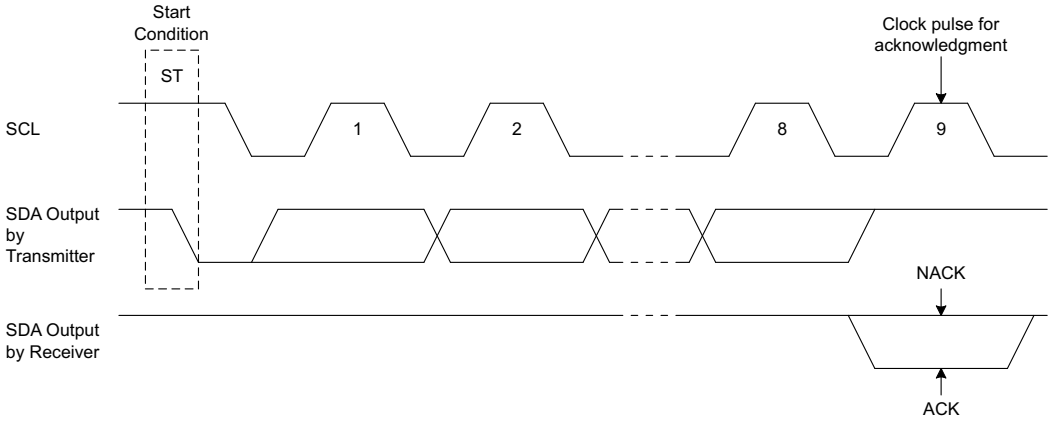

Figure 20. Acknowledgment on the I²C Bus

10.2.1.2 Write Operations

Data is transmitted to the TS3A227E by send the device salve address and setting the LSB to a logic 0. The command byte is sent after the address and determines which register receives the data that follows the command byte. The next byte is written to the specified register on the rising edge of the ACK clock pulse. See Figure 2 and Figure 3 for different modes of write operations.

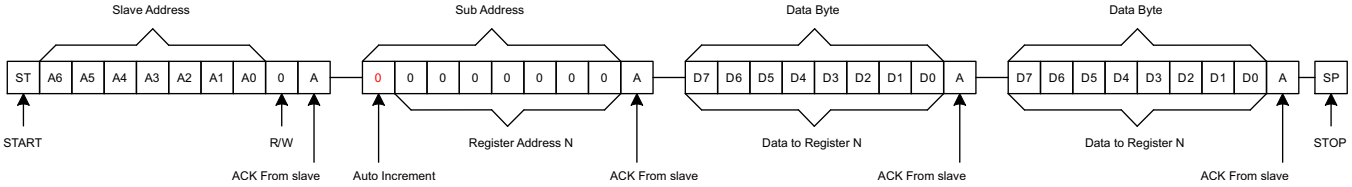

Figure 21. Repeated Data Write to a Single Register

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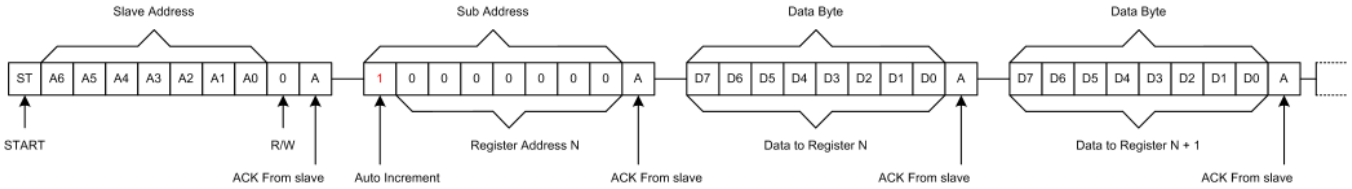

Figure 22. Burst Data Write to Multiple Registers

10.2.1.3 Read Operations

The bus master must send the TS3A227E slave address with the LSB set to logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device slave address is sent again but this time the LSB is set to logic 1. Data from the register defined by the command byte then is sent back to the host by the TS3A227E. Data is clicked into the SDA output shift register on the rising edge of the ACK clock pulse. Figure 23 and Figure 24 show read operations that use a restart between the sub-address write and the read operation. A Stop and start condition between the sub-address write and the read operation is also acceptable.

Notes:

1. SDA is pulled low on ACK from the slave or master.
2. Register write always a require sub-address write before writing the first data.
3. Repeated data writes to a single register continue indefinitely until n I^2C Stop or Re-start.
4. Repeated data reads from a single register continue indefinitely until an I^2C NACK is received from the master
5. Burst data writes start at the specified register address, then advance to the next register address, even to the read-only registers and continue until the Stop or Re-start. For the read-only registers, data write appears to occur, although the register contents are not changed by the write operations.
6. Burst data reads start at the specified register address, then advance to the next register address and continues until an I^2C NACK is received from the master.

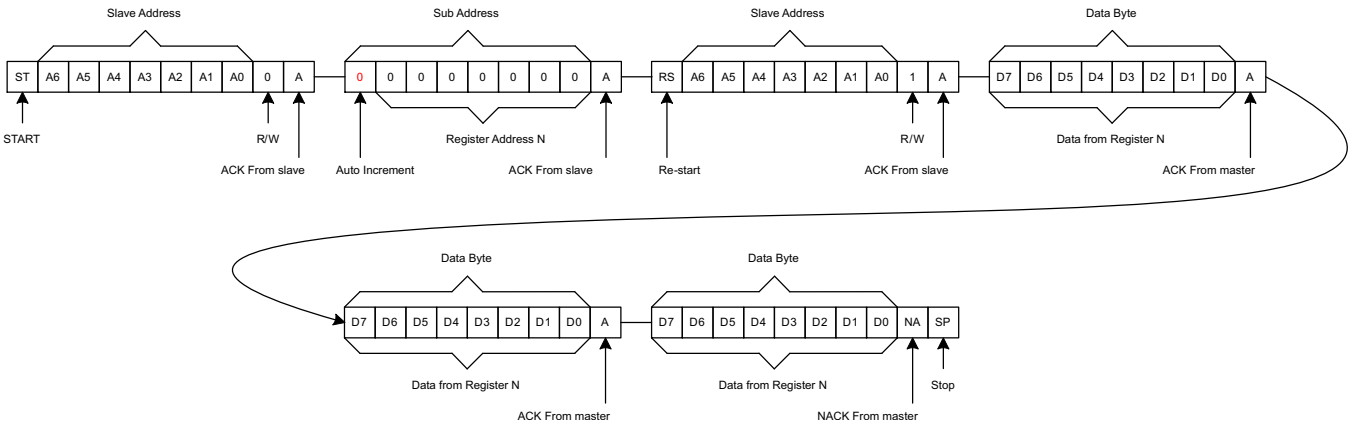

Figure 23. Repeated Data Read From a Single Register

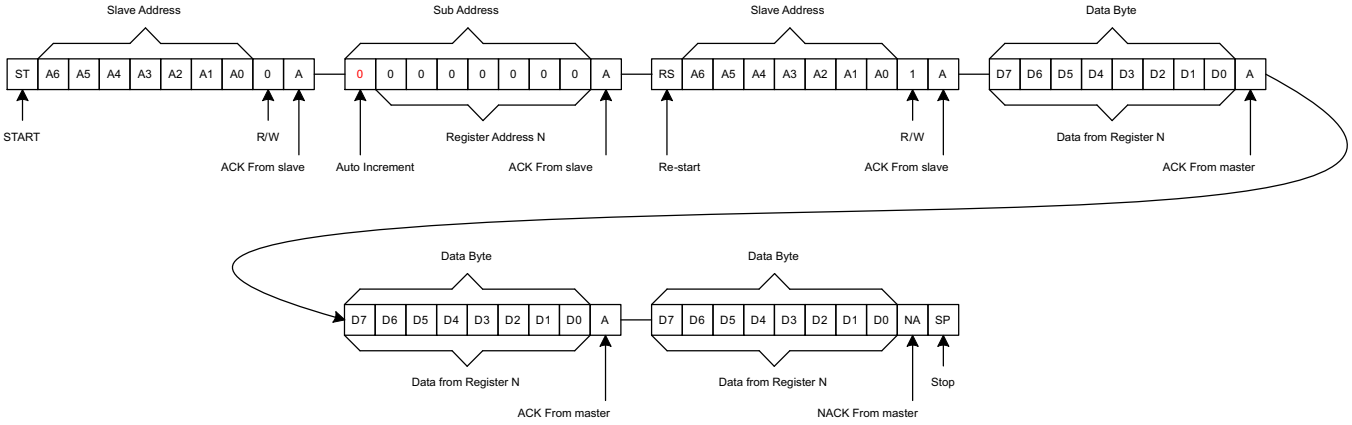

Figure 24. Burst Data Read From Multiple Registers

10.2.2 Detailed Design Procedure

10.2.2.1 Accessory Insertion

The TS3A227E monitors the $\overline{\text{DET\_TRIGGER}}$ pin to determine when an insertion event occurs. A high to low transition one the $\overline{\text{DET\_TRIGGER}}$ pin will start the internal de-bounce timer (default 90 ms). This transition is shown in Figure 19. Once the de-bounce timer has expired, it is determined that an accessory is inserted and the detection algorithm is performed to determine what the accessory is and where the ground line is located.

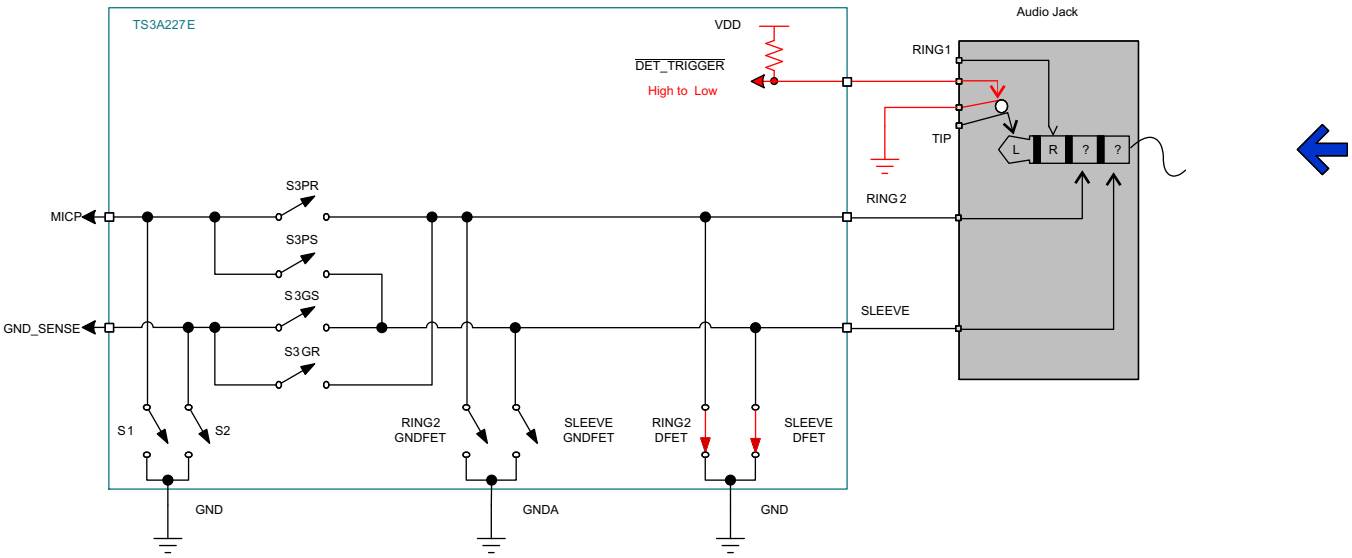

Figure 25. DET_TRIGGER Transition Diagram

Once a $\overline{\text{DET\_TRIGGER}}$ transition has occurred, any I^2C register changes will not be serviced until after the de-bounce and detection sequence have completed. If $\overline{\text{DET\_TRIGGER}}$ transitions from Low to High before the de-bounce period has expired. The I2C register changes will be serviced before a new de-bounce timer is started from another High to Low transition on the $\overline{\text{DET\_TRIGGER}}$ pin. The I2C communication has to complete before the next High to Low transition to take effect.

10.2.2.2 Audio Jack Selection

The audio jack the system uses plays a key role in how the system performs and the experience the end user has with the equipment. In real-world scenarios a user might plug in the headset to the audio jack very slowly. This creates a challenging case for the TS3A227E detection mechanism and detection error can occur if care is not taken when designing the components around the TS3A227E.

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The main concern for slow plug-in is the detection process may have already started before the headset is fully inserted into the jack. If the detection is running with the headset out of position, a false impedance measurement may occur. For best performance a jack should be chosen that puts the detection mechanism on the TIP pin at the end of physical jack to ensure that it is fully inserted.

The TS3A227E EVM contains test points for all the jack pins and can be blue wired to prototype audio jacks for testing.

10.2.2.3 Switch Status

Table 18 depicts the switch status for each device configuration. A switch diagram is provided in Figure 26.

Table 18. Switch Status

Device State	S1	S2	S3PS	S3PR	S3GS	S3GR	RING2 GNDFET	SLEEVE GNDFET	RING2 DFET	SLEEVE DFET
Default State (No insertion or VDD = 0 V)	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	On	On
Detection running	High-Z	On	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
3-pole	On	High-Z	High-Z	High-Z	On	On	On	On	On	On
3-pole with FM support	On	High-Z	High-Z	High-Z	High-Z	On	On	High-Z	High-Z	High-Z
4-pole OMTP	High-Z	High-Z	High-Z	On	On	High-Z	High-Z	On	High-Z	On
4-pole OMTP with FM support	High-Z	High-Z	High-Z	On	On	High-Z	High-Z	On	High-Z	High-Z
4-pole Standard	High-Z	High-Z	On	High-Z	High-Z	On	On	High-Z	On	High-Z
4-pole Standard with FM support	High-Z	High-Z	On	High-Z	High-Z	On	On	High-Z	High-Z	High-Z

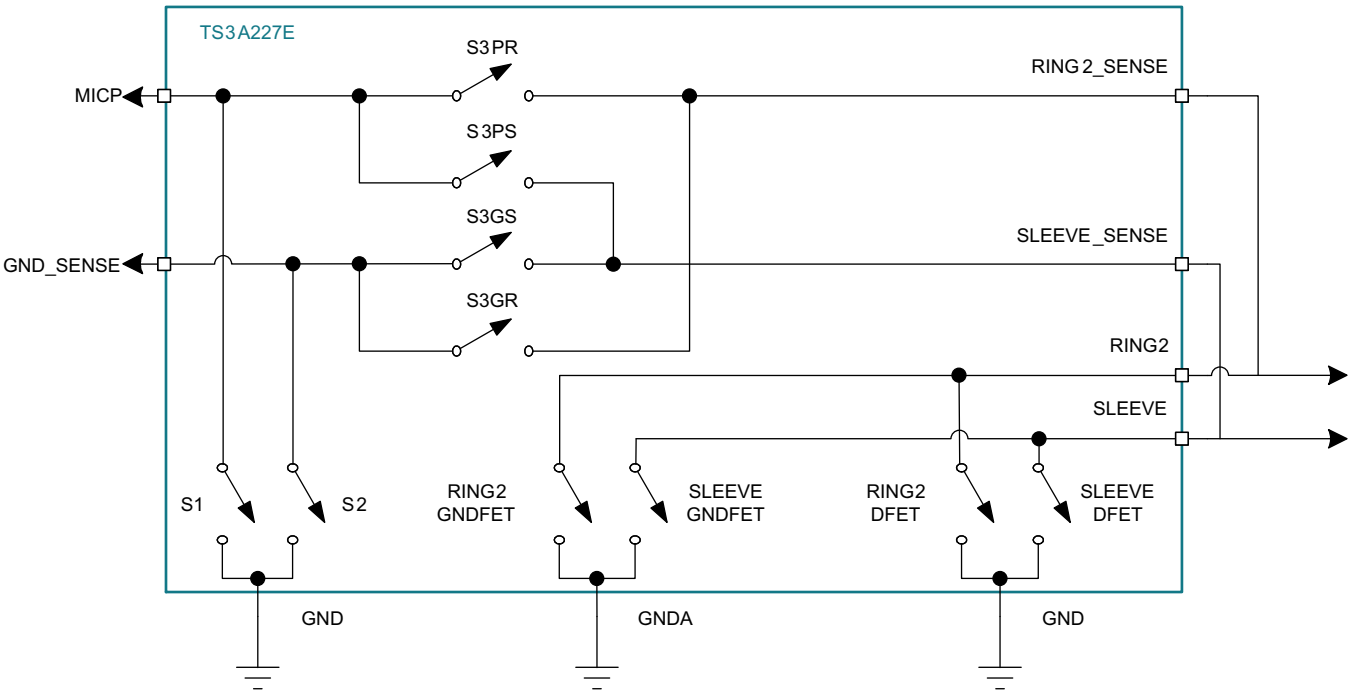

Figure 26. Switch Diagram

10.2.2.3.1 Switch Status Diagrams

Closed switches are red in Figure 27 through Figure 31. The diagrams reflect switch states when manual switch control is not enabled.

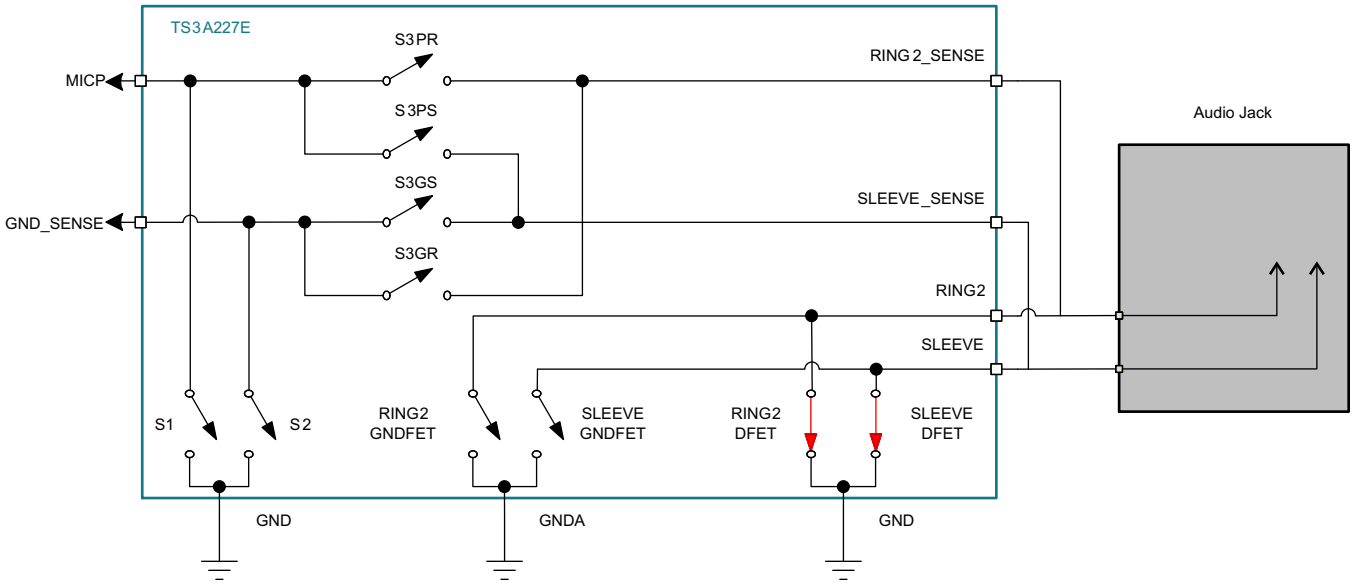

Figure 27. Default Switch State With No Accessory Inserted

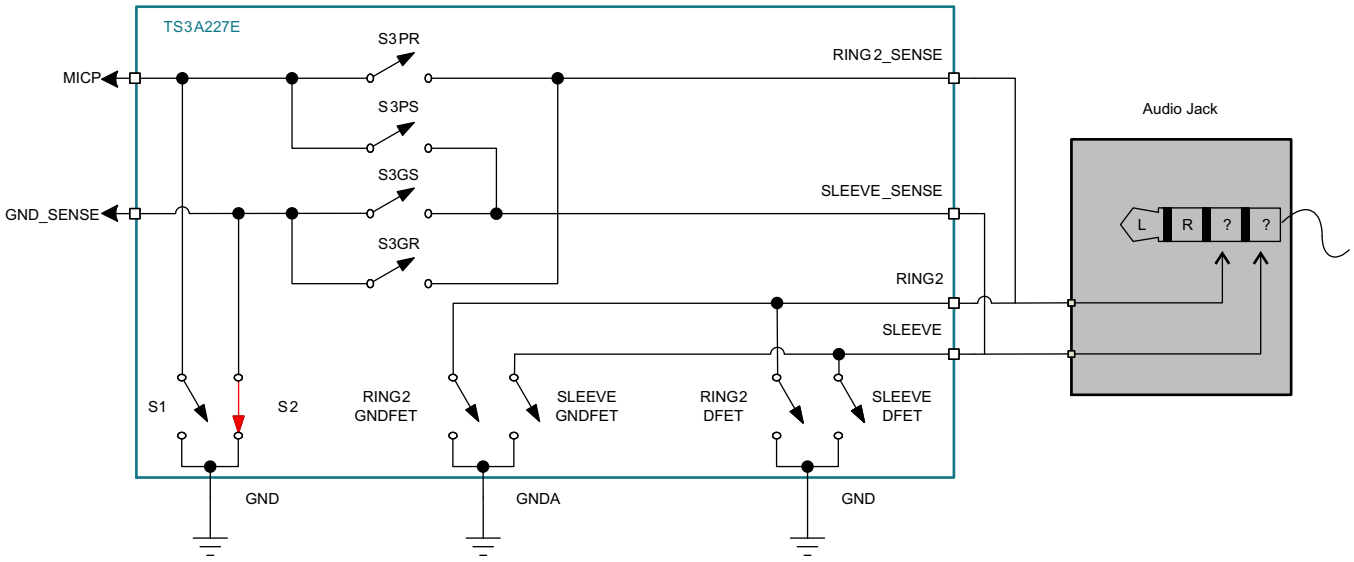

Figure 28. Switch State During Detection

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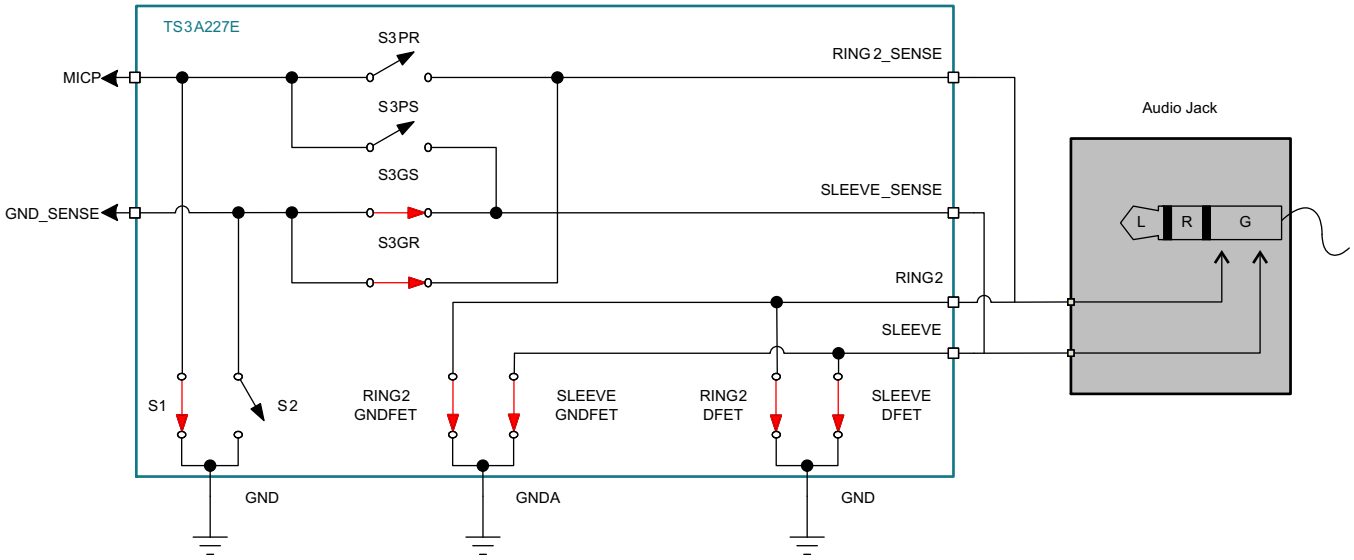

Figure 29. Switch State After Detecting a 3-Pole Headphone

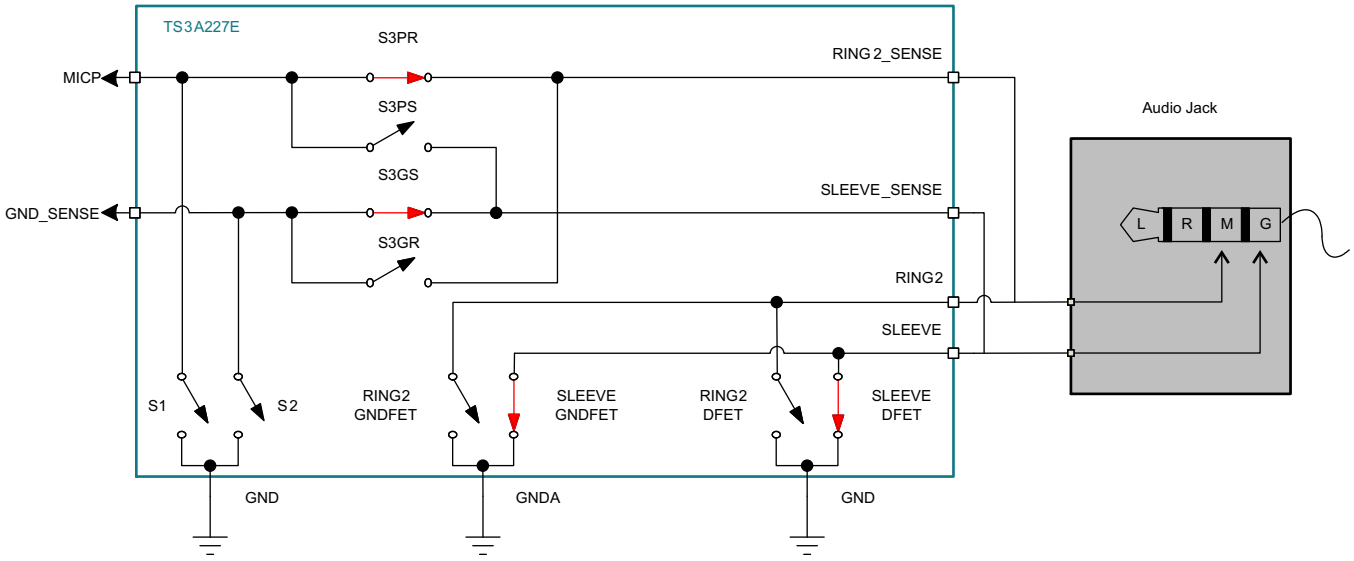

Figure 30. Switch State After Detection a 4-pole OMTP Headset

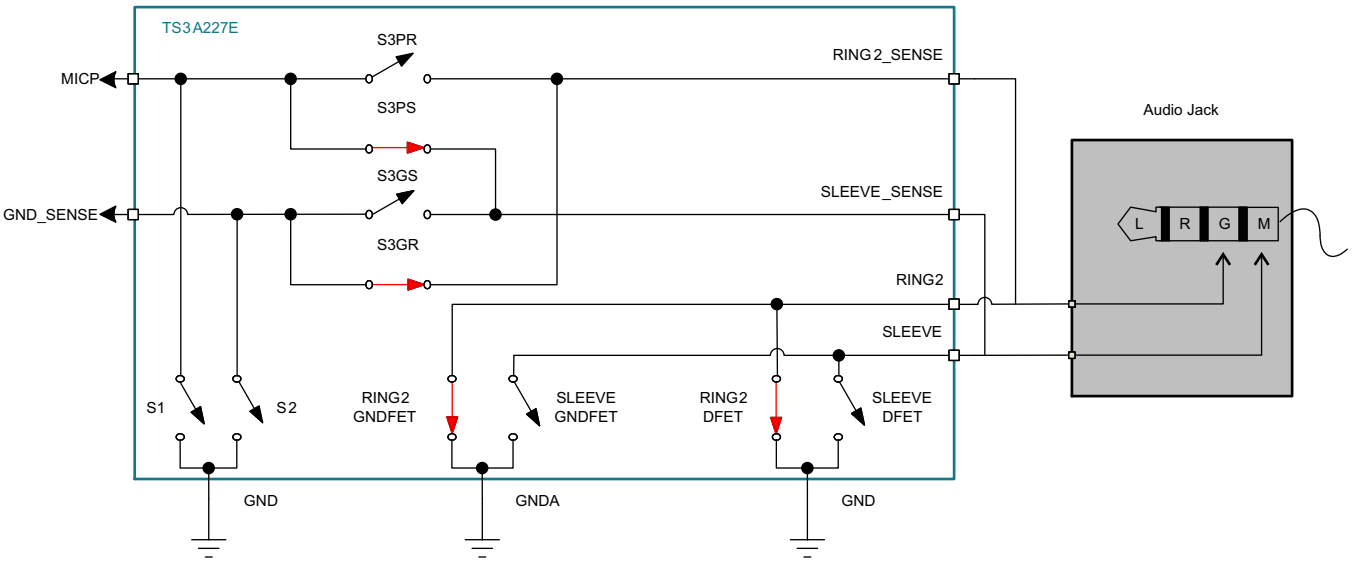

Figure 31. Switch State After Detecting a 4-Pole Standard Headset

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10.2.2.4 Key Press Detection

10.2.2.4.1 Key Press Thresholds

The TS3A227E features the ability to adjust the key press thresholds on the fly. The default key press bins are shown below with the default values of the threshold registers optimized to detect these keys. The values for the bins represent the equivalent resistance of the key being pressed with the microphone in parallel. Any equivalent resistance outside these bins is not guaranteed to be detected correctly.

KEY	TYPICAL RESISTANCE	EQUIVALENT RESISTANCE RANGE
Key 1	50 Ω	0 Ω – 66 Ω
Key 2	135 Ω	126 Ω – 156 Ω
Key 3	240 Ω	228 Ω – 264 Ω
Key 4	470 Ω	360 Ω – 680 Ω

The Threshold 1 register (Address 0Dh) adjusts the detection boundary between Key 1 and Key2. The Threshold 2 register (Address 0Eh) adjusts the detection boundary between Key 2 and Key 3. The Threshold 3 register (Address 0Fh adjusts the detection boundary between Key 3 and Key4.

The thresholds are 7 bit values that can be adjusted for the following formula.

$$\text{Target bin boundary} = \text{KP Threshold}[6:0] \times 6\ \Omega \quad (1)$$

It is important for the proper operation of the KP detection algorithm that the thresholds be ordered correctly: KP Threshold 1< KP Threshold 2 < KP Threshold 3. Placing them out of order will cause incorrect keys to be detected. For information on defining the key press gray zones see the Key Press Gray Zones section.

10.2.2.4.2 System Requirements

The Key Press detection algorithm has the following system requirements to be function properly:

- MICBIAS output voltage equivalent to key press settings 2 register value within 2.5%
- MICBIAS pullup resistance equal to 2.2 kΩ ±1%
- Audio jack contact resistance must be limited to < 100 mΩ. See further information below.

Figure 32 depicts the resistor network without the TS3A227E switches for simplicity.

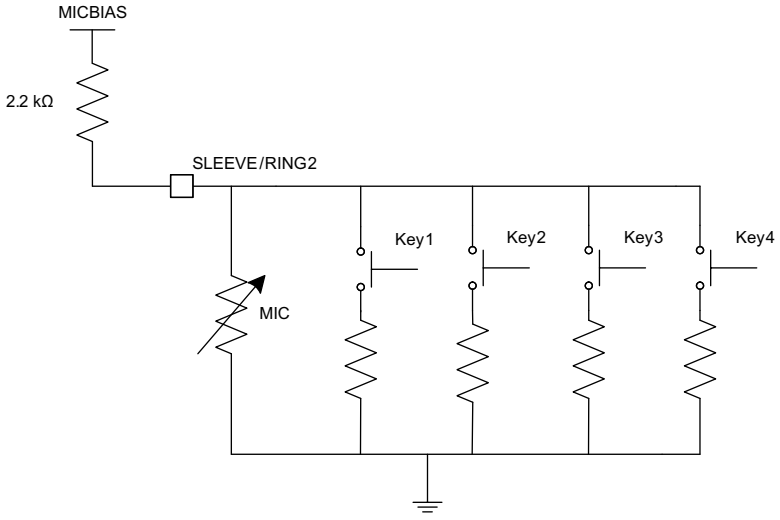


Figure 32. Headset Microphone and Key Network

When the user presses a key it creates a voltage divider network between the MICBIAS output of the codec and the system ground. This will be a measurable voltage on the SLEEVE/RING2 pin that follows Equation 2. Note that this is simplified because it does not include the TS3A227E switches or the contact resistance of the jack itself.

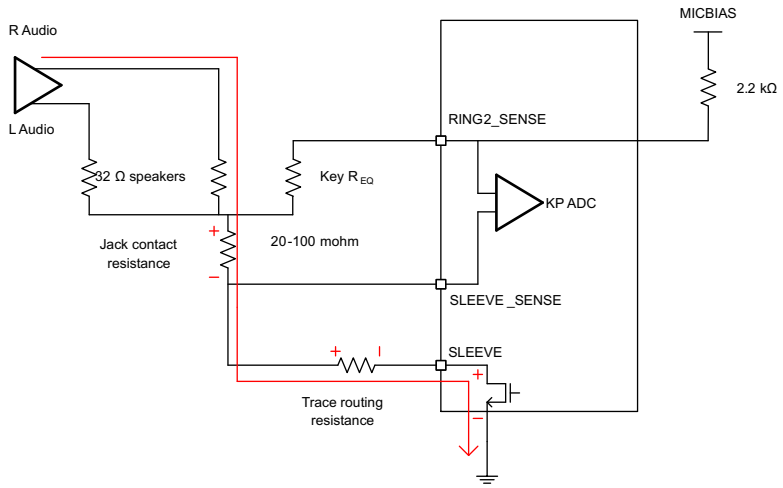
$$V_{SLEEVE/RING2} = \left(V_{MICBIAS} + \Delta V_{MICBIAS}\right) \times \frac{R_{EQ}}{\left(2.2k + \Delta_{2.2k}\right) + R_{EQ}} \quad (2)$$

The R_{EQ} can be calculated with the following:

$$R_{EQ} = \frac{R_{MIC} \times R_{KEY}}{R_{MIC} + R_{KEY}} \quad (3)$$

As a result of the above calculations, an ADC attempting to detect the voltage on SLEEVE/RING2 to determine which key is pressed (whichever is the microphone pin) is reliant on the accuracy on the MICBIAS output and the 2.2 kΩ pull-up resistor. The key press bins are targeted assuming ideal values for these system conditions and then the gray zone between the bins takes into account the system variations. As a result the better the accuracy of the MICBIAS output and pull-up resistor the better the accuracy of the key press detection.

In addition to the above, the contact resistance of the audio jack itself can play a role in how accurate the key press detection is. A general rule is less contact resistance is better. In the figure below a more complete picture of the system and the voltage the TS3A227E will detect is shown.



The red line denotes the current path for the output of the codec to follow when it enters the speakers and eventually sinks into the GNDFETs of the TS3A227E. This audio current adds a voltage offset at the audio jack contact resistance, the trace routing resistance, and the GNDFET itself. Because the TS3A227E has kelvin connections to the jack via the SLEEVE_SENSE RING2_SENSE pins the trace routing resistance and GNDFET induced voltage offsets can be compensated.

However, the jack contact resistance is not visible by the device and cannot be compensated for. To maintain the default bin targets the system must ensure that for a given audio jack contact resistance the max current being output by the codec/amplifier lies below the curve in Figure 34. This ensures a max error introduced of 5 mV into the KP detection algorithm.

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10.2.2.4.3 Key Press Grey Zones

When defining custom bins and thresholds it is important to also correctly define the "gray zone" between the bins to ensure that the system will always correctly identify the key that is being pressed. The gray zone region accounts for the absolute error in key press detection, encompasses the error of the internal ADC along with errors from system tolerances and variation. The equation below can be used to determine the gray zone required between each of the bins. Note that the size of the gray zone will vary depending on the actual value of the key press threshold.

$$\text{Gray Zone} = \pm [(\varepsilon_{(ADC,GAIN)} + \varepsilon_{MICBIAS} + \varepsilon_{RBIAS} + \varepsilon_{(CONT,GAIN)}) \times R_{(KP\ Threshold)}) + (\varepsilon_{(ADC,OFF)} + \varepsilon_{(CONT,OFF)}) + K_{BUFF}) \times 6\ \Omega] \quad (4)$$

TERM	DESCRIPTION	VALUE	UNIT
$\varepsilon_{(ADC,GAIN)}$	Internal ADC gain error	0.015%	
$\varepsilon_{MICBIAS}$	Codec MICBIAS output voltage variation. Default bin values assume an output variation of 2.5%.	0.025%(1)	
ε_{RBIAS}	MICBIAS resistor variation. Default bin values assume a 1% tolerance of the 2.2 kΩ MICBIAS resistor.	0.01%(1)	
$\varepsilon_{CONT.GAIN}$	Gain error introduced by contact resistance of the audio jack.	$\frac{R_{Contact} \times I_{MAX}}{V_{MICBIAS}}$	
$\varepsilon_{KP\ Threshold}$	KP threshold target identified by system. E.g. the KP Threshold between bins 1 and 2 for the default key press bins is 96 Ω.	Defined by system(1)	Ω
$\varepsilon_{ADC,OFF}$	Internal ADC offset and linearity error	1.5	LSB
$\varepsilon_{CONT,OFF}$	Offset error introduced by contact resistance of the audio jack.	$\frac{\frac{R_{Contact} \times I_{MAX}}{V_{MICBIAS}}}{128}$	LSB
K_{BUFF}	Buffer constant added to total system gray zone to ensure bin values are detected correctly. It is recommended to use a minimum of 2 for this when defining key gray zones to ensure system level margins.	2	LSB
$R_{Contact}$	Max contact resistance of audio jack	Defined by system(1)	Ω
I_{MAX}	Maximum combined (Right and Left) audio output current into the jack.	Defined by system(1)	A
$V_{MICBIAS}$	MICBIAS output voltage of the codec	Defined by system(1)	V

(1) These values can vary depending on the system

Example Calculation

The default KP Threshold 1 value for the TS3A227E is 10h or 96 Ω. Using the Gray Zone equation the specified gray zone between keys 1 and 2 can be confirmed assuming the following:

- $V_{MICBIAS}$ = 2.2 V
- $I_{MAX} \times R_{Contact}$ = 5 mV
- $R_{(KP\ Threshold)}$ = 96 Ω
- Default values for all other terms

$$\text{Gray Zone} = \pm \left[\left(0.015 + 0.025 + 0.01 + \frac{5\text{mV}}{2.2} \right) \times 96\ \Omega + \left(1.5 + \frac{\frac{5\text{mV}}{2.2}}{128} + 2 \right) \times 6\Omega \right] \quad (5)$$

This yields a gray zone of ± 27 Ω. The KP Threshold 1 gray zone can be used to identify the upper limit of key 1 and the lower limit of key 2:

Bin 1 upper limit = KP Threshold 1 – Gray Zone 1
Bin 2 lower limit = KP Threshold 1 + Gray Zone 1

This formula yields an upper limit of 69 Ω. Because each LSB is 6 Ω we round down to the even number of 66 Ω. For the beginning of key 2 we set the value at (96 Ω + 27 Ω) or 126 Ω (123 Ω rounded up to the nearest LSB). This method can be used to define the rest of the key bin thresholds.

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10.2.2.4.4 Behavior

The TS3A227E can monitor the microphone line of a 4-pole headset to detect up to 4 key presses/releases and report the key press events back to the host. The key press detection must be activated manually by setting the KP Enable bit of the Device Settings 2 register. To ensure proper operation the MICBIAS voltage must be applied to MICP before enabling key press detection.

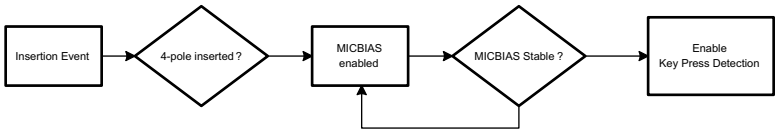

Figure 33. Proper Key Press Enable Sequence

The TS3A227E monitors the S3 switch matrix to determine the location of the microphone. If the Manual Switch Control bit is set to '1', the S3 matrix must be configured in one of the following 2 configurations for the key press detection to operate. Other configurations are not supported with key press detection.

S3PR	S3PS	S3GR	S3GS	MIC LOCATION
On	High-Z	High-Z	On	RING2
High-Z	On	On	High-Z	SLEEVE

If the voltage on the microphone line drops below the key press detection threshold for a duration longer than the key press de-bounce time, the key press is considered to be valid. At this point the detected key has the corresponding Key # Press interrupt bit set to '1' and the interrupt is asserted. The corresponding Key # Release interrupt is cleared at the same time the Key # Press interrupt is set.

Once the key is released for a duration longer than the key release de-bounce time, a Key Release interrupt is generated to inform the host that the key has been released. The corresponding Key # released interrupt bit is set to '1' and the interrupt is asserted.

The Key Press interrupt register will clear the contents and return to the default status of 0h when Key Press detection is disabled via an I2C write or a removal event.

Notes about key press detection:

- The MICBIAS setting adjusts the detection threshold and must be set to the value that is closest to the MICBIAS output of the codec. If the MICBIAS voltage being used is between different MICBIAS settings of the TS3A227E then the closest value that is greater than the MICBIAS voltage should be used.
  - E.G. if the codec output is 2.2 V, the 2.3 V MICBIAS setting in the TS3A227E should be used.
- If any pending interrupt is not read by the host and a key is pressed, the TS3A227E will continue to run key press detection until the Key Press Enable bit is set to '0'

The host will interpret Key Press and Release interrupts using the following pseudo-code:

```
If (Key # Press && Key # Release) {
        Key # was pressed one time and is not being held.
}
else if (Key # Release ) {
        Key # is being pressed, start the key press duration timer
}
 else if (Key # Release) {
        Key # has been released, end the key press duration timer
}
```

The key press duration timer the host starts after reading that a key is pressed can be used as follows:

```
If (Key # Press Duration Timer > XXX ms) {
        The Key # is being held down, handle accordingly.

        E.g. if Key # is the volume up key, the system will increment the volume until the Key #
        Release interrupt is read from the TS3A227E
}
```

10.2.2.4.5 Single Key Press Timing

The diagram below depicts a key press event where the MIC is on the SLEEVE pin. If the MIC is on RING2 the timing diagram will be same.

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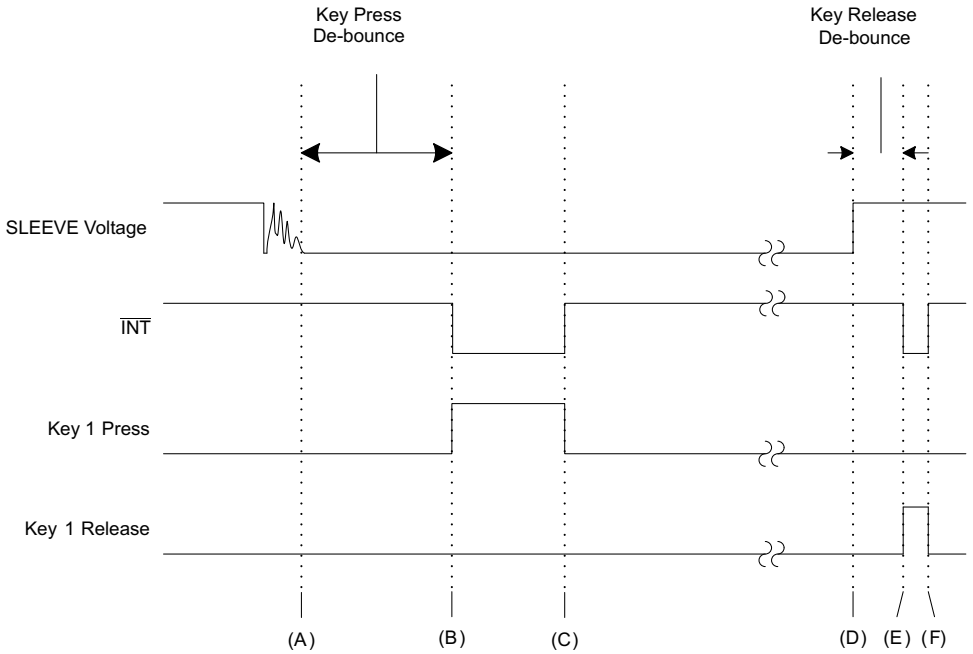

A. At this point the SLEEVE voltage has stopped glitching and the Key Press De-bounce timer will no longer restart.
B. Point B is the end of the key press de-bounce period. $\overline{INT}$ will be asserted with the Key Press bit set.
C. The host read and clears the interrupt register, de-asserting the $\overline{INT}$ pin.
D. Here the key is released and the key release de-bounce period begins.
E. The key release de-bounce period ends and the $\overline{INT}$ pin is asserted again with the Key Release bit set.
F. Here the host reads and clears the interrupt register, de-asserting the $\overline{INT}$ pin.

10.2.2.4.6 Multiple Key Press Timing

The diagram below depicts a multiple key press event in which the host does not immediately read the interrupt register. The MIC is on the SLEEVE pin in this diagram. If the MIC is on RING2 the timing diagram will be the same.

NOTE

If the KP Enable bit is set to '0' during key press detection, key press detection will stop immediately and all the key press/release bits will be cleared.

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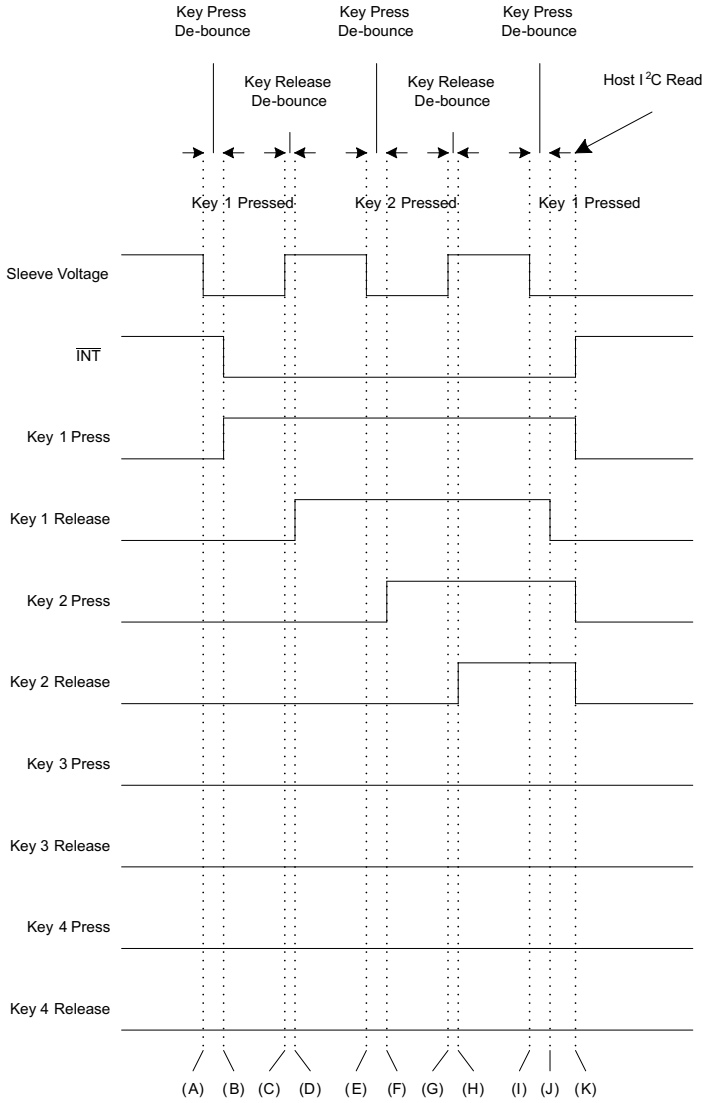

A. The SLEEVE voltage drops below the Key Press Detection threshold and the Key Press De-bounce timer is started

B. The end of the key press de-bounce timer. Key 1 is detected, the Key 1 Press interrupt is set and the interrupt line is asserted. The Key 1 Release interrupt is cleared.

C. The SLEEVE voltage rises to MICBIAS as the key is released. The Key Release de-bounce timer is started.

D. The Key Release de-bounce timer expires. The Key 1 Release bit is set and the interrupt is asserted.

E. The SLEEVE voltage drops below the Key Press Detection threshold and the Key Press De-bounce timer is started

F. The end of the key press de-bounce timer. Key 2 is detected, the Key 2 Press interrupt is set and the interrupt line is asserted. The Key 2 Release interrupt is cleared.

G. The SLEEVE voltage rises to MICBIAS as the key is released. The Key Release de-bounce timer is started.

H. The Key Release de-bounce timer expires. The Key 2 Release bit is set and the interrupt is asserted.

I. The SLEEVE voltage drops below the Key Press Detection threshold and the Key Press De-bounce timer is started

J. The end of the key press de-bounce timer. Key 1 is detected, the Key 1 Press interrupt is set and the interrupt line is asserted. The Key 1 Release interrupt is cleared.

K. The host reads the I2C interrupt register and sees the following interrupts:
   - Key 1 Press
   - Key 2 Press
   - Key 2 Release

   Using the pseudo-code in the key press detection section this is interpreted as:
   - Key 2 was pressed one time and is not being held
   - Key 1 is currently pressed, start the key press duration timer

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10.2.2.4.7 Raw Data Key Press Detection

In addition to threshold adjustment the TS3A227E features the ability to utilize the internal ADC raw output with the Raw Data En bit of the Device Setting 2 register.

Notes on using the Raw ADC Output:

- Key Press/Release interrupts that have not been serviced will not be cleared upon setting the Raw Data En bit to '1'.
- By Setting the Raw Data En bit to '1' the Key Press Threshold registers will be ignored. Instead of reporting key 1 through 4 press and releases the TS3A227E will only use Key 1 Press to indicate that a key is pressed and the Key 1 Release interrupt to report that the key was released.
- The ADC Output register will only be cleared after the Raw Data En bit is cleared. The Raw Data En bit is cleared if the Key Press Enable bit is set to '0'. Consequently the ADC Output register clears if the Raw Data En bit is set to '0', the Key Press Enable bit is set to '0', or a removal event occurs. This means the ADC Output register will not clear after it is read.
- A manual software trigger can be initiated after a key was pressed to run the ADC detection again. This will not set the Key 1 Press interrupt.
- The ADC Output is updated after a Key is detected or if the manual ADC trigger bit is set to '1'. If an ADC conversion has completed the ADC Conversion interrupt bit will be set to '1' regardless if there was a software initiated trigger or if a new key press was detected.
- If the ADC has completed a conversion the output is always non 0 meaning the lowest possible detection threshold of the ADC is 01h. If the ADC Output register is 00h a conversion has not been completed or the ADC Output was cleared.

The previous section on gray zones should be applied to any bins create for the raw ADC mode.

10.2.3 Application Curves

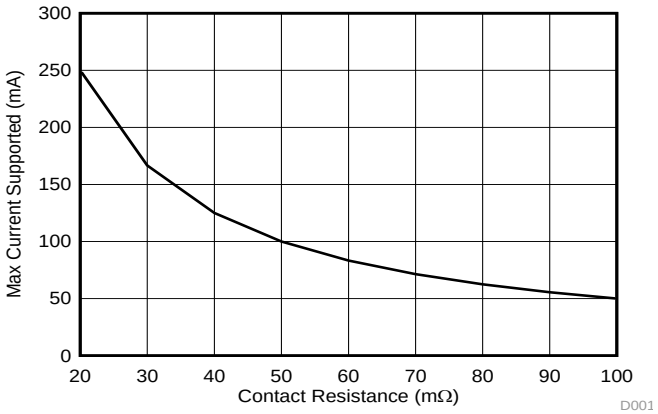

Figure 34. Max Current vs Contact Resistance

11 Power Supply Recommendations

The TS3A227E is designed to operate from an input voltage supply range between 2.5 V and 4.5 V. This input supply is recommended to be decoupled to ground via two de-coupling capacitors of 0.1µF and 1µF placed as close as possible to the TS3A227E. To ensure a POR trip during a power-down and power-on event the power supply should follow the minimum and maximum V_{DD} rise and fall times specified in the electrical specifications section.

The TS3A227E features the ability to power the digital IO pins at a different rail than the supply. This allows systems to run the TS3A227E at 3.3 V and still use a 1.8 V eliminating the need for a translator. Have the 1.8 V rail while the device is powered from a higher voltage will increase the current consumption of the device due to CMOS shoot through current. This increased supply current is documented in the electrical specifications table.

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12 Layout

12.1 Layout Guidelines

- The VDD pin must have de-coupling capacitors places as closely to the device as possible. Typically recommended capacitors are a 0.1 µF and 1 µF capacitor.
- If FM support is not needed connect GNDA to system GND along with the GND connections with the shortest connections possible.
- RING2 and SLEEVE should be routed on the same layer as the audio jack for best performance with less than 50 mΩ to the audio jack pins. These two pins should have priority in layout over other pins. It is recommended to not use vias on these traces and pair the device with an audio jack that facilitates this type of layout.
- The RING2_SENSE and SLEEVE_SENSE pins are kelvin connections to the audio jack and should be shorted to RING2 and SLEEVE as close to the audio jack as possible. If there are 0 Ω resistors between the SLEEVE/RING2 pins and the jack, connect the SENSE lines to the jack sleeve and ring2 contacts. If a microphone is connected one of the SENSE lines will carry the microphone signal and the MICBIAS supply. It is recommended that these traces not have more than 1 Ω impedance to the jack.
- Route the I^2C and digital signals away from the audio signals to prevent coupling onto the audio lines.

12.2 Layout Example (QFN)

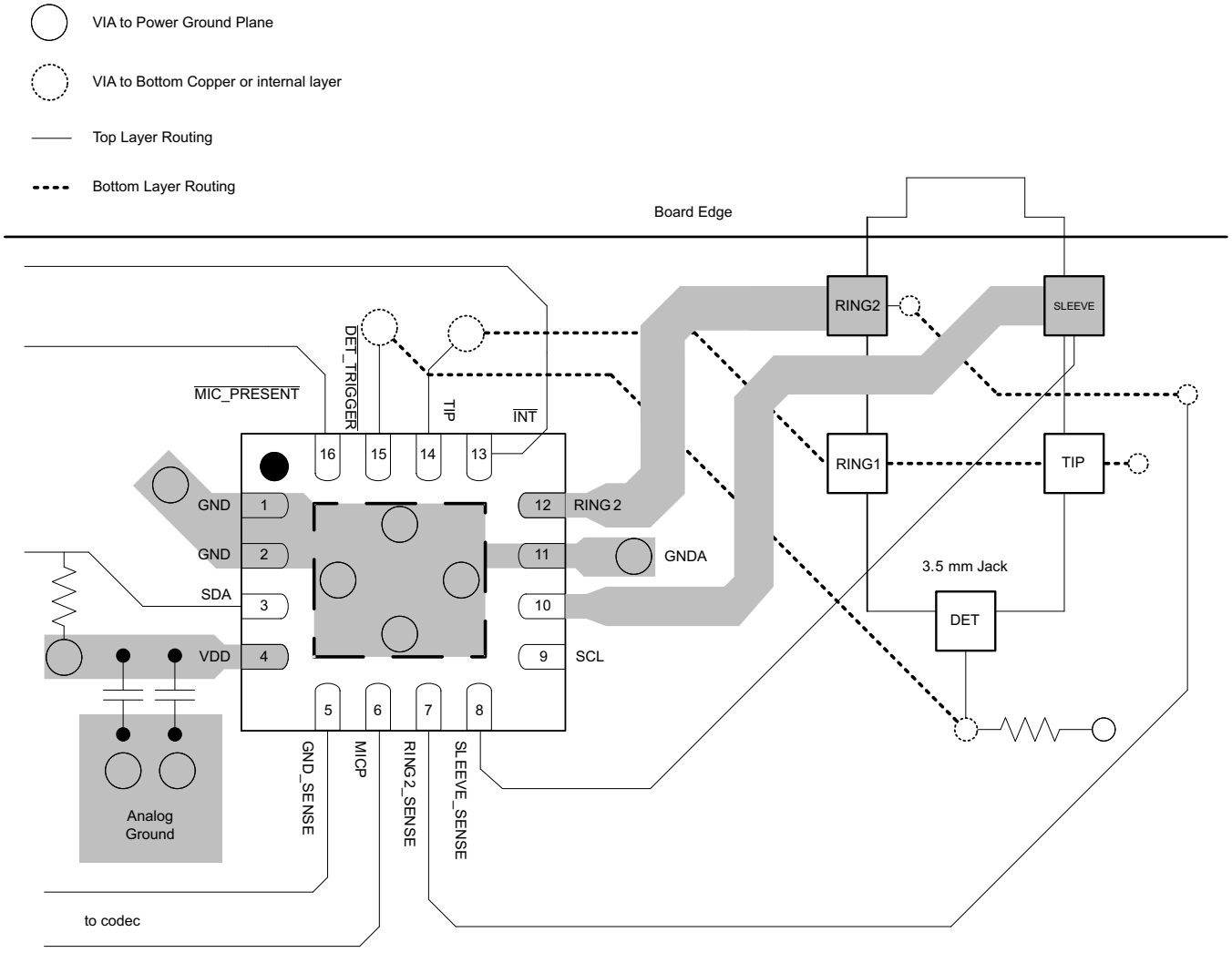

Figure 35. QFN Layout Example

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12.3 Layout Example (DSBGA)

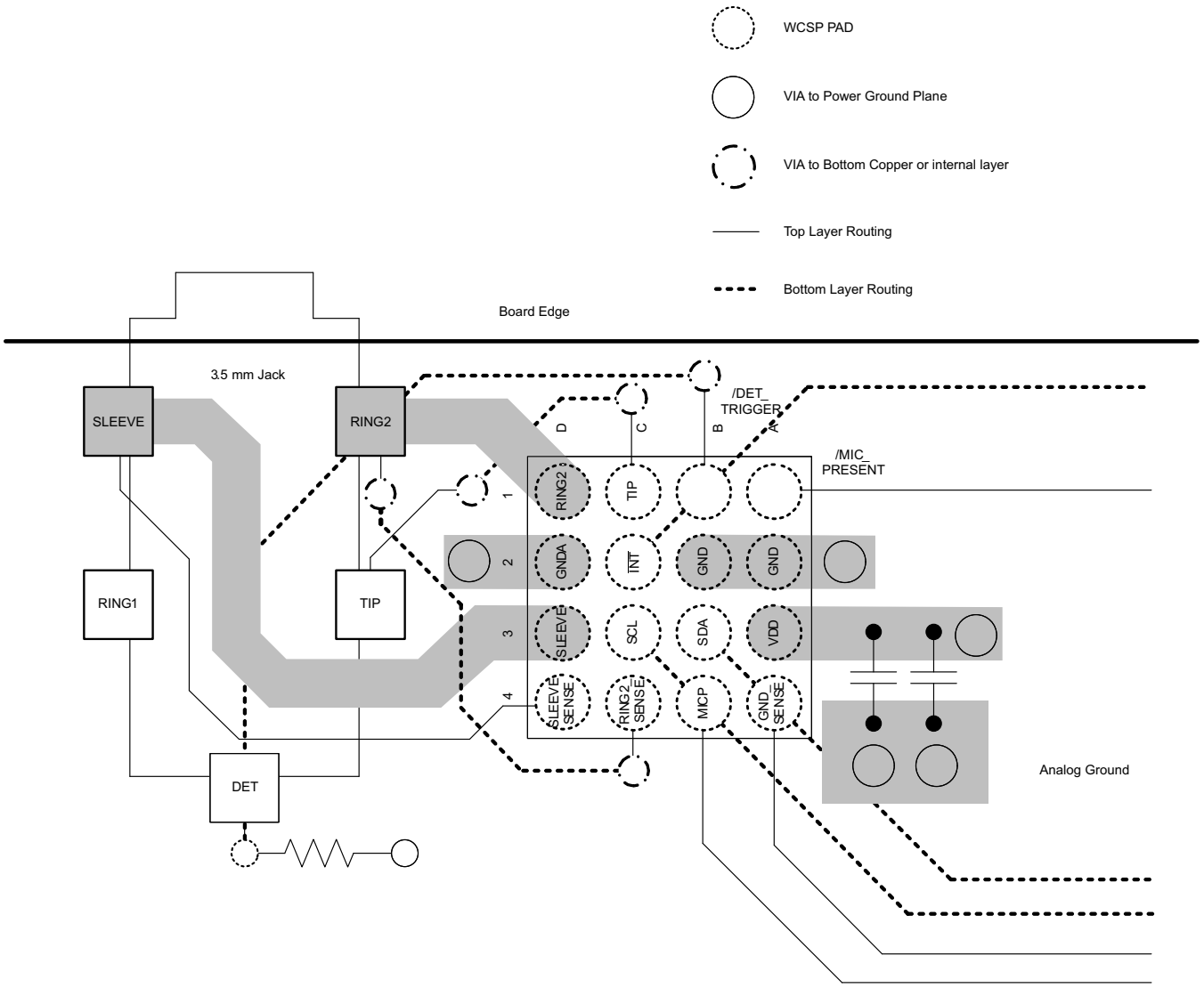

Figure 36. DSBGA Layout Example

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A227ERVAR	ACTIVE	VQFN	RVA	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	227	Samples
TS3A227EYFFR	ACTIVE	DSBGA	YFF	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	227E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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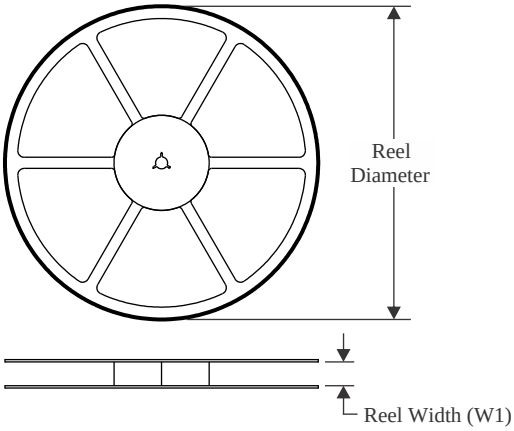
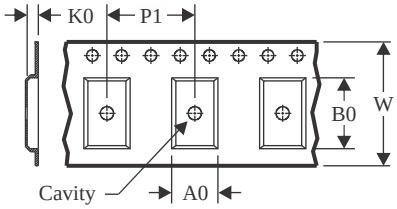
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

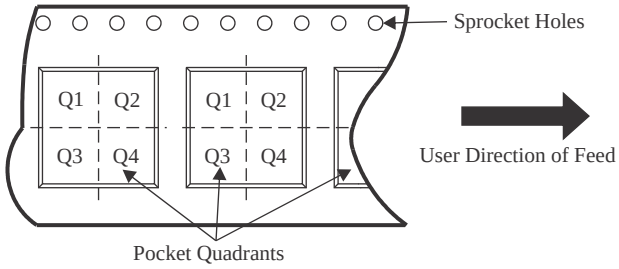


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

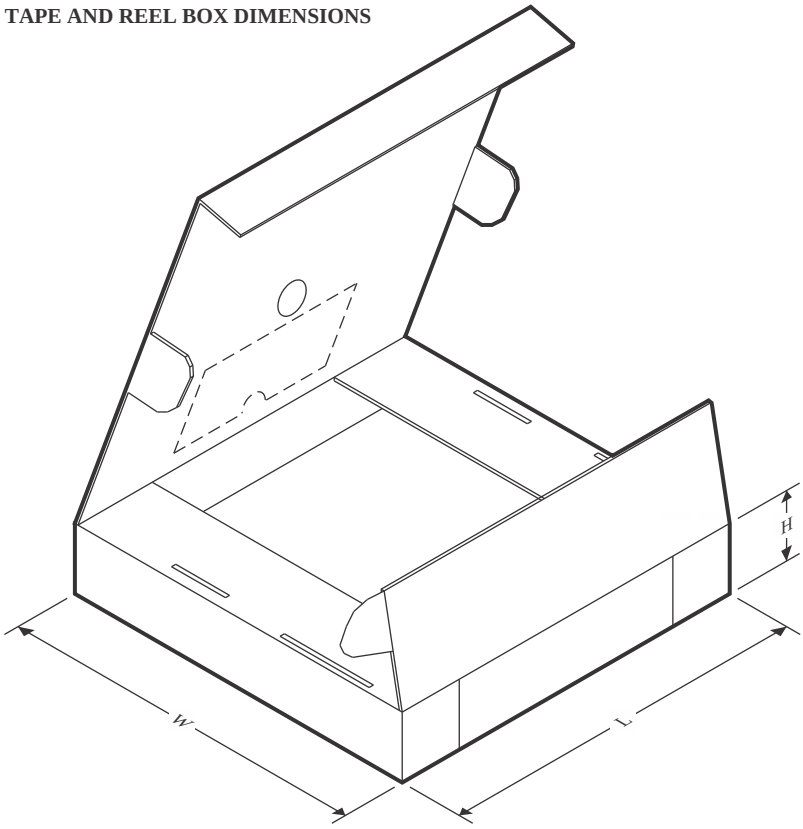
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A227ERVAR	VQFN	RVA	16	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TS3A227EYFFR	DSBGA	YFF	16	3000	180.0	8.4	1.94	1.94	0.69	4.0	8.0	Q1

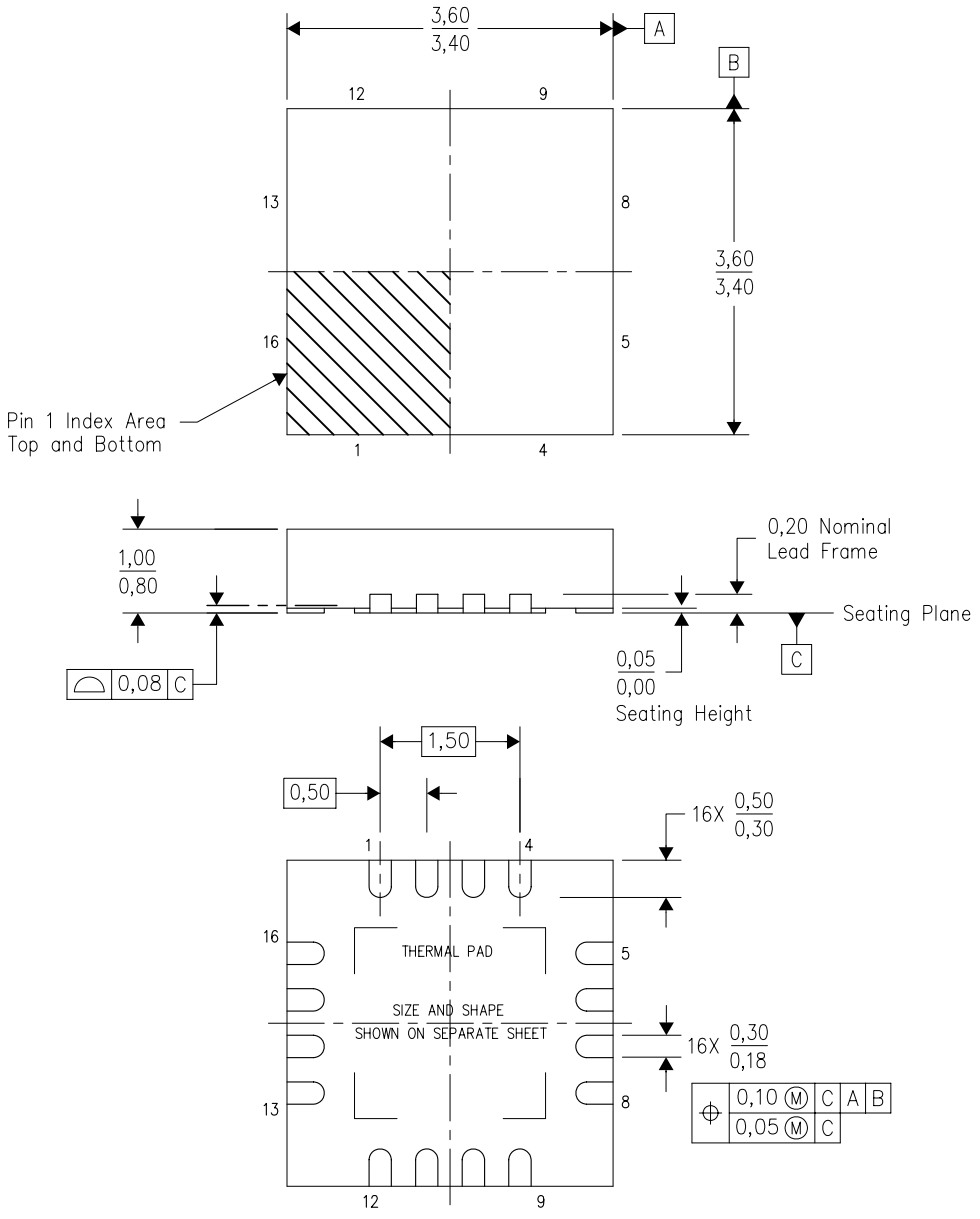
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A227ERVAR	VQFN	RVA	16	3000	346.0	346.0	33.0
TS3A227EYFFR	DSBGA	YFF	16	3000	182.0	182.0	20.0

RVA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



4209676/C 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

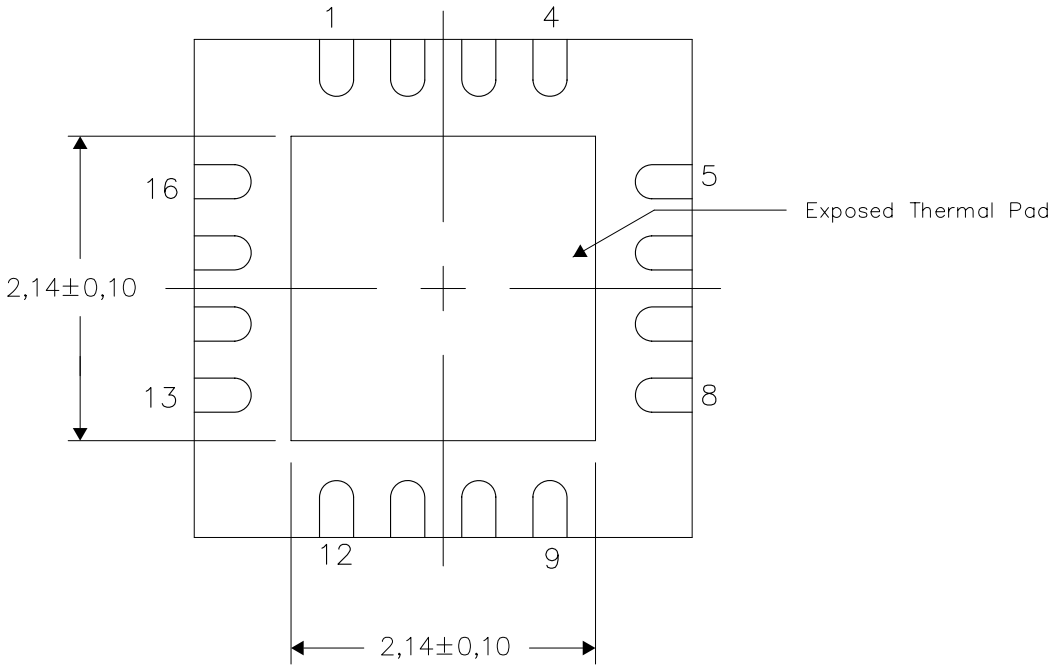
RVA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

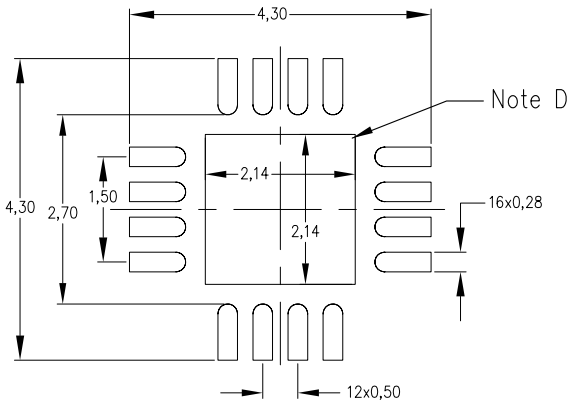
Exposed Thermal Pad Dimensions

4209715/B 05/11

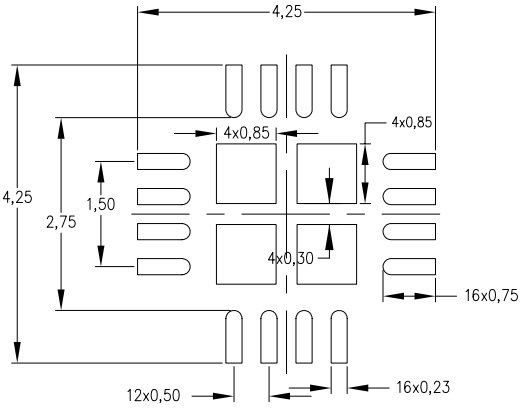
NOTE: All linear dimensions are in millimeters

RVA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout

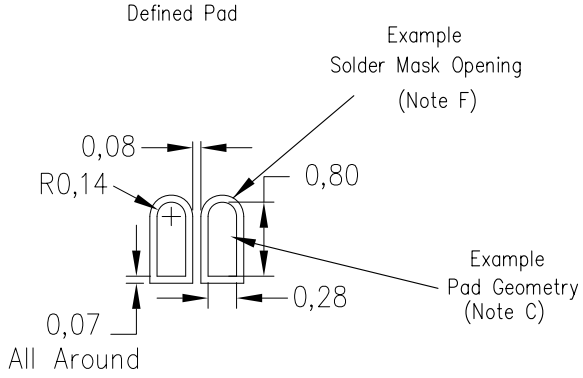


Example Stencil Design
0.125mm Stencil Thickness
(Note E)

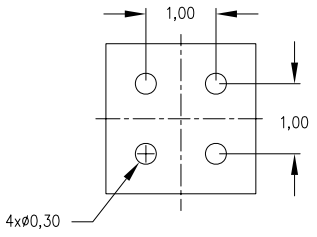


63% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad



Example Via Layout Design
may vary depending on constraints
(Note D, F)



4211274/B 05/11

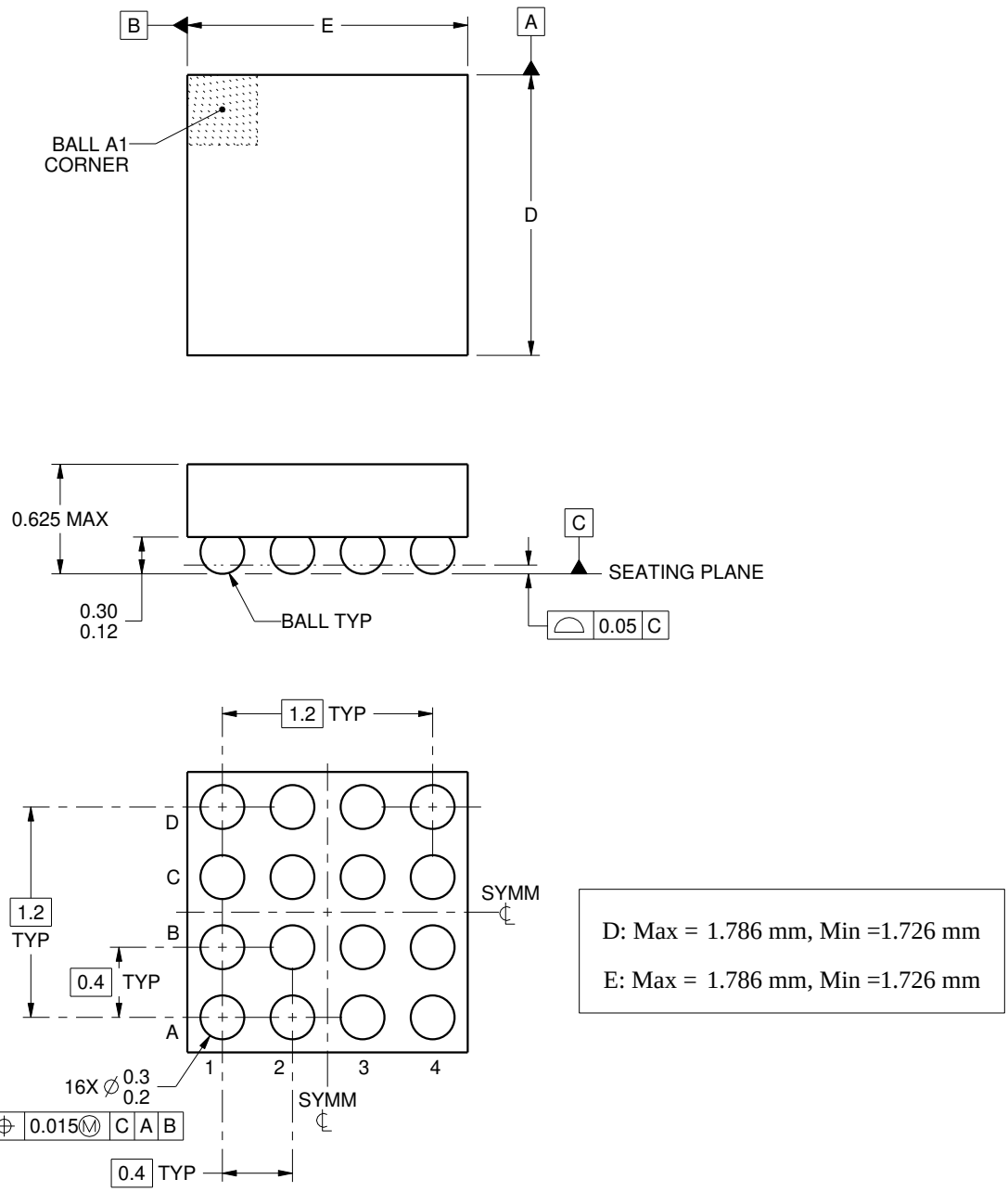
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

PACKAGE OUTLINE

YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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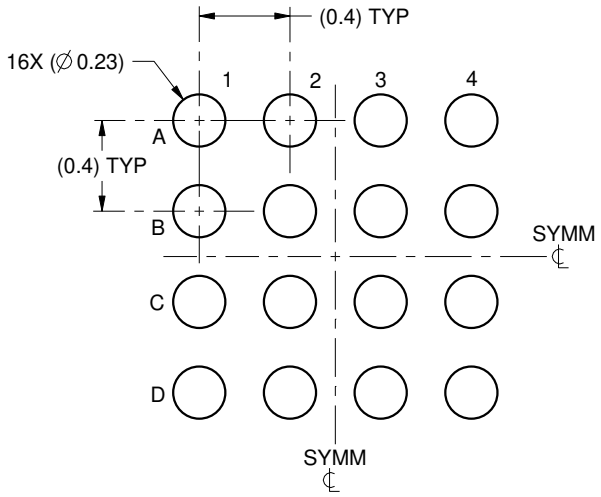
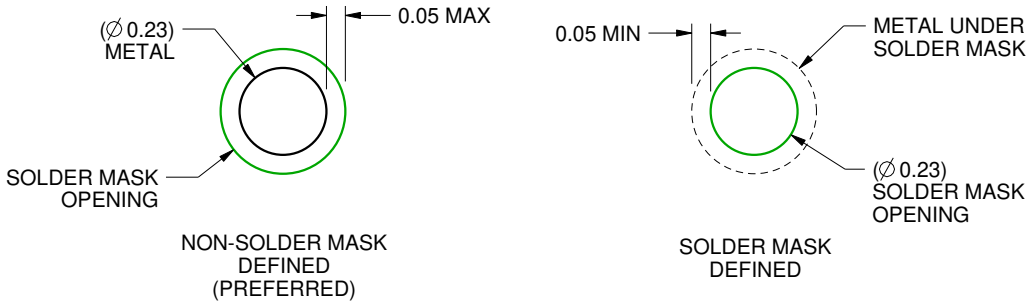
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

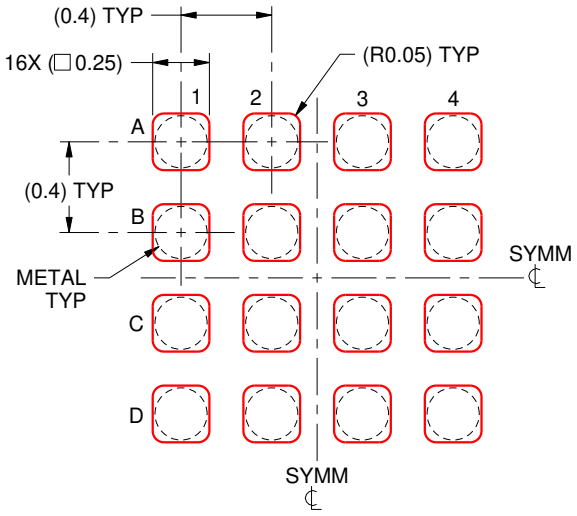
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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