

## Evaluating the AD7366/AD7367

### FEATURES

Full-featured evaluation board for the [AD7366/AD7367](#)  
PC control in conjunction with the system demonstration  
platform ([EVAL-SDP-CB1Z](#))  
PC software for control and data analysis (time and  
frequency domain)  
Standalone capability

### ONLINE RESOURCES

Evaluation kit contents  
[AD7366/AD7367](#) evaluation board  
Evaluation software CD for the [AD7366/AD7367](#)  
[EVAL-AD7366/AD7367SDZ](#)  
9 V mains power supply adapter  
Document needed for reference  
[AD7366/AD7367](#) data sheet  
Required software  
[EVAL-AD7366SDZ/AD67SDZ](#) evaluation software  
Design and integration files  
[Schematics, layout files, and bill of materials](#)

### EQUIPMENT NEEDED

System demonstration platform ([EVAL-SDP-CB1Z](#))  
Precision analog signal source  
SMB cables  
USB cables  
PC running Windows™ with USB 2.0 port

### GENERAL DESCRIPTION

The EVAL-AD7366SDZ/EVAL-AD7367SDZ is a full-featured evaluation board, designed to allow the user to easily evaluate all features of the [AD7366/AD7367](#). The evaluation board can be control-led via the system demonstration platform (SDP) connector (J8). The [EVAL-SDP-CB1Z](#) board allows the evaluation board to be controlled via the USB port of a PC using the [AD7366/AD7367](#) evaluation software.

The EVAL-AD7366SDZ/EVAL-AD7367SDZ generates all required power supplies on board and supplies power to the [EVAL-SDP-CB1Z](#) controller board.

On-board components include

- [AD8021](#): Low noise, high speed amplifier for 16-bit systems
- [ADP1613](#): Step-up PWM dc-to-dc switching converter
- [ADP3303-5](#): High accuracy anyCAP™ 200 mA low dropout linear regulator
- [ADP2301](#): 1.2 A 20 V, 1.4 MHz nonsynchronous step-down switching regulator
- [ADP1720](#): 50 mA, high voltage, micropower linear regulator
- [ADM1185](#): Quad voltage monitor and sequencer
- [ADG3308](#): Low voltage, 1.15 V to 5.5 V, 8-channel bidirectional logic level translator
- [AD780](#): 5 V/3.0 V ultrahigh precision band gap voltage reference

Various link options are described in the Evaluation Board Hardware section.

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**REVISION HISTORY**

**9/12—Rev. 0 to Rev. A**

Changed EVAL-AD7366CBZ and EVAL-AD7367CBZ to EVAL-AD7366SDZ and EVAL-AD7367SDZ Throughout.....	1
Changes to Title .....	1
Reorganized Layout.....	Universal
Changes to Figure 1 .....	3
Added Quick Start Guide Section .....	4
Replaced Evaluation Board Software Section .....	10
Removed Evaluation Board Schematics and Artwork Section .....	12
Added Figure 15 to Figure 19; Renumbered Sequentially .....	13

**6/07—Revision 0: Initial Version**

# FUNCTIONAL BLOCK DIAGRAM

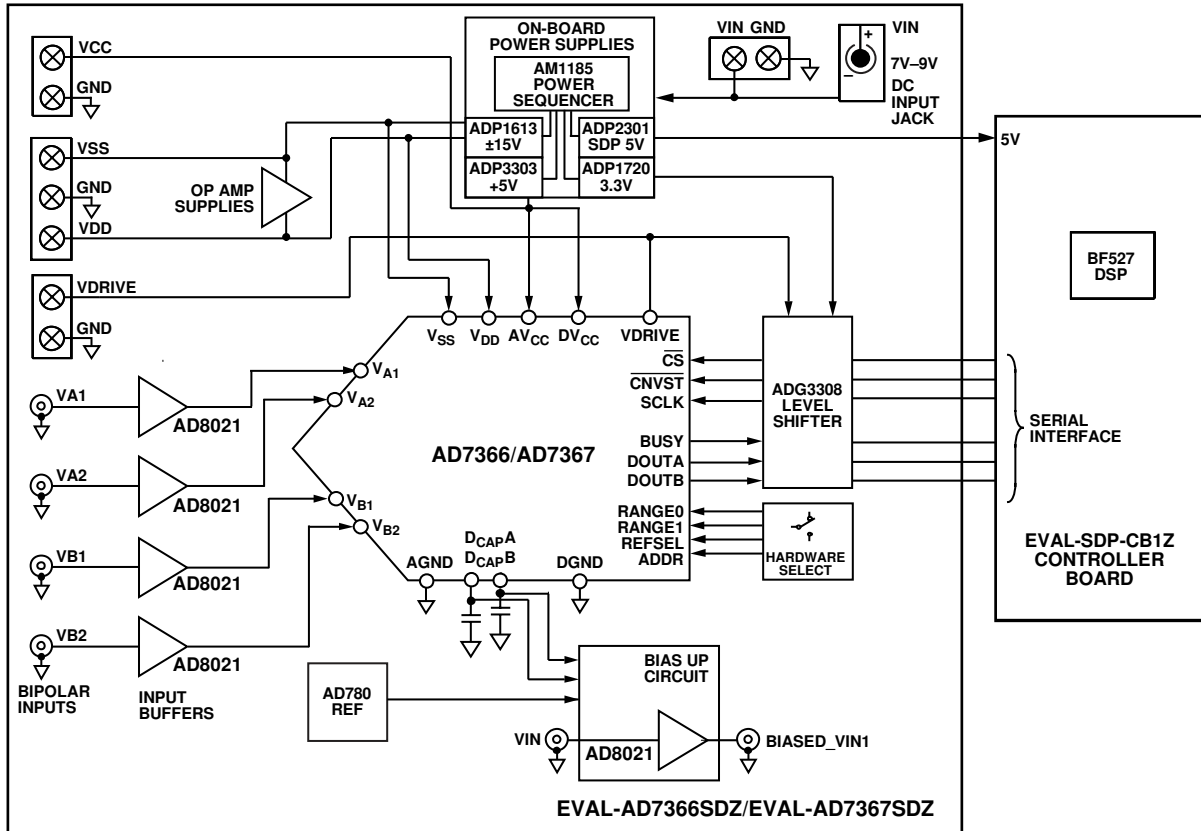


Figure 1.

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## QUICK START GUIDE

### RECOMMENDED QUICK START STEPS

To install the software, complete the following steps:

1. Install the [AD7366/AD7367](#) software from the enclosed CD. Ensure that the [EVAL-SDP-CB1Z](#) board is disconnected from the USB port of the PC while installing the software. The PC must be restarted after the installation.
2. Connect the [EVAL-SDP-CB1Z](#) board to the EVAL-AD7366SDZ/EVAL-AD7367SDZ board as shown in Figure 2.
3. Screw the two boards together with the enclosed nylon screw-nut set to ensure the boards connect firmly together.
4. Connect the 9 V power supply adapter included in the kit to connector J702 on the EVAL-AD7366SDZ/ EVAL-AD7367SDZ board.
5. Connect the [EVAL-SDP-CB1Z](#) board to the PC via the USB cable. For Windows® XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the [EVAL-SDP-CB1Z](#) board if prompted by the operating system.
6. Launch the EVAL-AD7366SDZ/EVAL-AD7367SDZ software from the Analog Devices subfolder in the **Programs** menu.

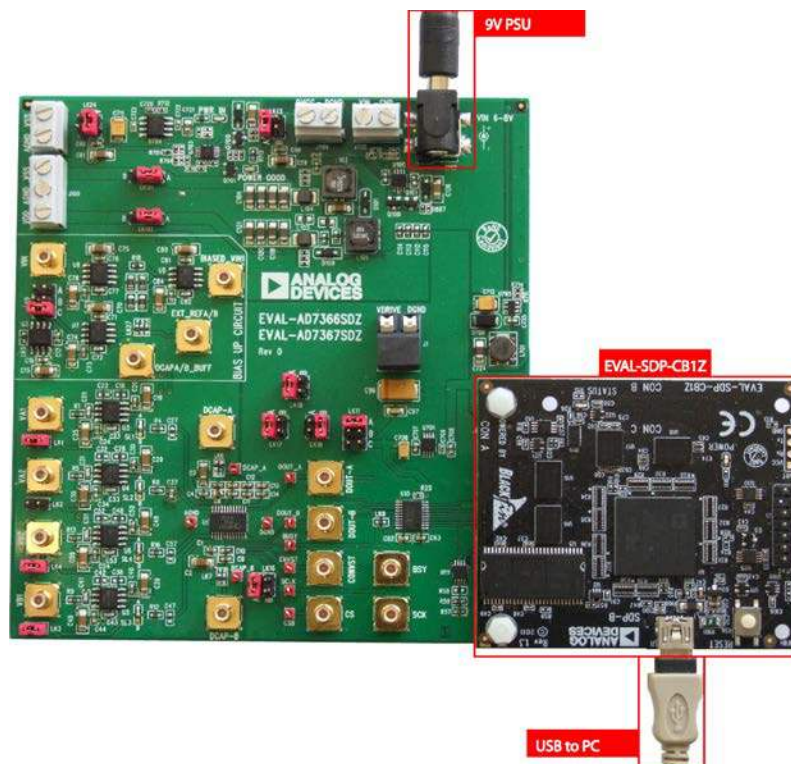


Figure 2. Hardware Configuration—Setting Up the Evaluation Board

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## EVALUATION BOARD HARDWARE

### AD7366/AD7367 DEVICE DESCRIPTION

The AD7366/AD7367 are dual 12-bit/14-bit, high speed, low power, successive approximation analog-to-digital converters (ADCs) that feature throughput rates up to 1 MSPS. The device contains two ADCs, each preceded by a 2-channel multiplexer, and a low noise, wide bandwidth track-and-hold amplifier.

The AD7366/AD7367 are fabricated on the Analog Devices, Inc., industrial CMOS process (*i*CMOS2), which is a technology platform combining the advantages of low and high voltage CMOS. The *i*CMOS<sup>®</sup> process allows the AD7366/AD7367 to accept high voltage bipolar signals in addition to reducing power consumption and package size.

The AD7366/AD7367 can accept true bipolar analog input signals in the  $\pm 10$  V range,  $\pm 5$  V range, and 0 V to 10 V range.

The AD7366/AD7367 have an on-chip 2.5 V reference that can be disabled to allow the use of an external reference. If a 3 V reference is applied to the D<sub>CAP</sub>A and D<sub>CAP</sub>B pins, the AD7366/AD7367 can accept a true bipolar  $\pm 12$  V analog input. Minimum  $\pm 12$  V V<sub>DD</sub> and V<sub>SS</sub> supplies are required for the  $\pm 12$  V input range.

Complete specifications for the AD7366/AD7367 are provided in the AD7366/AD7367 data sheet, available from Analog Devices, which should be consulted in conjunction with this user guide when using the AD7366/AD7367 evaluation board.

## HARDWARE LINK OPTIONS

There are 23 link options, which must be set for the required operating setup before using the evaluation board. The functions of these options are outlined in Table 1. Table 1 shows the position in which all the links are set when the evaluation board is packaged. Jumper and solder link (LKx) options must be set correctly to select the appropriate operating setup before using the evaluation board. The default link positions are shown in Table 2 while the functions of these options are outlined in Table 1.

**Table 1. Link Options**

Link No.	Function															
LK1	Shorts input VA1 to ground when inserted.															
LK2	Shorts input VA2 to ground when inserted.															
LK3	Shorts input VB1 to ground when inserted.															
LK4	Shorts input VB2 to ground when inserted.															
SL1	VA1 Signal Selection. Position A: Input signal is buffered by amplifier U3. Position B: Input signal is passed directly to <a href="#">AD7366/AD7367</a> (via Resistor R4).															
SL2	VA1 Signal Selection. Position A: Input signal is buffered by amplifier U4. Position B: Input signal is passed directly to <a href="#">AD7366/AD7367</a> (via Resistor R8).															
SL3	VA1 Signal Selection. Position A: Input signal is buffered by amplifier U5. Position B: Input signal is passed directly to <a href="#">AD7366/AD7367</a> (via Resistor R12).															
SL4	VA1 Signal Selection. Position A: Input signal is buffered by amplifier U6. Position B: Input signal is passed directly to <a href="#">AD7366/AD7367</a> (via Resistor R16).															
LK5	<a href="#">AD780</a> Reference Output Voltage Selection. Placed: VOUT = 3 V. Unplaced: VOUT = 2.5 V.															
LK6	DCAP_A Source Selection. Position A: DCAP_A connected to LK9. Position B: DCAP_A pin connected to external source via SMB socket DCAP-A.															
LK7	DCAP_B Source Selection. Position A: DCAP_B connected to LK9. Position B: DCAP_B pin connected to external source via SMB socket DCAP-B.															
LK8	BUSY Pin Connection to Level Shifter.															
LK9	BIAS-UP Circuit Bias Voltage Selection. Bias voltage supplied to Pin 3 of U7 is sourced as follows: Position A: DCAP_A (see LK6). Position B: DCAP_B (see LK7). Position C: U2 <a href="#">AD780</a> precision reference. Ensure LK6 or LK7 is in the appropriate position.															
LK11	VDRIVE Voltage Selection. Sets the voltage at the VDRIVE pin of the <a href="#">AD7366/AD7367</a> . Position A: VDRIVE connected to on-board 5 V. Position B: Externally supplied voltage supplied via J1. Position C: VDRIVE connected to on-board 3.3 V.															
LK16	REFSEL Selection. Controls which internal or external reference voltage is used. Position A: Internal reference voltage is selected. Position B: External reference voltage is selected. This voltage may be supplies to DCAPA and/or DCAPB pins.															
LK17	ADDR Selection. This selects which pair of inputs are to be sampled. Position A: VA2 and VB2 are sampled. Position B: VA1 nd VB1 are sampled.															
LK18 LK19	Range Selection. Set up the analog input voltage range for all inputs.															
	<table border="1"> <thead> <tr> <th>LK18 (RANGE0)</th> <th>LK19 (RANGE1)</th> <th>Range Selected</th> </tr> </thead> <tbody> <tr> <td>A (1)</td> <td>A (1)</td> <td>Do not use.</td> </tr> <tr> <td>A (1)</td> <td>B (0)</td> <td>±5 V</td> </tr> <tr> <td>B (0)</td> <td>A (1)</td> <td>0 V to 10 V</td> </tr> <tr> <td>B (0)</td> <td>B (0)</td> <td>±10 V</td> </tr> </tbody> </table>	LK18 (RANGE0)	LK19 (RANGE1)	Range Selected	A (1)	A (1)	Do not use.	A (1)	B (0)	±5 V	B (0)	A (1)	0 V to 10 V	B (0)	B (0)	±10 V
LK18 (RANGE0)	LK19 (RANGE1)	Range Selected														
A (1)	A (1)	Do not use.														
A (1)	B (0)	±5 V														
B (0)	A (1)	0 V to 10 V														
B (0)	B (0)	±10 V														

Link No.	Function
LK23	DVCC Source Selection. Position A: DVCC to <a href="#">AD7366/AD7367</a> supplied from on-board 5 V supply. Position B: DVCC to <a href="#">AD7366/AD7367</a> supplied from external supply via J704.
LK24	AVCC Source Selection. Position A: AVCC to <a href="#">AD7366/AD7367</a> supplied from on-board 5 V supply. Position B: AVCC to <a href="#">AD7366/AD7367</a> supplied from external supply via J703.
LK27	BIAS-UP Voltage Selection Source: Select voltage source supplied to U9 Pin 3. (Note that this will be ½ of the voltage selected by this link setting.) Position A: Buffered voltage as selected by LK9. (See LK 9) Position B: 0 V. Position C: External voltage via SMB connector EXT_REF A/B.
LK101 <sup>1</sup>	VSS Selection. Position A: VSS supplied from on-board supply. Position B: VSS supplied from external source via J100 terminal 1.
LK102 <sup>1</sup>	VDD Selection. Position A: VDD supplied from on-board supply. Position B: VDD supplied from external source via J100 terminal 3.

<sup>1</sup> Both LK101 and LK102 should always be in corresponding positions.

**Table 2. Link Options—Setup Conditions**

Link No.	Position	Function
LK1	INSERTED	Input VA1 shorted to ground.
LK2	INSERTED	Input VA2 shorted to ground.
LK3	INSERTED	Input VB1 shorted to ground.
LK4	INSERTED	Input VB2 shorted to ground.
SL1	A	Input signal is buffered by amplifier.
SL2	A	Input signal is buffered by amplifier.
SL3	A	Input signal is buffered by amplifier.
SL4	A	Input signal is buffered by amplifier.
LK5	INSERTED	VOUT = 3 V.
LK6	A	DCAP_A connected to LK9.
LK7	A	DCAP_A connected to LK9.
LK8	INSERTED	
LK9	C	Reference voltage sourced from <a href="#">AD780</a> .
LK11	A	VDRIVE pin 5 V.
LK16	A	Internal reference voltage is selected.
LK17	B	VA1 and VB1 are sampled.
LK18	A	±5 V analog input range selected.
LK19	B	
LK23	A	DVCC supplied from on-board 5 V.
LK24	A	AVCC supplied from on-board 5 V.
LK27	A	Buffered voltage as selected by LK9.
LK101	A	VSS supplied from on-board supply.
LK102	A	VDD supplied from on-board supply.

## POWER SUPPLIES

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as required by the operating mode.

When using the EVAL-AD7366SDZ/EVAL-AD7367SDZ in conjunction with the EVAL-SDP-CB1Z board, connect the ac transformer to connector J702. VCC, VDD, VSS, and VDRIVE are generated on board. Alternatively, a bench power supply may be connected to J700 to supply 7 V to 9 V.

Each supply is decoupled on the EVAL-AD7366SDZ/EVAL-AD7367SDZ using 10  $\mu$ F and 0.1  $\mu$ F capacitors.

**Table 3. External Power Supply Required**

Power Supply	Voltage Range	Purpose
VIN <sup>1</sup> J700 or J702	7 V to 9 V	Supplies all on-board power supplies, which generate all required voltages to run the evaluation board
VDD J100	12 V to 16.5 V	Amplifier +VDD
VSS J100	-12 V to -16.5 V	Amplifier -VSS
DVCC J703	4.75 V to 5.25 V	ADC digital supply
AVCC J704	4.7 V to 5.25 V	ADC analog supply
VDRIVE J1	2.7 V to 5.25 V	Supply voltage for the digital interface circuitry

<sup>1</sup> When this is supplied, all other power supplies are available on board. If this supply is not used, then all other supplies must be sourced from an external source.

## SERIAL INTERFACE

The AD7366/AD7367 uses a high speed serial interface, which allows sampling rates up to 800000. For details on the operation of the serial bus, refer to the AD7366/AD7367 data sheet.

The EVAL-AD7366SDZ/EVAL-AD7367SDZ communicates with the EVAL-SDP-CB1Z board using level shifters. The EVAL-SDP-CB1Z operates at a 3.3 V logic level. This allows VDRIVE voltages that exceed 3.3 V to be used without damaging the SDP interface.

Details of the serial interface can be found in the AD7366/AD7367 data sheet.

## SDP LIMITATIONS

Due to limitations in the speed of the EVAL-SDP-CB1Z in this application, the maximum sample rate is limited to 800000 samples per second. This limitation does not apply when using the EVAL-AD7366SDZ/EVAL-AD7367SDZ in standalone mode.

## STANDALONE MODE

The evaluation board may also be used without the EVAL-SDP-CB1Z. In this case, connection to the digital interface is made via the SMB connectors or, if preferred, by the test points.

## ANALOG INPUTS

The analog inputs on the EVAL-AD7366SDZ/EVAL-AD7367SDZ are filtered and buffered by the AD8021, low noise, high speed amplifier for 16-bit systems. The outputs from these amplifiers are connected to the AD7366/AD7367 via a low-pass RC filter network.

Alternatively, these buffers may be bypassed by solder link jumpers.

## REFERENCE OPTIONS

The reference source can be from the AD7366/AD7367 REFIN/REFOUT pin or from an AD780. An external reference voltage may also be applied to DCAP\_A or DCAP\_B SMB connectors

## SOCKETS/CONNECTORS

The functions of the socket connectors are shown in Table 4.

**Table 4. Socket Connector Functions**

Socket	Function
VA1	Input SMB for VA1
VA2	Input SMB for VA2
VB1	Input SMB for VB1
VB2	Input SMB for VB2
J1	VDRIVE terminal connectors
VIN	Bipolar input
DCAPA/B_BUFF	Buffered output of DCAPA/DCAPB
EXT REFA/B	Connection point for external reference to bias up circuit
BIASED_VIN1	Biased version of signal at VIN socket
DCAP_A	External input for DCAPA
DCAP_B	External input for DCAPB
DOUT_A	External serial data A output
DOUT_B	External serial data B output
CONVST	External CONVST input
CS	External CS input
BSY	External serial data output
SCK	External SCK input
J100	VSS and VDD screw terminal connectors
J700	7 V to 9 V bench supply screw terminal connector
J702	7 V to 9 V dc transformer power connector
J703	AVCC screw terminal connectors



## BASIC HARDWARE SETUP

The [AD7366/AD7367](#) evaluation board connects to the ([EVAL-SDP-CB1Z](#)) system demonstration board. The [EVAL-SDP-CB1Z](#) board is the controller board, which is the communication link between the PC and the main evaluation board.

Figure 2 shows a photograph of the connections made between the [AD7366/AD7367](#) daughter board and the [EVAL-SDP-CB1Z](#) board.

Before connecting power, connect the [EVAL-AD7366SDZ/EVAL-AD7367SDZ](#) board to connector A or connector B on the [EVAL-SDP-CB1Z](#) board. Nylon screws are included in the evaluation kit and can be used to ensure that the [EVAL-AD7366SDZ/EVAL-AD7367SDZ](#) board and the [EVAL-SDP-CB1Z](#) board are connected firmly together.

Once the [EVAL-AD7366SDZ/EVAL-AD7367SDZ](#) board and the [EVAL-SDP-CB1Z](#) board are connected securely, connect

the power supplies on the evaluation board. The [EVAL-AD7366SDZ/EVAL-AD7367SDZ](#) requires an external power supply, which is included in the evaluation board kit. Connect this power supply to the connector J702 on the [EVAL-AD7366SDZ/EVAL-AD7367SDZ](#) board. Alternatively, a bench power supply may be used to power the [EVAL-AD7366SDZ/EVAL-AD7367SDZ](#) via J700. Further details on the required power supplies connections and options are detailed in Table 4.

Before connecting the [EVAL-SDP-CB1Z](#) board to your PC, ensure that the [AD7366/AD7367](#) software has been installed from the enclosed CD. The full software installation procedure is detailed in the Evaluation Board Software section.

Finally, connect the [EVAL-SDP-CB1Z](#) board to the PC via the USB cable enclosed in the [EVAL-SDP-CB1Z](#) kit. If using Windows® XP platform, you may need to search for the [EVAL-SDP-CB1Z](#) drivers. Choose to automatically search for the drivers for the [EVAL-SDP-CB1Z](#) board if prompted by the operating system.

# EVALUATION BOARD SOFTWARE

## SOFTWARE INSTALLATION

The EVAL-AD7366SDZ/EVAL-AD7367SDZ evaluation kit includes software on a CD. Click the **setup.exe** file from the CD to run the install. The default location for the software is C:\Program Files\Analog Devices\AD7366\AD7367.

It is important to install the evaluation software before connecting the evaluation board and the **EVAL-SDP-CB1Z** board to the USB port of the PC. This ensures that the evaluation system is correctly recognized when connected to the PC.

There are two parts to the installation

1. **AD7366/AD7367** evaluation board software installation.
2. **EVAL-SDP-CB1Z** system demonstration platform board drivers installation.

Figure 3 to Figure 7 show the separate stages of the evaluation software. Figure 8 to Figure 12 show the separate steps to install the **EVAL-SDP-CB1Z** drivers. Proceed through all of the installation steps, allowing the software and drivers to be placed in the appropriate locations. Only after the software and drivers have been installed should you connect the **EVAL-SDP-CB1Z** board to the PC.



Figure 5. AD7366/AD7367 Install Window 3

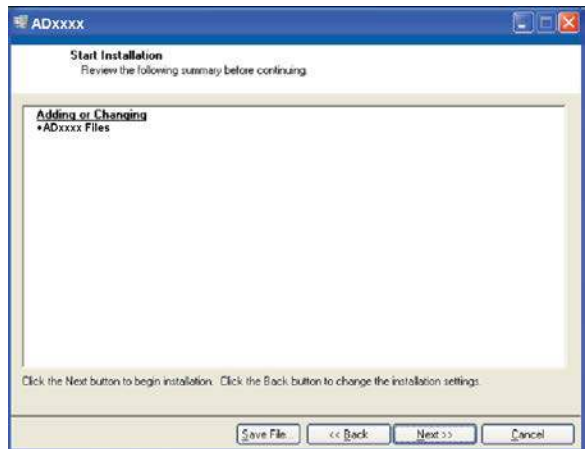


Figure 6. AD7366/AD7367 Install Window 4

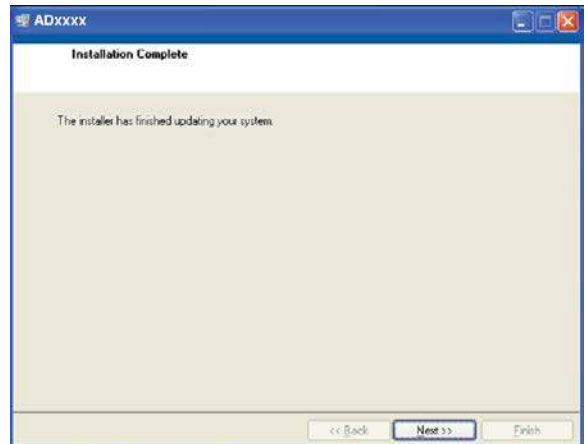


Figure 7. AD7366/AD7367 Install Window 5.

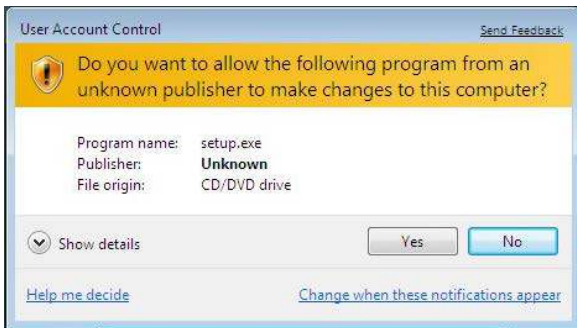


Figure 3. AD7366/AD7367 Install Window 1

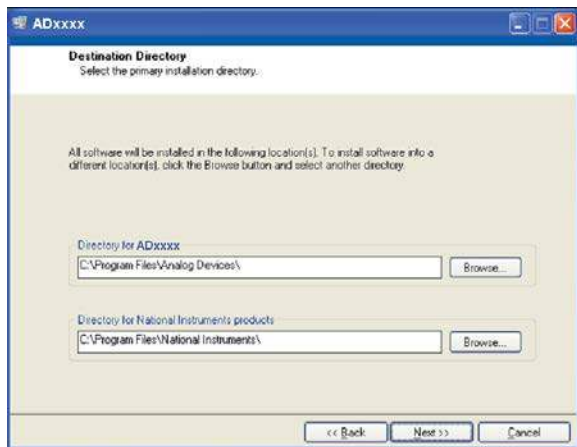
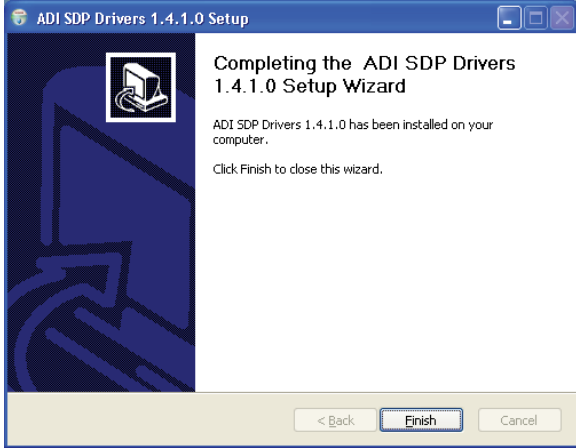
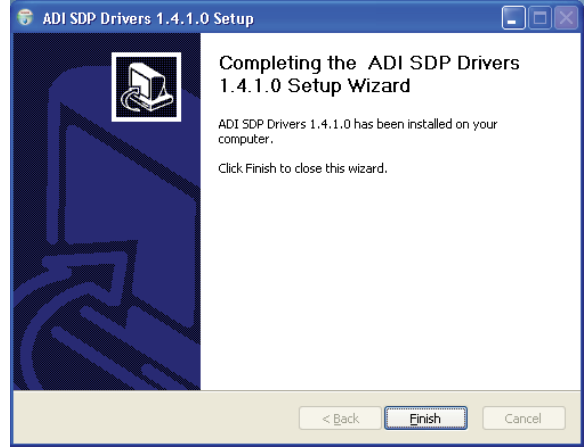


Figure 4. AD7366/AD7367 Install Window 2



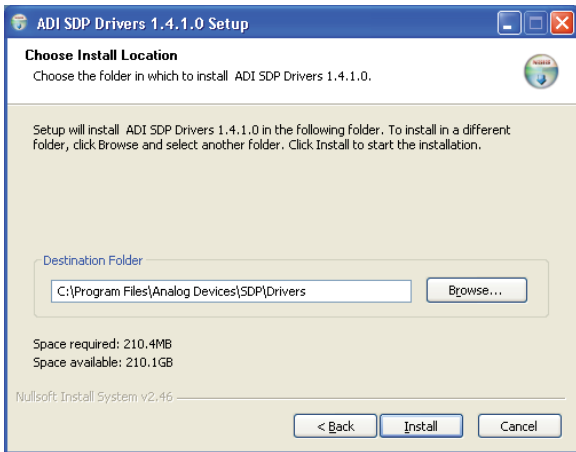
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Figure 8. ADI EVAL-SDP-CB1Z Drivers Setup Window 1



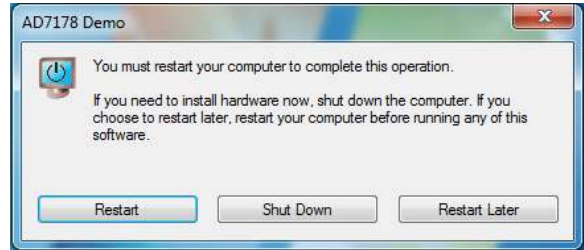
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Figure 11. ADI EVAL-SDP-CB1Z Drivers Setup Window 4



06704-009

Figure 9. ADI EVAL-SDP-CB1Z Drivers Setup Window 2



06704-012

Figure 12. ADI EVAL-SDP-CB1Z Drivers Setup Window 5



06704-010

Figure 10. ADI EVAL-SDP-CB1Z Drivers Setup Window 3

After installation from the CD is complete, connect the [AD7366/AD7367](#) evaluation board to the [EVAL-SDP-CB1Z](#) as described in the Evaluation Board Hardware section.

When you first plug in the [EVAL-SDP-CB1Z](#) board via the USB cable provided, allow the new **Found Hardware Wizard** to run. Once the drivers are installed, you may check that the board has connected correctly by looking at the **Device Manager** of the PC. The **Device Manager** can be found by right clicking on **My Computer>Manage>Device Manager** from the list of **System Tools** as shown in Figure 13. The [EVAL-SDP-CB1Z](#) board should appear under **ADI Development Tools**. This completes the installation.



Figure 13. Device Manager

06704-013

**LAUNCHING THE SOFTWARE**

Once the [AD7366SDZ/EVAL-AD7367SDZ](#) and [EVAL-SDP-CB1Z](#) are correctly connected to your PC, the [AD7366/AD7367](#) software can be launched.

To launch the software, complete the following steps:

1. From the **Start** menu, select **Programs>Analog Devices>AD7366/AD7367**. The main window of the software then displays.
2. If the [AD7366/AD7367](#) evaluation system is not connected to the USB port via the [EVAL-SDP-CB1Z](#) when the software is launched, a connectivity error displays (see Figure 14). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

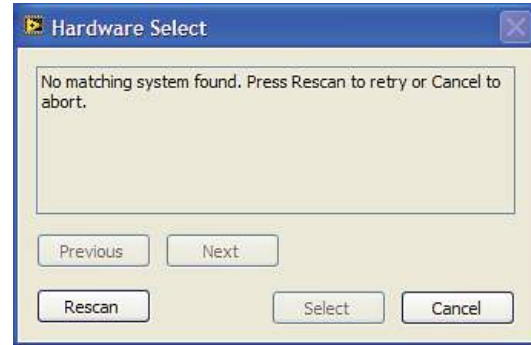


Figure 14. Connectivity Error Alert

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**SOFTWARE OPERATION**

When the software is launched, the panel opens and the software looks for hardware connected to the PC. The software detects the generic attached to the PC and returns this in a user dialog box.

The user software panel then launches as shown in Figure 15.

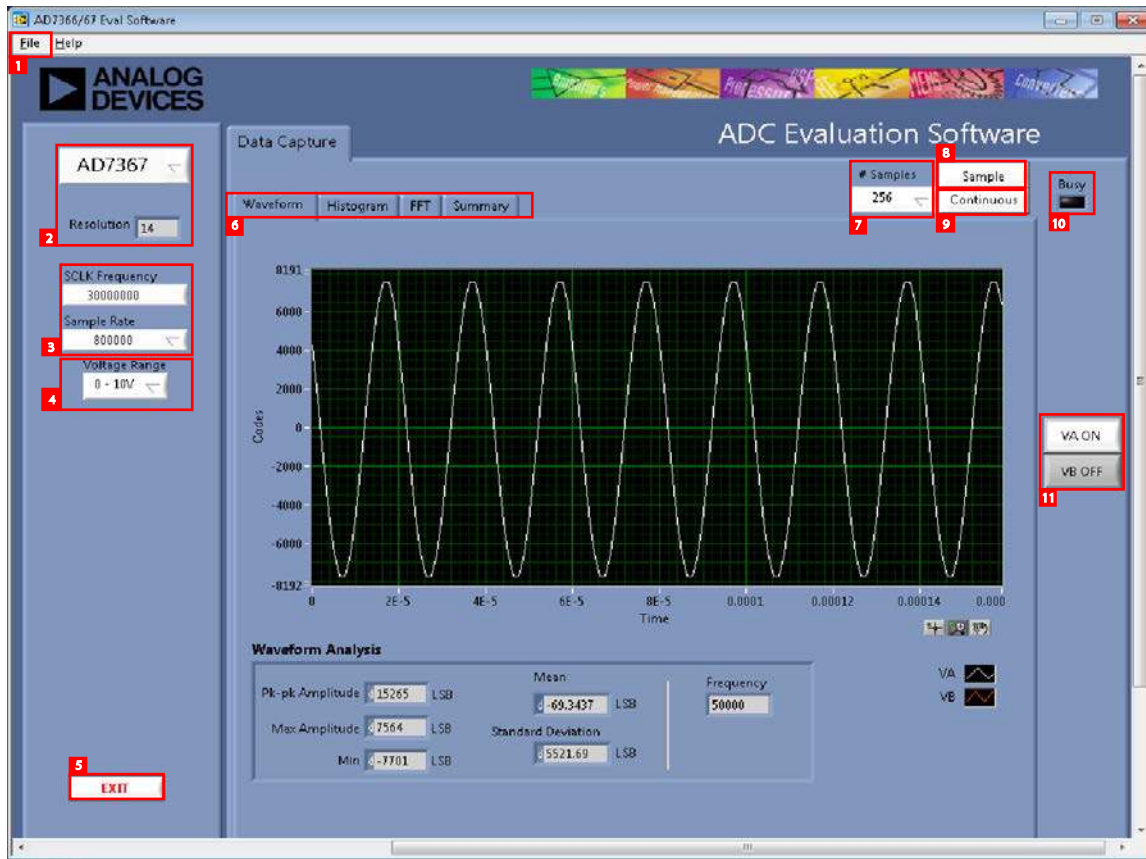


Figure 15. User Software Panel

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## DESCRIPTION OF USER SOFTWARE PANEL

The user software panel, as shown in Figure 15, has the following features. Refer to the labels numbered 1 through 11.

**File** menu (labeled 1 in Figure 15) offers choices of

- Load data. Load previously captured data in tab separated values (tsv) format for analysis.
- Save data as .tsv. Save captured data in tsv format for future analysis.
- Print front panel picture. Use to print the front panel to your default printer.
- Save picture. Use to save the current screen capture.
- Exit.

Drop-down menu (labeled 2 in Figure 15) is used to select the generic [AD7366](#) or [AD7367](#). The resolution of selected part is displayed.

**Sample Rate** (labeled 3 in Figure 15) can be selected from the drop-down menu. Rates of 800 kSPS, 500 kSPS, 400 kSPS, 200 kSPS, 100 kSPS, and 50 kSPS are allowed.

The SCLK frequency is fixed to 30 MHz when using the EVAL-AD7366SDZ/EVAL-AD7367SDZ in conjunction with the [EVAL-SDP-CB1Z](#) board.

**Voltage Range** (labeled 4 in Figure 15). Use this in conjunction with LK18 and LK19. Ensure that this setting matches the hardware setting.

**Exit** (labeled 5 in Figure 15). Use this to exit the software. Alternatively, go to **File>Exit**.

There are four tabs (labeled 6 in in Figure 15) available displaying the data in different formats:

- Waveform
- Histogram
- FFT
- Summary

Select the number of samples (labeled 7 in Figure 15) to analyze.

Choose **Sample** to perform a single capture (labeled 8 in Figure 15).

Choose **Continuous** to perform a continuous capture (labeled 9 in Figure 15) from the ADC. Click again to stop sampling.

This LED (labeled 10 in Figure 15) indicates when a read is in progress from the [EVAL-SDP-CB1Z](#) board.

Channel display buttons (labeled 11 in Figure 15). Use these to display multiple channel reads on the display. Select only one channel for FFT analysis.

Within any of the chart panels, the following tools allow user control of the different chart displays:



is used for controlling the cursor, if present.



is used for zooming in and out.



is used for panning.



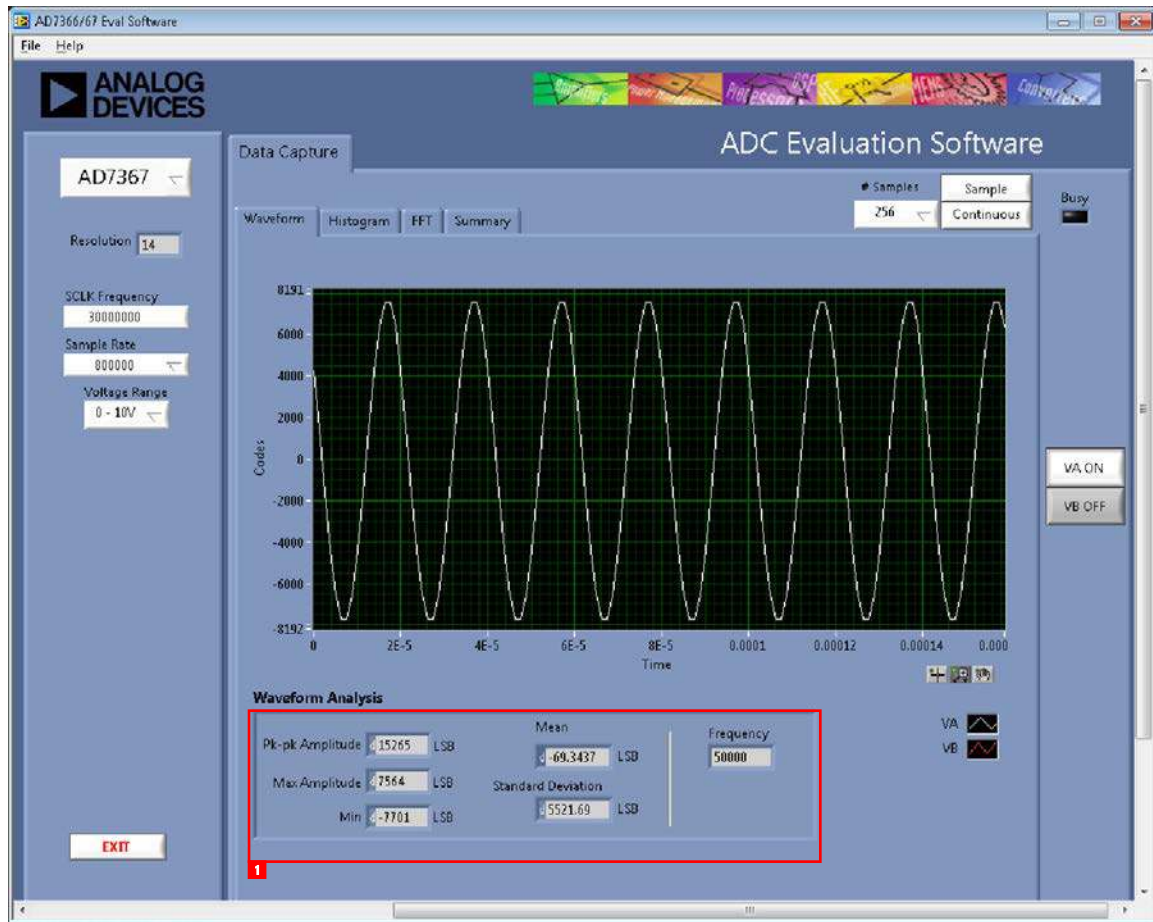


Figure 16. Waveform Capture Tab

**WAVEFORM CAPTURE**

Figure 16 illustrates the waveform capture tab. The input signal here is a 50 kHz sine wave.

The waveform analysis (labeled 1) reports back the amplitudes recorded from the captured signal in addition to the frequency of the signal tone.

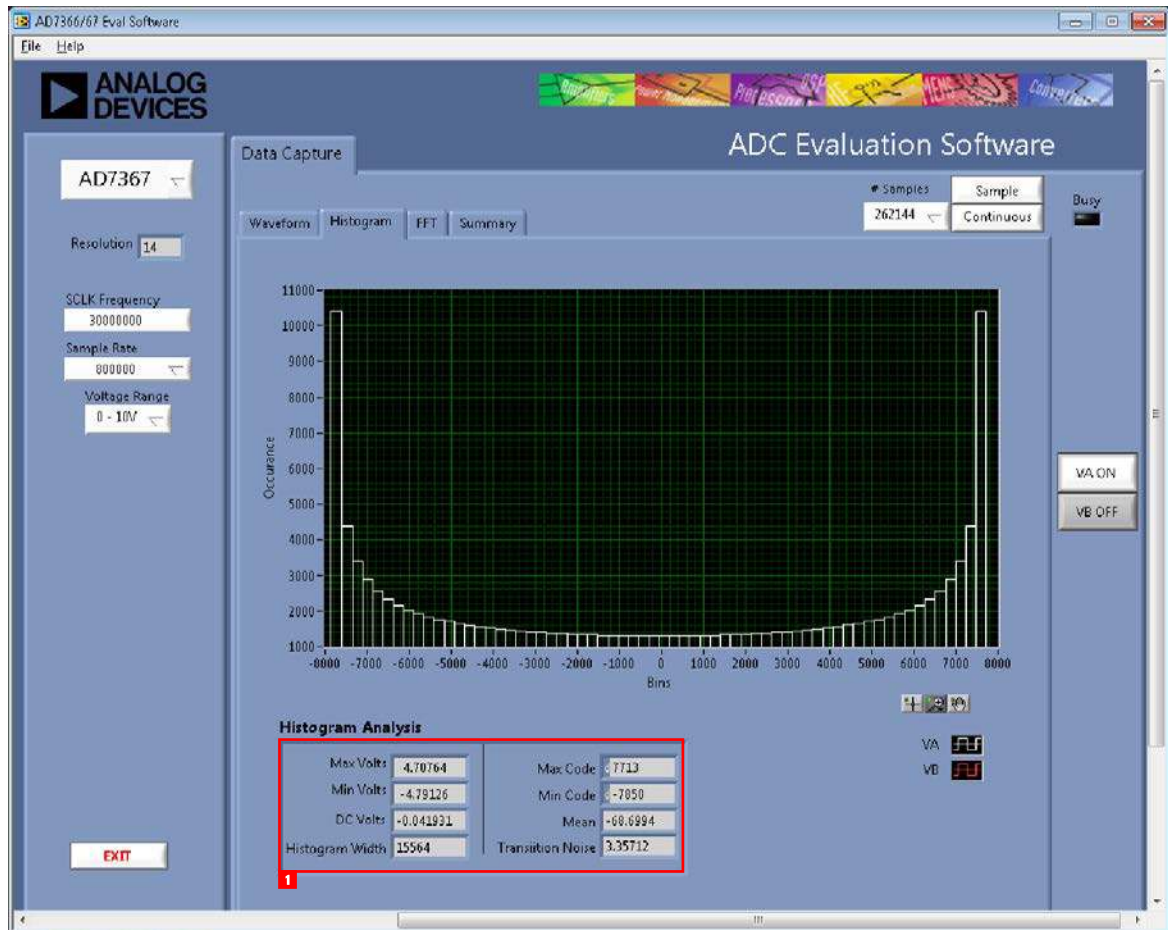


Figure 17. Histogram Capture Tab

## AC TESTING–HISTOGRAM

Figure 17 shows the histogram capture tab. This tests the ADC for the code distribution for ac input. In addition, it computes the mean and standard deviation, or transition noise of the converter, and displays the results.

Raw data is captured and passed to the PC for statistical computations. To perform a histogram test, select the **Histogram** tab from the test selection window and click **Start**.

Note that an ac histogram needs a quality signal source applied to the input SK1/SK3 connectors. Figure 17 shows the histogram for a 50 kHz sine wave applied to the ADC input with the results calculated.

The area labeled as 1 in Figure 17 illustrates the different measured values for the data captured.

## DC TESTING–HISTOGRAM

More commonly, the histogram is for dc testing. In these cases, a user tests the ADC for the code distribution for dc input and computes the mean and standard deviation, or transition noise of the converter, and displays the results. Raw data is captured and passed to the PC for statistical computations. To perform a histogram test, select the **Histogram** tab from the test selection window and click **Start**.





Figure 18. FFT Capture Tab

### AC TESTING—FFT CAPTURE

Figure 18 shows the FFT capture tab. This tests the traditional ac characteristics of the converter and displays a fast Fourier transform (FFT) of the results. As in the histogram test, raw data is captured and passed to the PC where the FFT is performed displaying SNR, SINAD, THD, and SFDR.

To perform an ac test, apply a sinusoidal signal to the evaluation board at the SMB inputs J4/63. Low distortion, better than 115 dB, is required to allow true evaluation of the part. One possibility is to filter the input signal from the ac source. There is no suggested band-pass filter, but consideration should be taken in the choice. Furthermore, if using a low frequency

band-pass filter when the full-scale input range is more than a few V p-p, it is recommended to use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

Figure 18 displays the results of the captured data. Label 1 in Figure 18 shows the input signal information. The portions of Figure 18 labeled 2 display the fundamental frequency and amplitude in addition to the 2<sup>nd</sup> to 5<sup>th</sup> harmonics. See label 3 also which displays the performance data (SNR, dynamic range, THD, SINAD, and noise performance.)

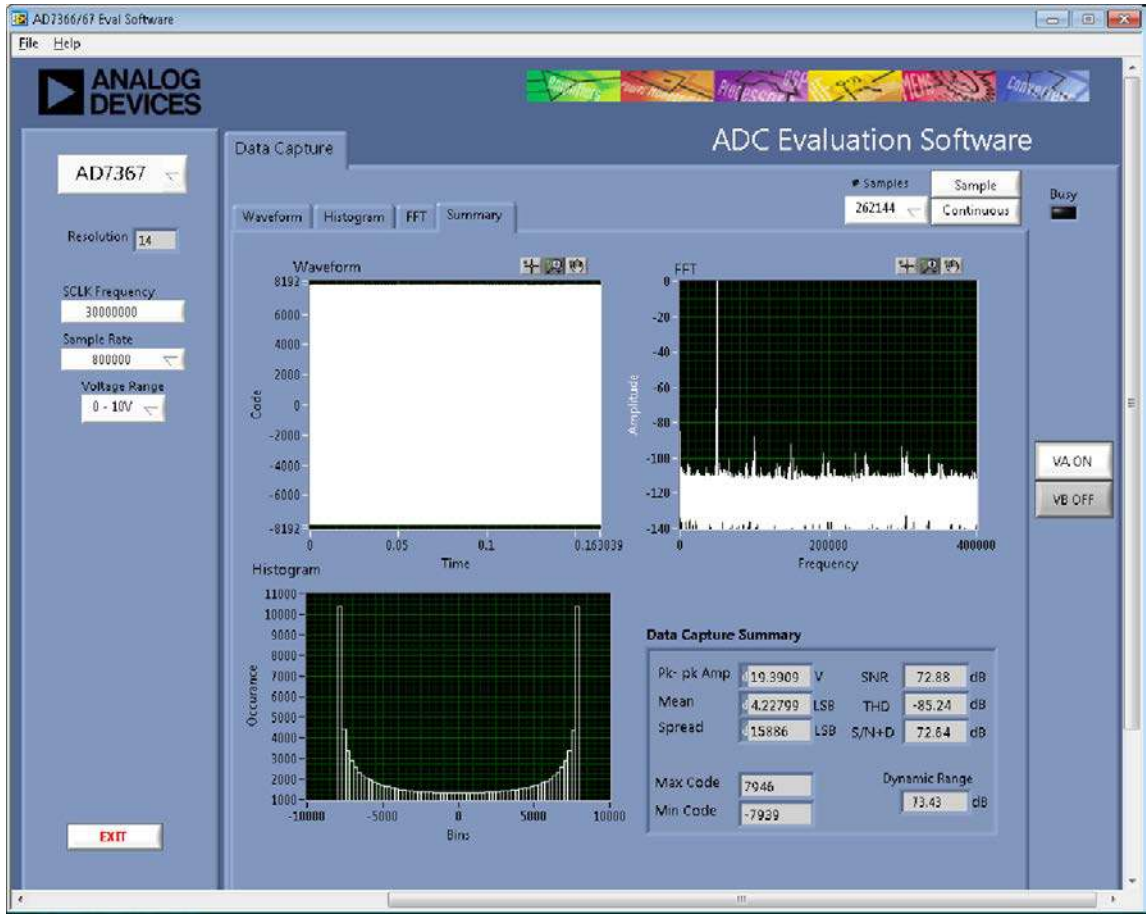


Figure 19. Summary Tab

**SUMMARY TAB**

Figure 19 shows the summary tab. This tab captures display information and provides this data in one panel with a synopsis of the information, including key performance parameters, such as SNR and THD.

**SAVE FILE**

The software can save the current captured data for later analysis; the file format is .tsv (tab separated values) (see Figure 20).

Users are prompted with a **Save** dialog box and should save to an appropriate folder location

**LOAD FILE**

User is prompted with a load dialog box. User may have to navigate to find these example files (see Figure 21). The default location for the example files is C:\Program Files\Analog Devices\AD7366\examples.

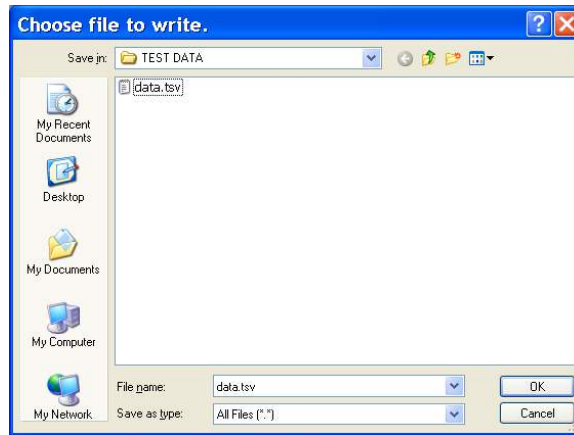


Figure 20. Save File Dialog Box

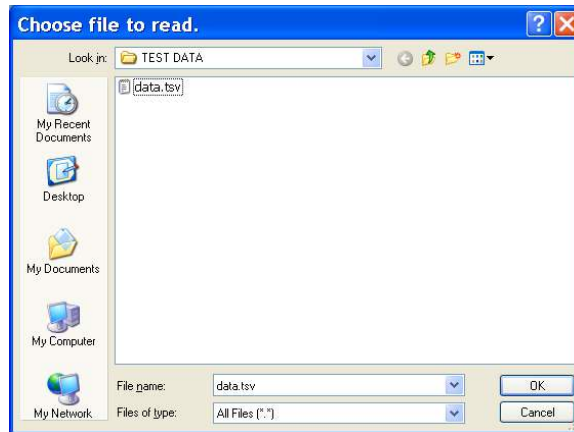


Figure 21. Load File Dialog Box

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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