Current Mode Boost Controller

General Description

The RT8525D is a wide input operating voltage range step up controller. High voltage output and large output current are feasible by using an external N-MOSFET. The RT8525D input operating range is from 4.5V to 25V.

The RT8525D is an optimized design for wide output voltage range applications. The output voltage of the RT8525D can be adjusted by the FB pin.

Ordering Information

RT8525D□□

Package Type
QW : WDFN-12L 3x3 (W-Type)
(Exposed Pad-Option 2)

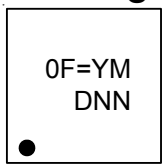
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



0F= : Product Code

YMDNN : Date Code

Features

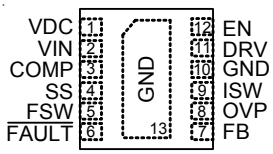
- **VIN Range : 4.5V to 25V**
- **Programmable Soft-Start Time**
- **Programmable Boost SW Frequency from 50kHz to 600kHz**
- **Output Over Voltage Protection**
- **Output Under Voltage Protection**
- **12-Lead WDFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- LCD TV, Monitor Display Backlight
- LED Driver Application
- High Current High Output Voltage DC/DC Converters
- High Input Voltage DC/DC Converters

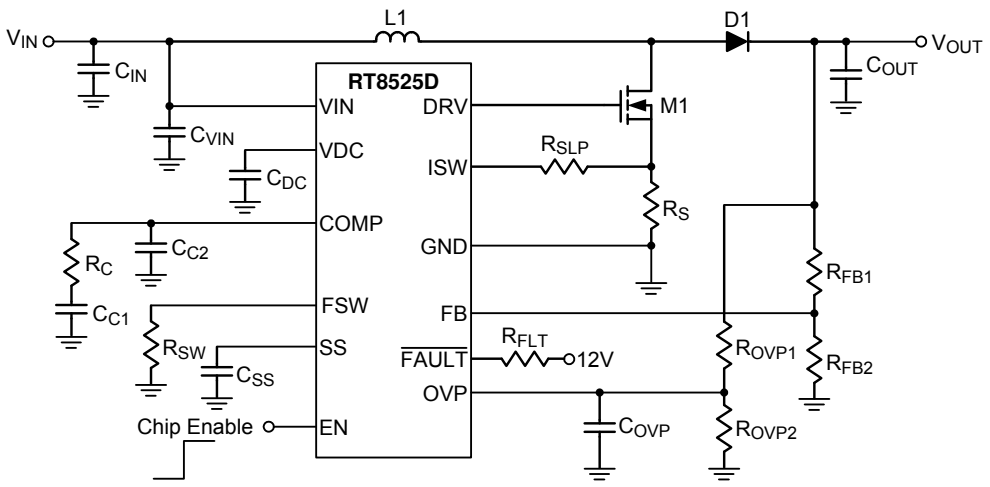
Pin Configurations

(TOP VIEW)



WDFN-12L 3x3

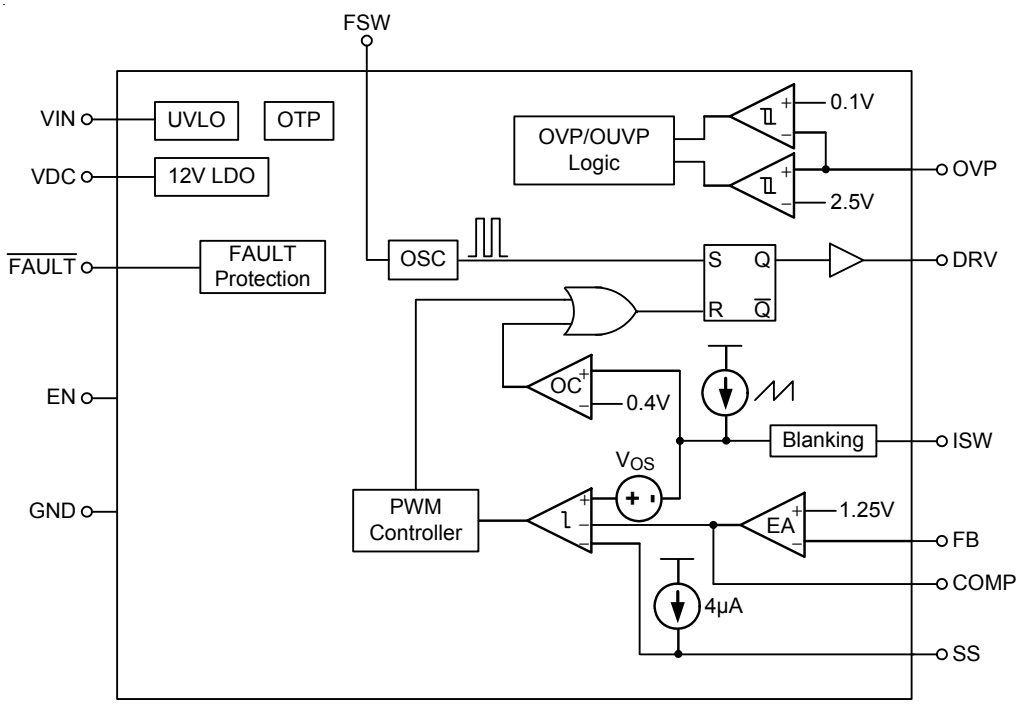
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDC	Output of Internal Pre-Regulator.
2	VIN	IC Power Supply.
3	COMP	Compensation for Error Amplifier. Connect a compensation network to ground.
4	SS	External Capacitor to Adjust Soft-Start Time.
5	FSW	Frequency Adjust Pin. This pin allows setting the switching frequency with a resistor from 50kHz to 600kHz.
6	$\overline{\text{FAULT}}$	Open Drain Output for Fault Detection.
7	FB	Feedback to Error Amplifier Input.
8	OVP	Sense Output Voltage for Over Voltage Protection and Under Voltage Protection.
9	ISW	External MOSFET Switch Current Sense Pin. Connect the current sense resistor between the external N-MOSFET switch and ground.
10, 13 (Exposed Pad)	GND	Ground of Boost Controller. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
11	DRV	Drive Output for the N-MOSFET.
12	EN	Chip Enable (Active High).

Function Block Diagram



Operation

The RT8525D is a wide input operating voltage range and current mode step up controller. High voltage output and large output current are feasible by using an external N-MOSFET.

The error amplifier EA adjusts COMP voltage by comparing the feedback signal from the output voltage with the internal 1.25V reference.

Fault Protection

The protection functions include output over voltage, output under voltage, over temperature protection. The $\overline{\text{FAULT}}$ pin will be pulled low once a protection is triggered, and a suitable pulled-high R_{FLT} is required. The detail description can refer to the Figure 2. Fault Protection Function Block.

Blanking

N-MOSFET current is measured by external RS. The slope compensator works together with sensing voltage of R_{SENSE} to the ISW pin. There is need blanking time to avoid noise and parasitism effect.

Absolute Maximum Ratings (Note 1)

- VIN to GND ---------- –0.3V to 26.4V
- VDC, DRV, $\overline{\text{FAULT}}$ to GND ---------- –0.3V to 13.2V
- EN, COMP, SS, FSW, FB, OVP, ISW to GND ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-12L 3x3 ---------- 1.667W
- Package Thermal Resistance (Note 2)
  WDFN-12L 3x3, θ_{JA} ---------- 60°C/W
  WDFN-12L 3x3, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 21V, C_{IN} = 10µF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply							
Quiescent Current		I_Q	No Switching, R_{SW} = 56kΩ	--	1.3	2	mA
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	10	--	µA
Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	--	3.8	--	V
Under Voltage Lockout Hysteresis		ΔV_{UVLO}		--	500	--	mV
12V Regulator							
Regulator Output Voltage		V_{DC}	13.5V < V_{IN} < 16V, 1mA < I_{LOAD} < 100mA	11.4	12	12.6	V
			16V < V_{IN} < 20V, 1mA < I_{LOAD} < 50mA				
			20V < V_{IN} < 25V, 1mA < I_{LOAD} < 20mA				
Dropout Voltage		V_{DROP}	V_{IN} – V_{DC}, V_{IN} = 12V, I_{LOAD} = 100mA	--	500	--	mV
Short-Circuit Current Limit		I_{SC}	V_{DC} Short to GND	--	270	--	mA
Control Input							
EN Threshold Voltage	Logic-High	V_{IH}		2	--	--	V
	Logic-Low	V_{IL}		--	--	0.8	
EN Sink Current		I_{IH}	V_{EN} = 5V	--	5	--	µA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Delay	Sleeping Mode	t_{SLEEP}	R_{SW} = 56kΩ, EN = L, 12V Regular Shutdown	55	--	--	ms
	Shutdown Mode	t_{SHDN}	R_{SW} = 56kΩ, EN = L, IC Shutdown	110	--	--	ms
Boost Controller							
Switching Frequency		f_{SW}	R_{SW} = 56kΩ	--	200	--	kHz
Minimum On-Time		t_{MON}		--	250	--	ns
Maximum Duty		D_{MAX}	Switching	90	--	--	%
Feedback Voltage		V_{FB}		--	1.25	--	V
Slope Compensation							
Peak Magnitude of Slope Compensation Current		$I_{SLOPE, PK}$		--	50	--	μA
Soft-Start							
Soft-Start Current		I_{SS}		3	4	5	μA
Gate Driver							
DRV On-Resistance		$R_{DS(ON)\_N}$	I_{SINK} = 100mA (N-MOSFET)	--	1	--	Ω
		$R_{DS(ON)\_P}$	I_{SOURCE} = 100mA (P-MOSFET)	--	1.5	--	Ω
Peak Sink Current		I_{PEAKsk}	C_{LOAD} = 1nF	--	2.2	--	A
Peak Source Current		I_{PEAKsr}	C_{LOAD} = 1nF	--	2.55	--	A
Rise Time		t_r	C_{LOAD} = 1nF	--	6	--	ns
Fall Time		t_f	C_{LOAD} = 1nF	--	5	--	ns
Protection Function							
OCP Threshold		V_{OCP}	Including Slope Compensation Magnitude	--	0.4	--	V
V_{OUT} OVP Threshold		V_{OVP}		--	2.5	--	V
V_{OUT} UVP Threshold		V_{UVP}		--	0.1	--	V
Thermal Shutdown Temperature		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	50	--	°C

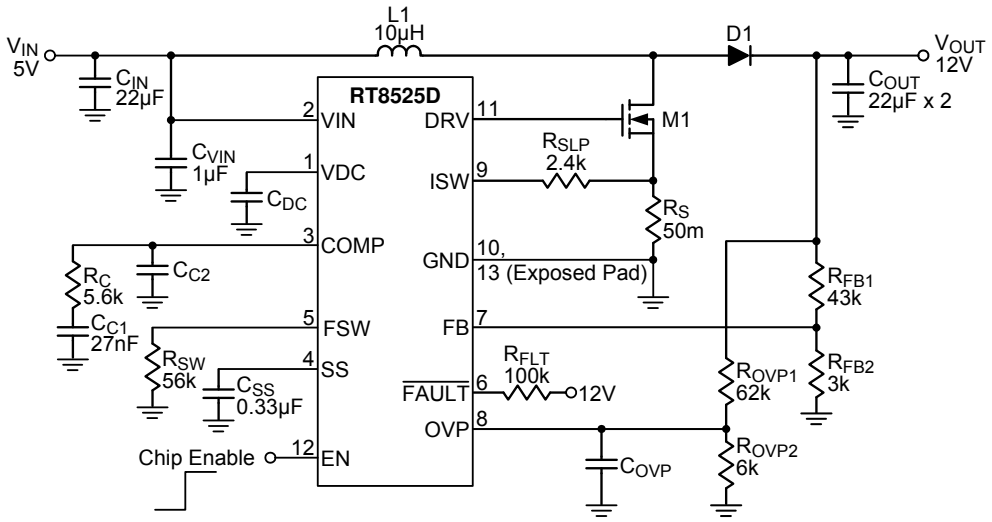
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

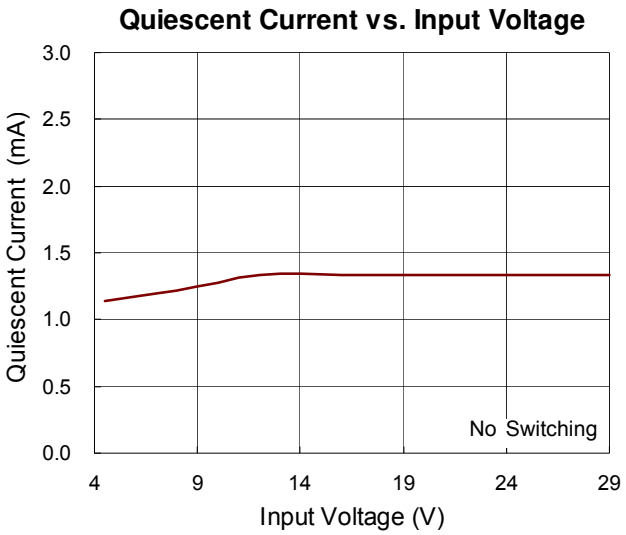
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

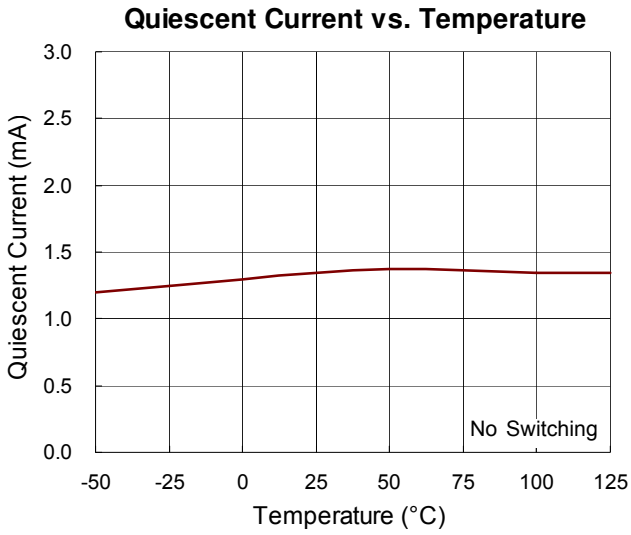
Note 4. The device is not guaranteed to function outside its operating conditions..

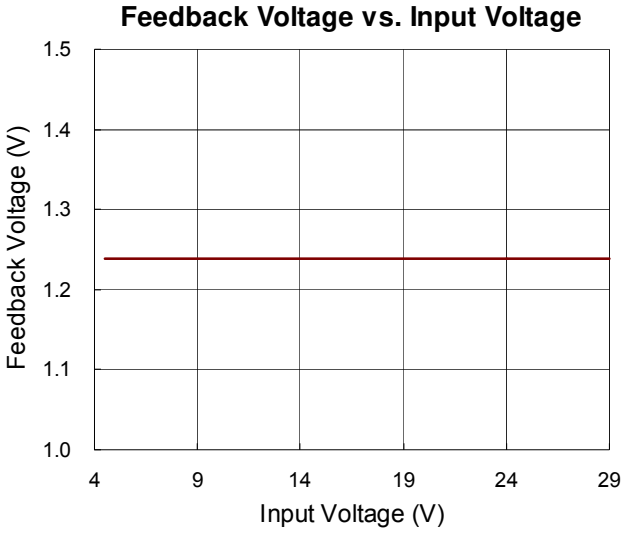
Typical Application Circuit

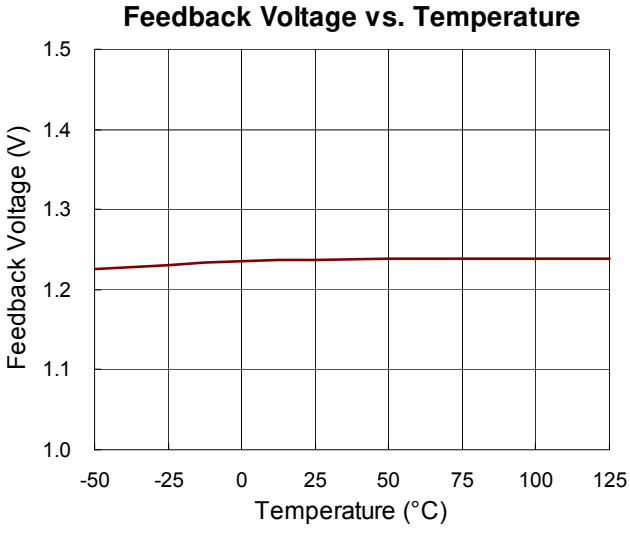


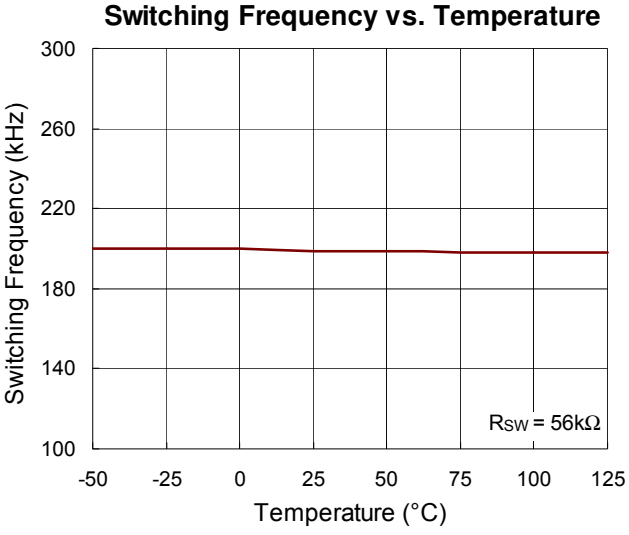
Typical Application Circuit

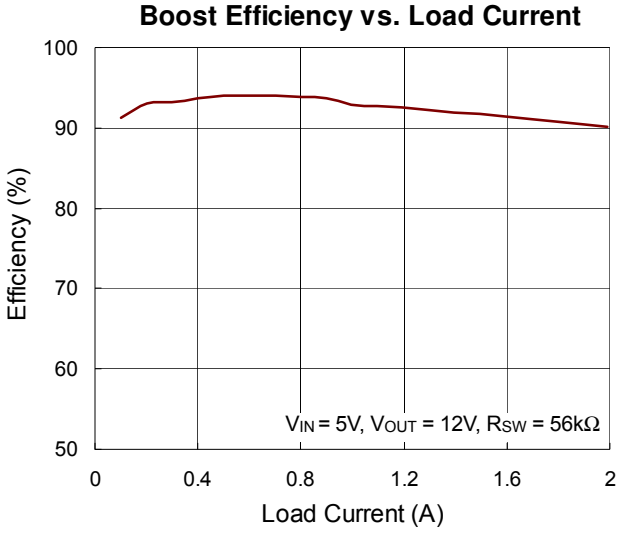












Applications Information

The RT8525D is a wide input operating voltage range step up controller. High voltage output and large output current are feasible by using an external N-MOSFET. The protection functions include output over voltage, output under voltage, over temperature and current limiting protection.

Boost Output Voltage Setting

The regulated output voltage is set by an external resistor divider according to the following equation :

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right), \text{ where } V_{FB} = 1.25V \quad (typ.)$$

The recommended value of R_{FB2} should be at least 1kΩ for saving sacrificing. Moreover, placing the resistor divider as close as possible to the chip can reduce noise sensitivity.

Boost Switching Frequency

The RT8525D boost driver switching frequency is able to be adjusted by a resistor R_{SW} ranging from 18kΩ to 220kΩ. The following figure illustrates the corresponding switching frequency within the resistor range.

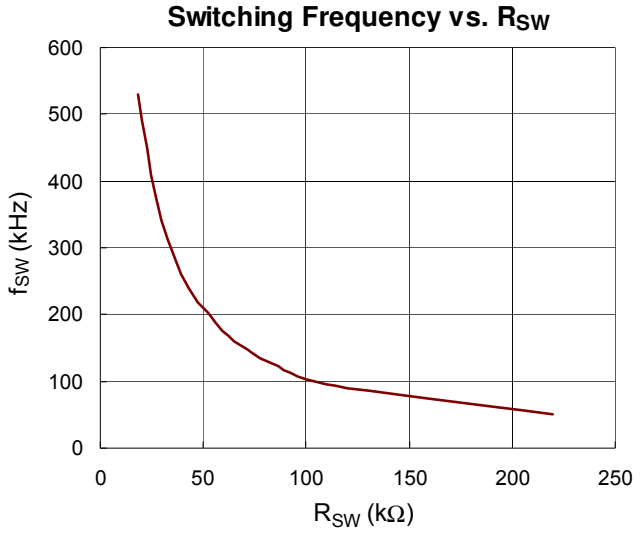


Figure 1. Boost Switching Frequency

Boost Loop Compensation

The voltage feedback loop can be compensated by an external compensation network consisted of R_C, C_{C1} and C_{C2}. Choose R_C to set high frequency gain for fast transient response. Select C_{C1} and C_{C2} to set the zero and pole to maintain loop stability. A typical compensation for the RT8525D is choosing 3kΩ for R_C and 27nF for C_{C1}.

Soft-Start

The soft-start of the RT8525D can be achieved by connecting a capacitor from the SS pin to GND. The built-in soft-start circuit reduces the start-up current spike and output voltage overshoot. The external capacitor charged by an internal 4μA constant charging current determines the soft-start time. The SS pin limits the rising rate of the COMP pin voltage and thereby limits the peak switch current. The soft-start interval is set by the soft-start capacitor according to the following equation :

$$t_{SS} \cong C_{SS} \times 5 \times 10^5$$

A typical value for the soft-start capacitor is 0.33μF. The soft-start capacitor is discharged when EN voltage falls below its threshold after shutdown delay or UVLO occurs.

Slope Compensation and Current Limiting

A slope compensation is applied to avoid sub-harmonic oscillation in current-mode control. The slope compensation voltage is generated by the internal ramp current flow through a slope compensation resistor R_{SLP}. The inductor current is sensed by the sensing resistor R_S. Both of them are added and presented on the ISW pin. The internal ramp current is rising linearly form zero at the beginning of each switching cycle to 50μA in maximum on-time of each cycle. The slope compensation resistor R_{SLP} can be calculated by the following equation :

$$R_{SLP} > \frac{(V_{OUT} - V_{IN}) \times R_S}{2 \times L \times 50\mu \times f_{SW}}$$

where R_S is current sensing resistor, L is inductor value, and f_{SW} is boost switching frequency.

The current flow through inductor during charging period is detected by a sensing resistor R_S. Besides, the slope compensation voltage also attributes magnitude to ISW. As the voltage at the ISW pin is over 0.4V, the DRV will be pulled low and turn off the external N-MOSFET. So that the inductor will be forced to leave charging stage and enter discharging stage to prevent over current. The current limiting can be calculated by the following equation:

$$R_S < \frac{0.4 - D_{MAX} \times R_{SLP} \times 50\mu}{I_{L,PK}}$$

where $I_{L,PK}$ is peak inductor current, and D_{MAX} is maximum duty.

Output Over Voltage Protection

The output voltage can be clamped at the voltage level determined by the following equation :

$$V_{OUT\,(OVP)} = V_{OVP} \times \left(1 + \frac{R_{OVP1}}{R_{OVP2}}\right),$$

where V_{OVP} = 2.5V (typ.)

where R_{OVP1} and R_{OVP2} are the voltage divider connected to the OVP pin.

Fault Protection

The $\overline{FAULT}$ pin will be pulled low once a protection is triggered, and a suitable pulled-high R_{FLT} is required. The suggested R_{FLT} is 100kΩ if the pulled-high voltage was 12V. The following figure illustrates the fault protection function block. If one of the OUVP and OTP occurs, the switch 1 will be turned on, and the voltage at node A will be under 0.25V. Then the protection function will perform action 2 to turn off the driver. When protection function is released, the RT8525D will re-start.

On the other hand, if the triggered protection is OVP, the voltage at node A will be decided by voltage divider composed of R_{FLT} and the internal 8kΩ resistor. This voltage must be designed between 0.25V and 1.25V by choosing R_{FLT} appropriately. Once the OVP turns on the Switch 2, the divided $\overline{FAULT}$ voltage will activate action 1 to turn off the driver without resetting soft-start. Therefore, when protection function OVP is released, the RT8525D will be in normal operation.

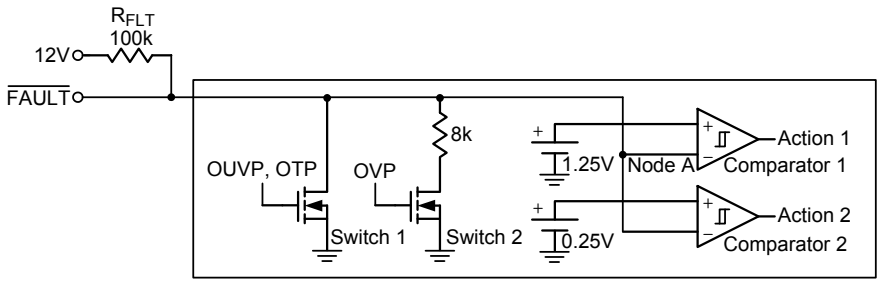


Figure 2. Fault Protection Function Block

Power MOSFET Selection

For the applications operating at high output voltage, switching losses dominate the overall power loss. Therefore, the power N-MOSFET switch is typically chosen for drain voltage, VDS, rating and low gate charge. Consideration of switch on-resistance $R_{DS(ON)}$ is usually secondary. The VDC regulator in the RT8525D has a fixed output current limit to protect the IC and provide 12V DRV voltage for N-MOSFET switch gate driver.

Inductor Selection

The boundary value of the inductance L between Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM) can be approximated by the following equation :

$$L = \frac{D \times (1-D)^2 \times V_{OUT}}{2 \times f_{SW} \times I_{OUT}}$$

where

V_{OUT} is the maximum output voltage,

V_{IN} is the minimum input voltage,

fsw is the operating frequency,

I_{OUT} is the sum of current from all LED strings,

and D is the duty cycle calculated by the following equation :

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

The boost converter operates in DCM over the entire input voltage range if the inductor value is less than the boundary value L. With an inductance greater than L, the converter operates in CCM at the minimum input voltage and may transit to DCM at higher voltages. The inductor must be selected with a saturated current rating greater than the peak current provided by the following equation :

$$I_{LPK} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} + \frac{VIN \times D \times T}{2 \times L}$$

where η is the efficiency of the power converter.

Diode Selection

Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. The power dissipation, reverse voltage rating and pulsating peak current are the important parameters for Schottky diode selection. Make sure that the diode's peak current rating exceeds I_{LPK}, and reverse voltage rating exceeds the maximum output voltage.

Capacitor Selection

Output ripple voltage is an important index for estimating the performance. This portion consists of two parts, one is the product of input current and ESR of output capacitor, another part is formed by charging and discharging process of output capacitor. Refer to figure 3, evaluate ΔV_{OUT1} by ideal energy equalization. According to the definition of Q, the Q value can be calculated as following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2} \Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2} \Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{SW}} = C_{OUT} \times \Delta V_{OUT1}$$

where f_{SW} is the switching frequency, and ΔI_L is the inductor ripple current. Move C_{OUT} to the left side to estimate the value of ΔV_{OUT1} as the following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{SW}}$$

Finally, by taking ESR into consideration, the overall output ripple voltage can be determined as the following equation :

$$\Delta V_{OUT} = I_{IN} \times ESR + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{SW}}$$

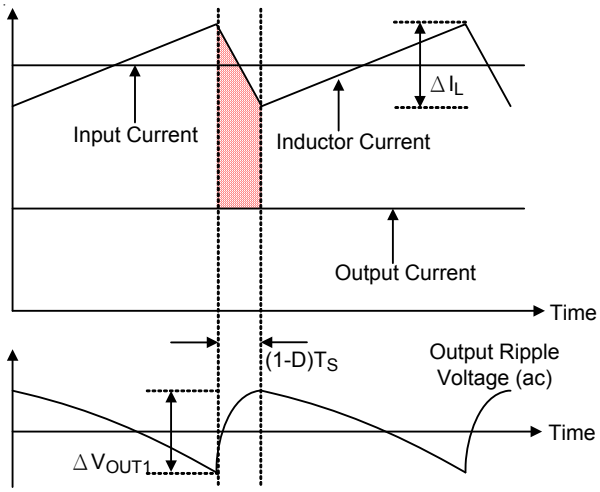


Figure 3. The Output Ripple Voltage without the Contribution of ESR

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-12L 3x3 package, the thermal resistance, θ_{JA}, is 60°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.667W for

WDFN-12L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal

resistance, θ_{JA}. The derating curve in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

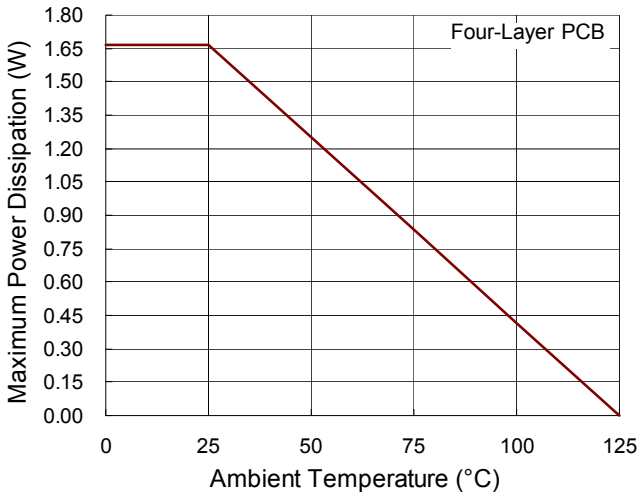


Figure 4. Derating Curve of Maximum Power Dissipation

Layout Considerations

PCB layout is very important for designing switching power converter circuits. The following layout guides should be strictly followed for best performance of the RT8525D.

- The power components L_1, D_1, C_{IN}, C_{OUT}, M1 and R_S must be placed as close as possible to reduce current loop. The PCB trace between power components must be as short and wide as possible.
- Place components R_{FB1} and R_{FB2} close to IC as possible. The trace should be kept away from the power loops and shielded with a ground trace to prevent any noise coupling.
- The compensation circuit should be kept away from the power loops and should be shielded with a ground trace to prevent any noise coupling. Place the compensation components to the COMP pin as close as possible, no matter the compensation is R_C, C_{C1} or C_{C2}.

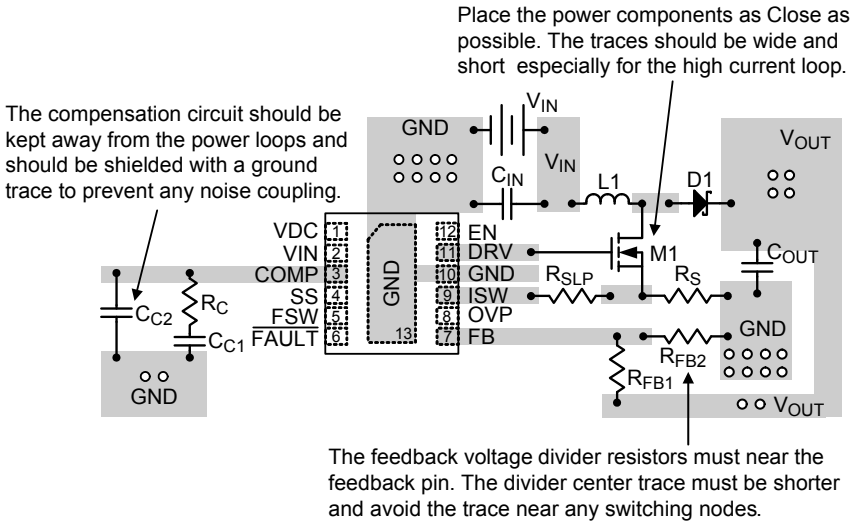
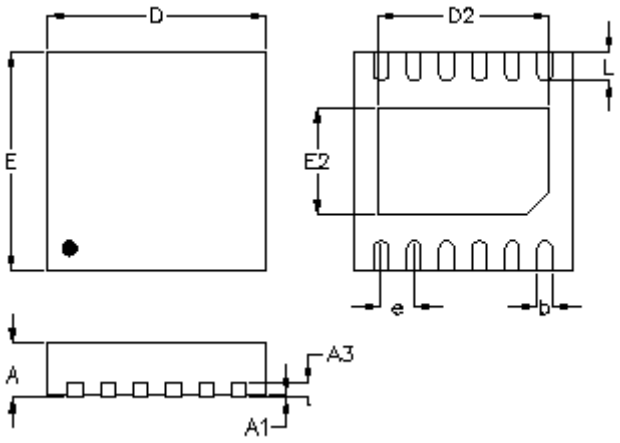
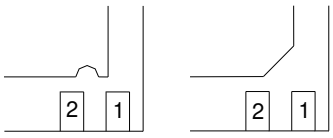


Figure 5. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		2.950	3.050	0.116	0.120
D2	Option1	2.300	2.650	0.091	0.104
	Option2	1.970	2.070	0.078	0.081
E		2.950	3.050	0.116	0.120
E2	Option1	1.400	1.750	0.055	0.069
	Option2	1.160	1.260	0.046	0.050
e		0.450		0.018	
L		0.350	0.450	0.014	0.018

W-Type 12L DFN 3x3 Package

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