ART150FE

Power LDMOS transistor

Rev. 2 — 8 July 2022

AMPLEON

Product data sheet

1. Product profile

1.1 General description

Based on Advanced Rugged Technology (ART), this 150 W LDMOS RF transistor has been designed to cover a wide range of applications for ISM, broadcast and communications. The unmatched transistor has a frequency range of 1 MHz to 650 MHz.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	64	65	150	31.3	71.4
CW pulsed [1][2]	108	65	150	30.9	75.8
CW [2]	108	65	150	30.3	75.1
CW	128	65	150	28.7	71.0
CW	130	50	88	28.8	72.7
CW	130	32	38	27.2	73.9

[1] t_p = 100 μs; δ = 10 %.

[2] Production circuit.

1.2 Features and benefits

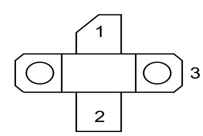
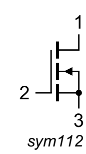
- High breakdown voltage enables class E operation up to V_{DS} = 53 V
- Qualified up to a maximum of V_{DS} = 65 V
- Characterized from 30 V to 65 V to support a wide range of applications
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness with no device degradation
- High efficiency
- Excellent thermal stability
- Designed for broadband operation
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Industrial, scientific and medical applications
  - Plasma generators
  - MRI systems
  - CO_2 lasers
  - Particle accelerators
  - Defrosting
- Broadcast
  - FM radio
  - VHF TV
- Radar
  - Non cellular communications
  - UHF radar

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
1	drain			
2	gate			
3	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT467C	ART150FEU	9349 603 45112	Tray; 20-fold; non-dry pack	60

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	[1]	-	200	V
V_{GS}	gate-source voltage		–9	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[2]	-	225	°C

[1] Specified over lifetime at maximum operating temperature.

[2] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

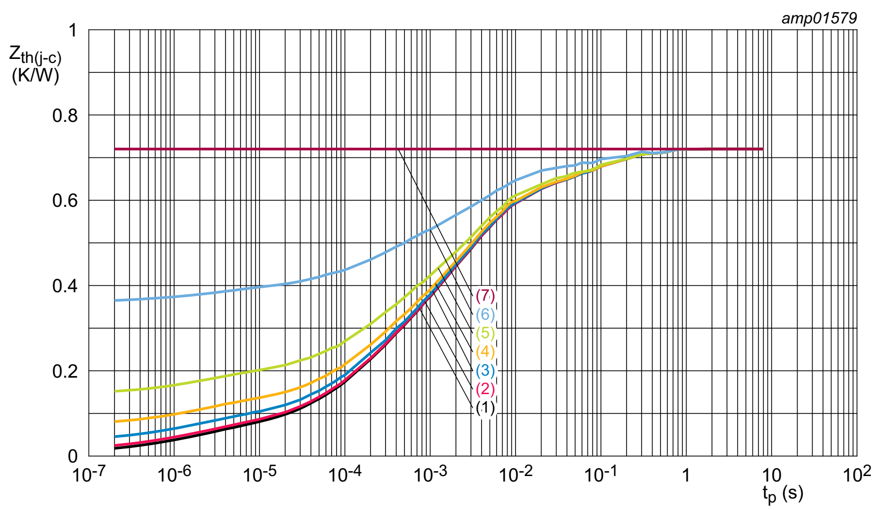
5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C; P_L = 150 W [1]	0.72	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 90 °C; t_p = 100 μs; δ = 10 %	0.21	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

[2] See Figure 1.



(1) δ = 1 %

(2) δ = 2 %

(3) δ = 5 %

(4) δ = 10 %

(5) δ = 20 %

(6) δ = 50 %

(7) δ = 100 % (DC)

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics

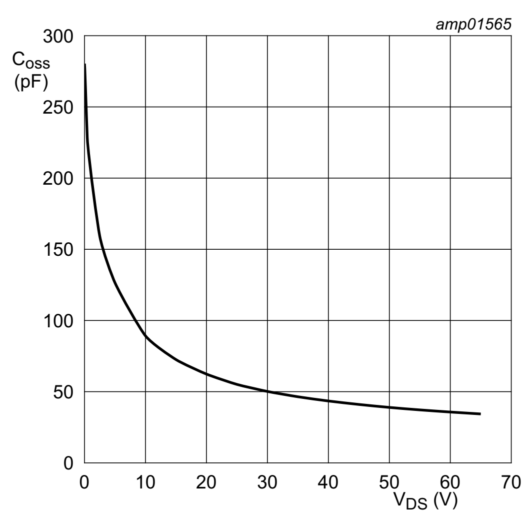
T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.11 mA	203	209	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 20 V; I_D = 111 mA	1.5	2.1	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 65 V	-	-	1.2	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 3.75 V; V_{DS} = 20 V	-	14.7	-	A
I_{GSS}	gate leakage current	V_{GS} = 13 V; V_{DS} = 0 V	-	-	120	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 3.75 V; I_D = 3.885 A	-	0.482	-	Ω

Table 7. AC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz	-	0.28	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz	-	113	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz	-	34.4	-	pF



V_{GS} = 0 V; f = 1 MHz

Fig 2. Output capacitance as a function of drain-source voltage; typical values

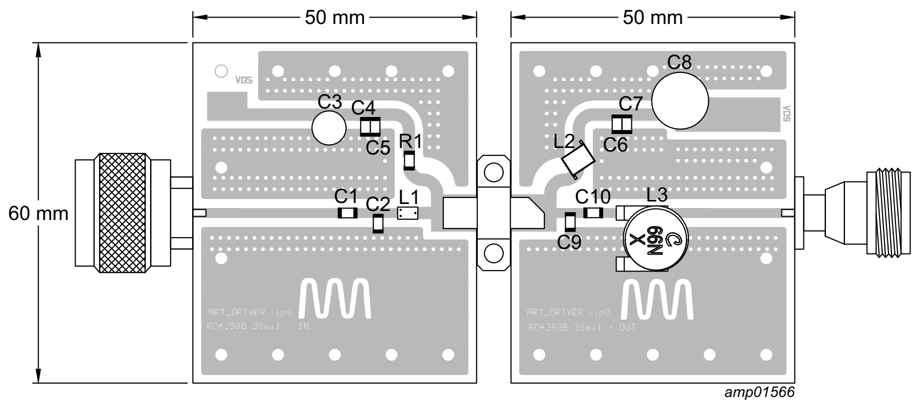
Table 8. RF characteristics

Test signal: CW pulsed; t_p = 100 μs; δ = 10 %; f = 108 MHz; RF performance at V_{DS} = 65 V; I_{Dq} = 20 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 150 W	29	31	-	dB
RL_{in}	input return loss	P_L = 150 W	-	–14	–9	dB
η_D	drain efficiency	P_L = 150 W	68	72	-	%

7. Application information

7.1 Application circuit f = 64 MHz



Printed-Circuit Board (PCB): Rogers RO4350; ε_r = 3.48 F/m; thickness = 0.762 mm.

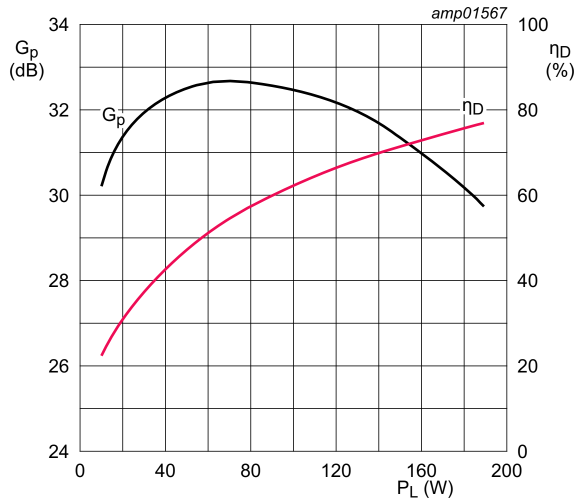
See Table 9 for a list of components.

Fig 3. Component layout

Table 9. List of components

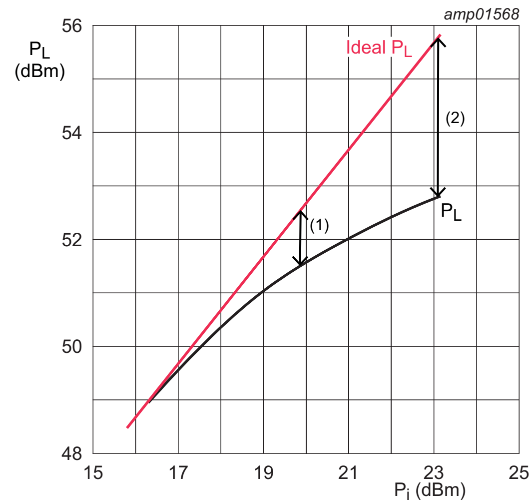
For test circuit see Figure 3.

Component	Description	Value	Remarks
C1, C5, C6	multilayer ceramic chip capacitor	100 nF, 100 V	
C2	multilayer ceramic chip capacitor	100 pF	ATC 800B
C3	electrolytic capacitor	47 μF	
C4, C7	multilayer ceramic chip capacitor	4.7 μF, 100 V	
C8	electrolytic capacitor	220 μF, 100 V	
C9	multilayer ceramic chip capacitor	39 pF	ATC 800B
C10	multilayer ceramic chip capacitor	160 pF	ATC 800B
R1	chip resistor	5.1 kΩ	SMD 1206
L1	chip inductor	120 nH	1206CS
L2	air core inductor	120 nH	1812SMS
L3	air core inductor	66 nH	1212VS-66NME



V_{DS} = 65 V; I_{Dq} = 10 mA; f = 64 MHz.

Fig 4. Power gain and drain efficiency as function of output power; typical values



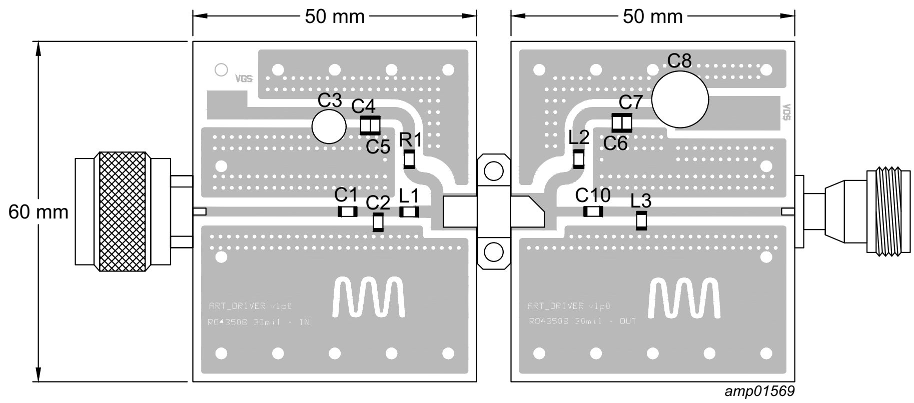
V_{DS} = 65 V; I_{Dq} = 10 mA; f = 64 MHz.

(1) $P_{L(1dB)}$ = 51.46 dBm (140 W)

(2) $P_{L(3dB)}$ = 52.81 dBm (191 W)

Fig 5. Output power as a function of input power; typical values

7.2 Application circuit f = 128 MHz



Printed-Circuit Board (PCB): Rogers RO4350; ε_r = 3.48 F/m; thickness = 0.762 mm.

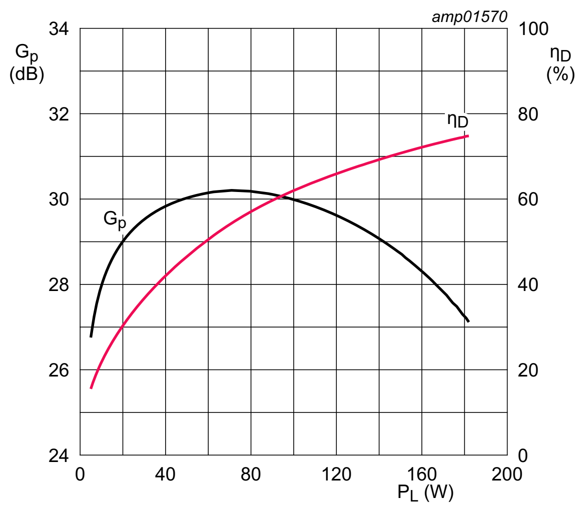
See Table 10 for a list of components.

Fig 6. Component layout

Table 10. List of components

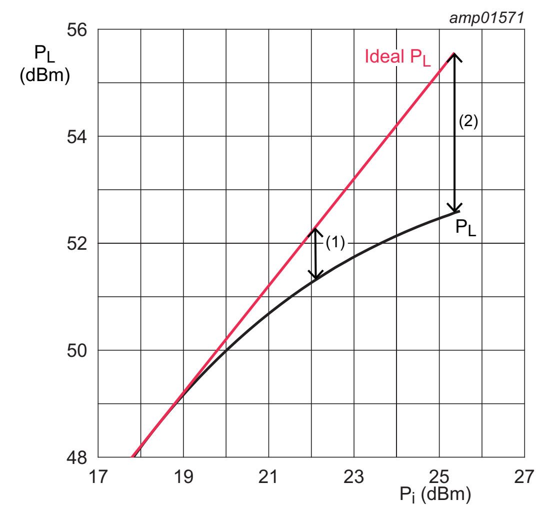
For test circuit see Figure 6.

Component	Description	Value	Remarks
C1, C5, C6	multilayer ceramic chip capacitor	100 nF, 100 V	
C2	multilayer ceramic chip capacitor	91 pF	ATC 800A
C3	electrolytic capacitor	47 μF	
C4, C7	multilayer ceramic chip capacitor	4.7 μF, 100 V	
C8	electrolytic capacitor	220 μF, 100 V	
C10	multilayer ceramic chip capacitor	68 pF	ATC 800B
R1	chip resistor	5.1 kΩ	SMD 1206
L1	chip inductor	27 nH	1206CS
L2	chip inductor	100 nH	1812SMS
L3	air core inductor	4 turns, D = 3 mm, L= 4.1 mm	0.8 mm wire



V_{DS} = 65 V; I_{Dq} = 20 mA; f = 128 MHz.

Fig 7. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 65 V; I_{Dq} = 20 mA; f = 128 MHz.

(1) $P_{L(1dB)}$ = 51.36 dBm (137 W)

(2) $P_{L(3dB)}$ = 52.57 dBm (181 W)

Fig 8. Output power as a function of input power; typical values

8. Test information

8.1 Ruggedness in class-AB operation

The ART150FE is capable of withstanding a load mismatch corresponding to VSWR = 65 ≥ 1 through all phases under the following conditions: V_{DS} = 65 V; I_{Dq} = 20 mA; P_L = 150 W; f = 108 MHz; CW and CW pulsed (t_p = 100 μs; δ = 10 %).

8.2 Impedance information

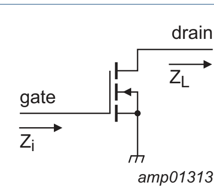


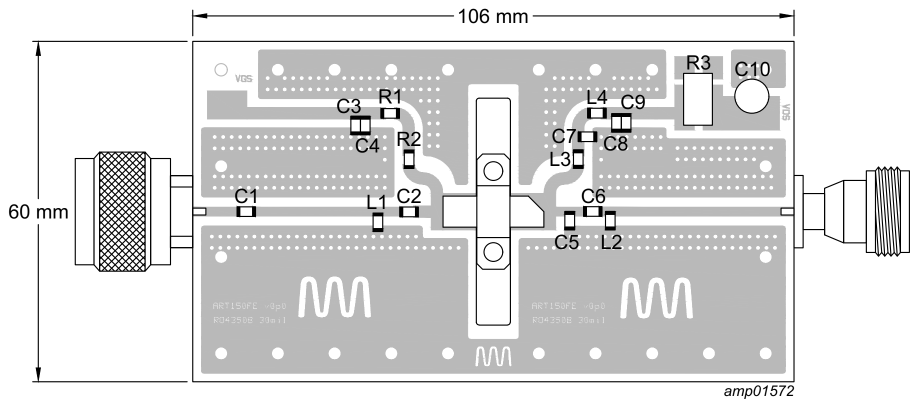
Fig 9. Definition of transistor impedance

Table 11. Typical impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 65 V and P_L = 150 W.

f	Z_i	Z_L
(MHz)	(Ω)	(Ω)
108	5.5 + j23.0	12.1 + j4.8

8.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.48 F/m; thickness = 0.762 mm.

See Table 12 for a list of components.

Fig 10. Component layout

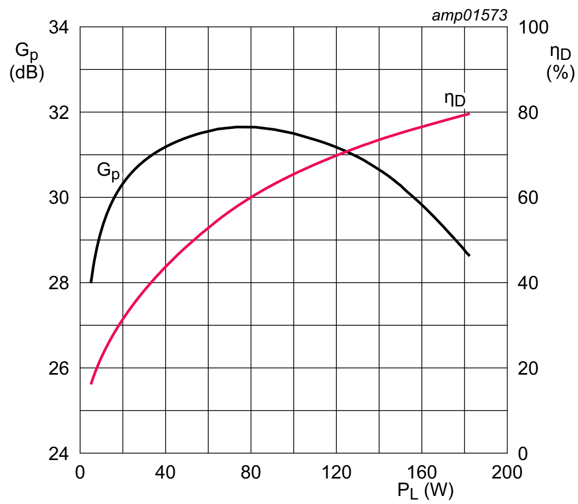
Table 12. List of components

For test circuit see Figure 10.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	1 nF	ATC 100B
C3, C9	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK: C5750X7R2A475K230KA
C4, C8	multilayer ceramic chip capacitor	100 nF, 100 V	AVX: 12061C104KAT2A
C5	multilayer ceramic chip capacitor	18 pF	ATC 100B
C6	multilayer ceramic chip capacitor	91 pF	ATC 100B
C7	multilayer ceramic chip capacitor	750 pF	ATC 100B
C10	electrolytic capacitor	470 μF, 100 V	Rybicon: 100ZLH470MEFC16X31.5
R1	chip resistor	0 Ω	SMD 1206
R2	chip resistor	5.1 kΩ	SMD 1206
R3	chip resistor	0.01 Ω	Ohmite: FC4L110R010FER
L1	chip inductor	22 nH	Coilcraft: 1206CS-220XJE
L2	air core inductor	35.5 nH	Coilcraft: B09TGLC
L3	air core inductor	82 nF	Coilcraft: 1812sms-R10GLB
L4	SM bead	Z47, 100 MHZ	Fair Rite: 2743019447

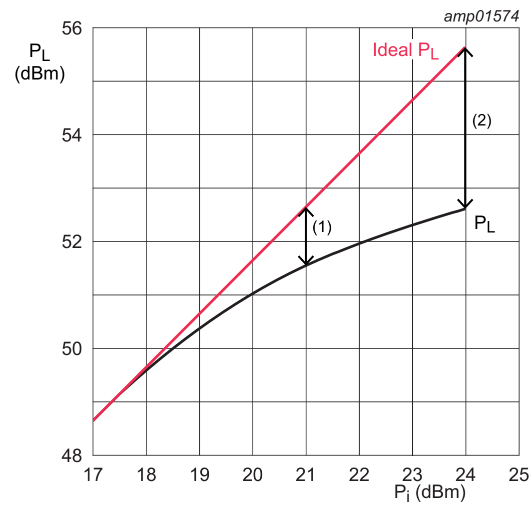
8.4 Graphical data

8.4.1 1-Tone CW



V_{DS} = 65 V; I_{Dq} = 20 mA; f = 108 MHz.

Fig 11. Power gain and drain efficiency as function of output power; typical values

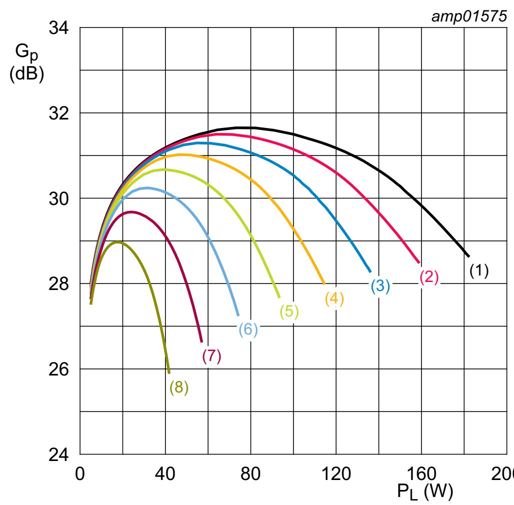


V_{DS} = 65 V; I_{Dq} = 20 mA; f = 108 MHz.

(1) $P_{L(1dB)}$ = 51.46 dBm (140 W)

(2) $P_{L(3dB)}$ = 52.60 dBm (182 W)

Fig 12. Output power as a function of input power; typical values



I_{Dq} = 20 mA; f = 108 MHz.

(1) V_{DS} = 65 V

(2) V_{DS} = 60 V

(3) V_{DS} = 55 V

(4) V_{DS} = 50 V

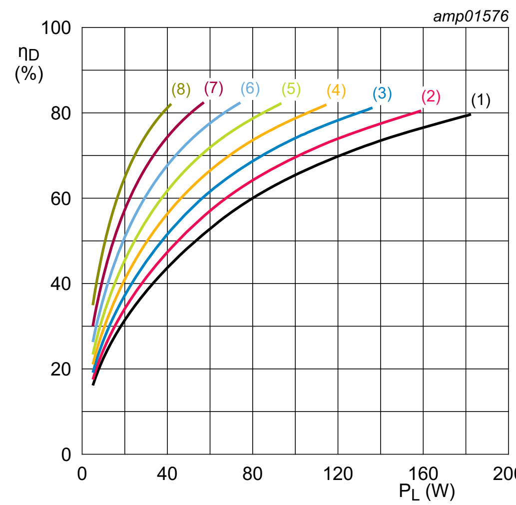
(5) V_{DS} = 45 V

(6) V_{DS} = 40 V

(7) V_{DS} = 35 V

(8) V_{DS} = 30 V

Fig 13. Power gain as a function of output power; typical values



I_{Dq} = 20 mA; f = 108 MHz.

(1) V_{DS} = 65 V

(2) V_{DS} = 60 V

(3) V_{DS} = 55 V

(4) V_{DS} = 50 V

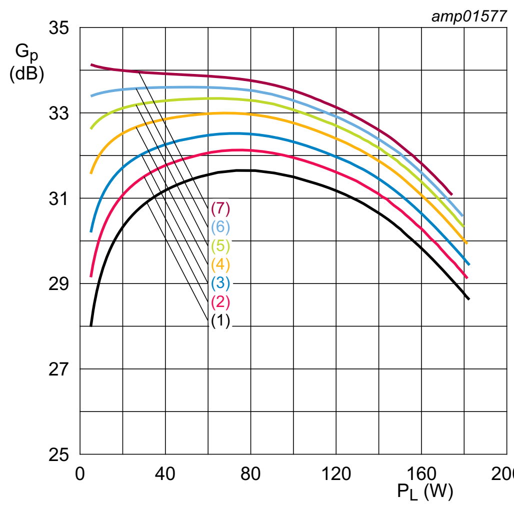
(5) V_{DS} = 45 V

(6) V_{DS} = 40 V

(7) V_{DS} = 35 V

(8) V_{DS} = 30 V

Fig 14. Drain efficiency as a function of output power; typical values



V_{DS} = 65 V; f = 108 MHz.

(1) I_{Dq} = 20 mA

(2) I_{Dq} = 50 mA

(3) I_{Dq} = 100 mA

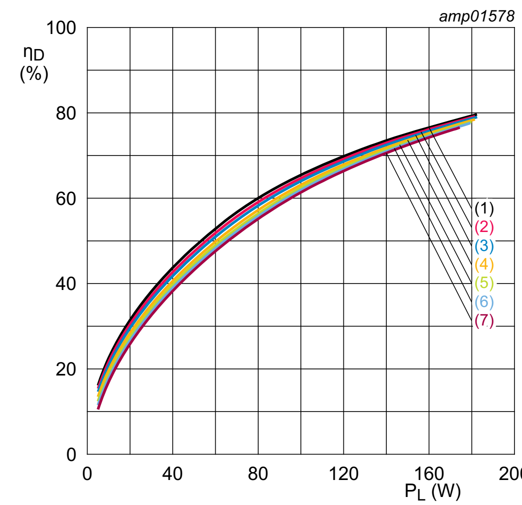
(4) I_{Dq} = 200 mA

(5) I_{Dq} = 300 mA

(6) I_{Dq} = 400 mA

(7) I_{Dq} = 500 mA

Fig 15. Power gain as a function of output power; typical values



V_{DS} = 65 V; f = 108 MHz.

(1) I_{Dq} = 20 mA

(2) I_{Dq} = 50 mA

(3) I_{Dq} = 100 mA

(4) I_{Dq} = 200 mA

(5) I_{Dq} = 300 mA

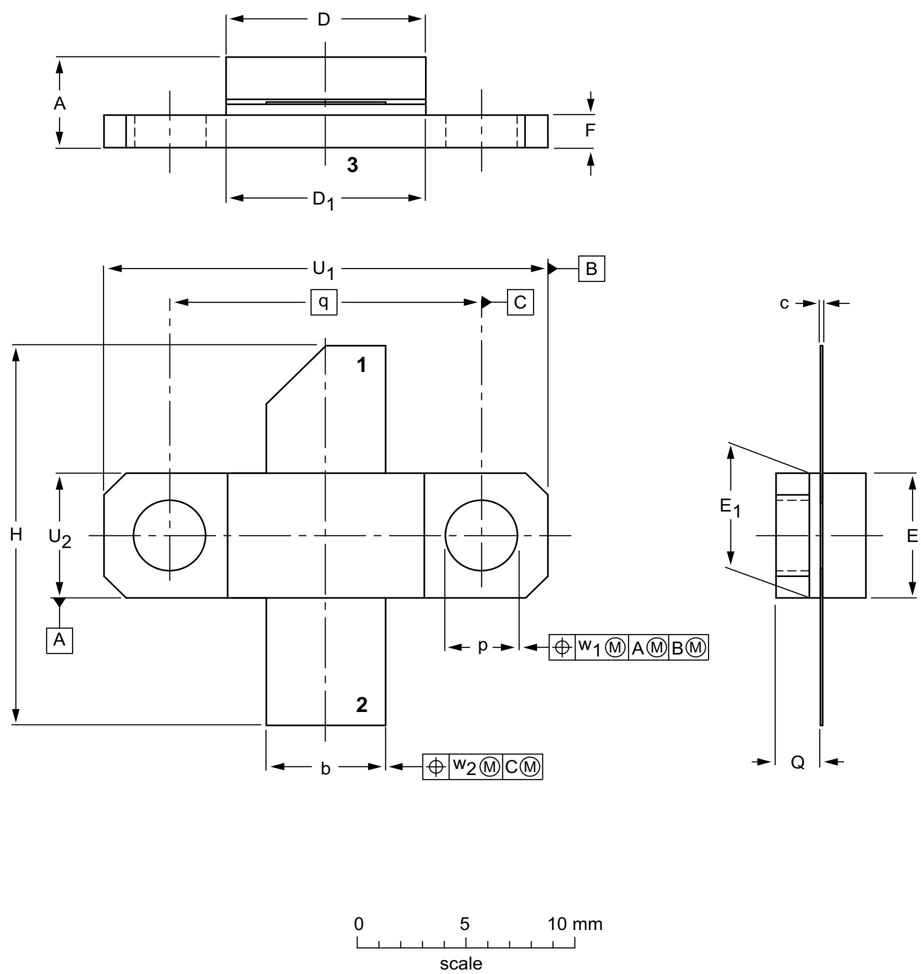
(6) I_{Dq} = 400 mA

(7) I_{Dq} = 500 mA

Fig 16. Drain efficiency as a function of output power; typical values

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT467C**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						~~99-12-28~~ 12-05-02

Fig 17. Package outline SOT467C

10. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 13. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

11. Abbreviations

Table 14. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
FM	Frequency Modulation
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MRI	Magnetic Resonance Imaging
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
UHF	Ultra High Frequency
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio

12. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ART150FE v.2	20220708	Product data sheet	-	ART150FE v.1
Modifications:	• Section 1.2 on page 1: first list item, changed value drain-source voltage • Table 4 on page 2: changed values gate-source voltage • Table 6 on page 4: changed value gate-source voltage • Section 13.2 on page 15: updated section • Section 13.3 on page 15: updated section			
ART150FE v.1	20210104	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

13.2 Definitions

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Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not guaranteed. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

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