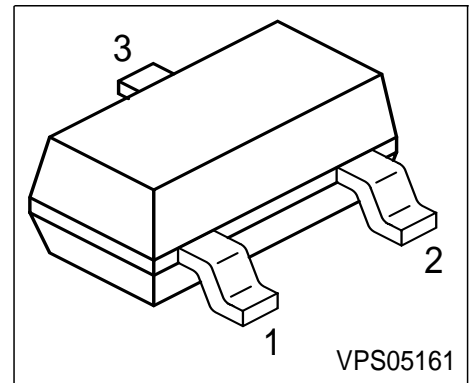
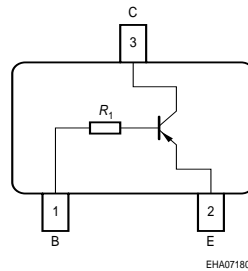


**PNP Silizium Digital Transistor**

- Switching circuit, inverter, interface circuit, driver circuit
- Built in bias resistor ( $R_1 = 4.7k\Omega$ )



Type	Marking	Pin Configuration			Package
BCR569	XLs	1 = B	2 = E	3 = C	SOT23

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Collector-emitter voltage	$V_{CEO}$	50	V
Collector-base voltage	$V_{CBO}$	50	
Emitter-base voltage	$V_{EBO}$	5	
Input on Voltage	$V_{i(on)}$	30	
DC collector current	$I_C$	500	mA
Total power dissipation, $T_S = 79\text{ °C}$	$P_{tot}$	330	mW
Junction temperature	$T_j$	150	°C
Storage temperature	$T_{stg}$	-65 ... 150	

**Thermal Resistance**

Junction - soldering point <sup>1)</sup>	$R_{thJS}$	≤ 215	K/W
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<sup>1</sup>For calculation of  $R_{thJA}$  please refer to Application Note Thermal Resistance

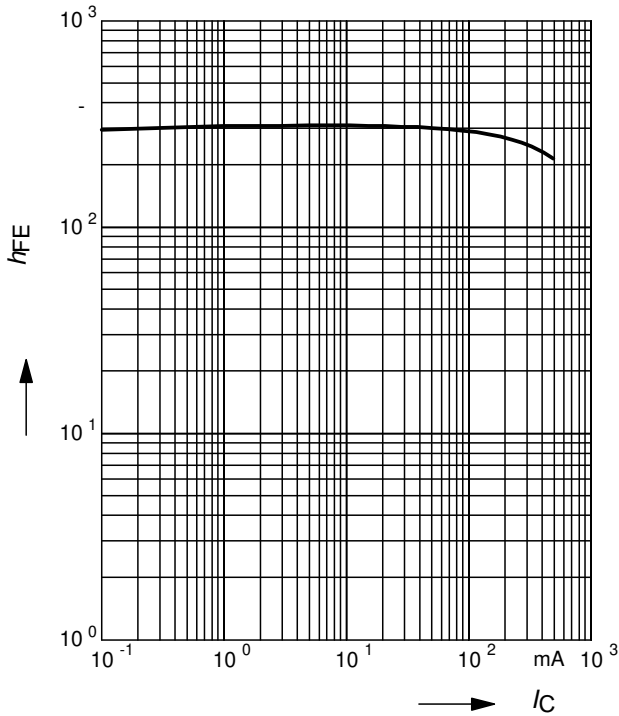
**Electrical Characteristics** at  $T_A=25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>DC Characteristics</b>					
Collector-emitter breakdown voltage $I_C = 100 \mu\text{A}, I_B = 0$	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10 \mu\text{A}, I_B = 0$	$V_{(BR)CBO}$	50	-	-	
Emitter-base breakdown voltage $I_E = 10 \mu\text{A}, I_C = 0$	$V_{(BR)EBO}$	5	-	-	V
Collector cutoff current $V_{CB} = 40 \text{ V}, I_E = 0$	$I_{CBO}$	-	-	100	nA
DC current gain 1) $I_C = 50 \text{ mA}, V_{CE} = 5 \text{ V}$	$h_{FE}$	120	-	630	-
Collector-emitter saturation voltage1) $I_C = 50 \text{ mA}, I_B = 2.5 \text{ mA}$	$V_{CEsat}$	-	-	0.3	V
Input off voltage $I_C = 100 \mu\text{A}, V_{CE} = 5 \text{ V}$	$V_{i(off)}$	0.4	-	0.8	V
Input on Voltage $I_C = 10 \text{ mA}, V_{CE} = 0.3 \text{ V}$	$V_{i(on)}$	0.5	-	1.5	
Input resistor	$R_1$	3.2	4.7	6.2	k $\Omega$
<b>AC Characteristics</b>					
Transition frequency $I_C = 50 \text{ mA}, V_{CE} = 5 \text{ V}, f = 100 \text{ MHz}$	$f_T$	-	150	-	MHz

 1) Pulse test:  $t < 300\mu\text{s}$ ;  $D < 2\%$

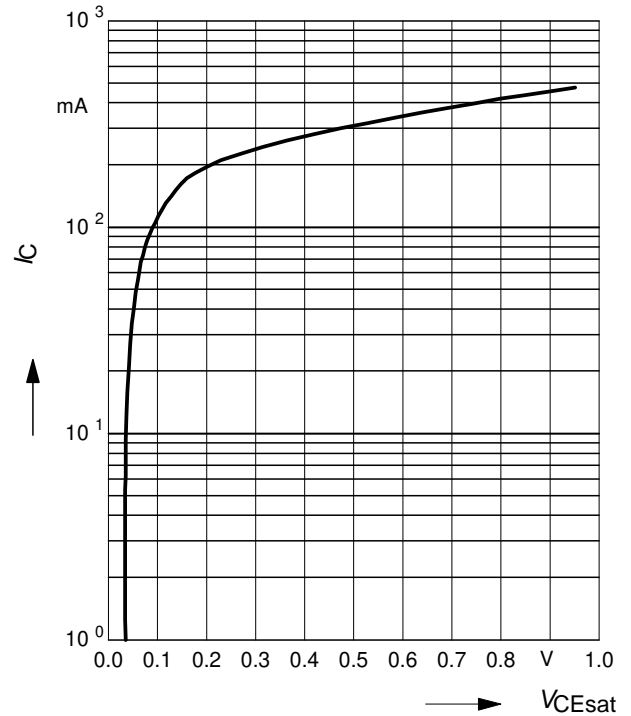
**DC Current Gain  $h_{FE} = f(I_C)$**

$V_{CE} = 5V$  (common emitter configuration)



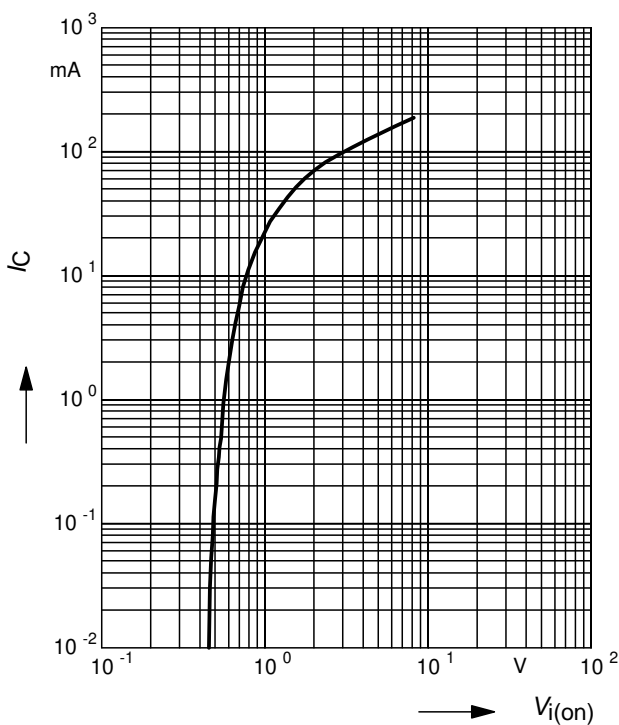
**Collector-Emitter Saturation Voltage  $V_{CEsat} = f(I_C), h_{FE} = 20$**

$V_{CEsat} = f(I_C), h_{FE} = 20$



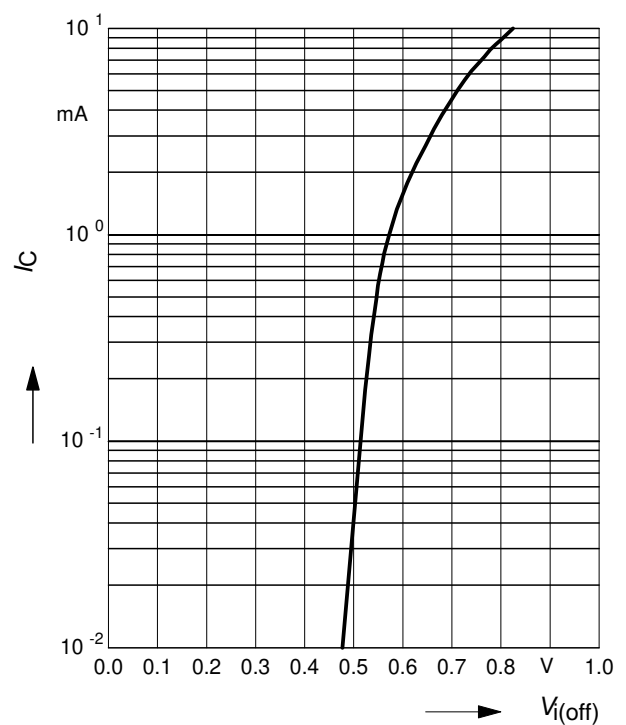
**Input on Voltage  $V_{i(on)} = f(I_C)$**

$V_{CE} = 0.3V$  (common emitter configuration)

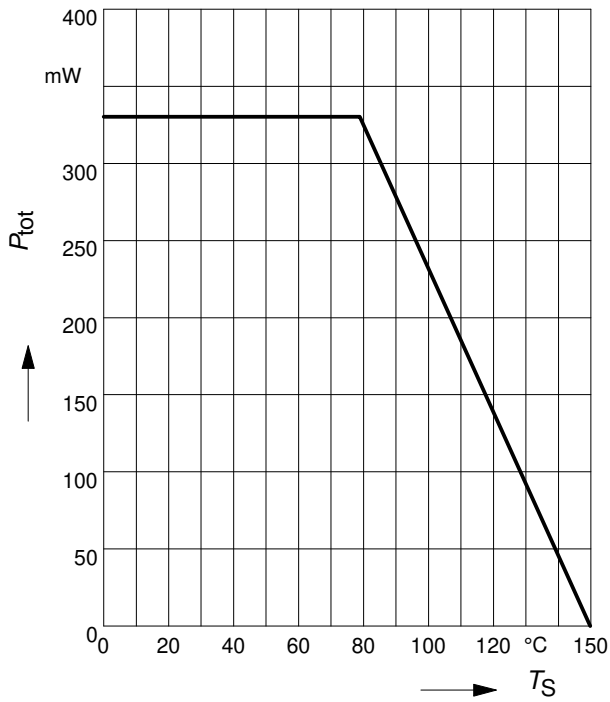


**Input off voltage  $V_{i(off)} = f(I_C)$**

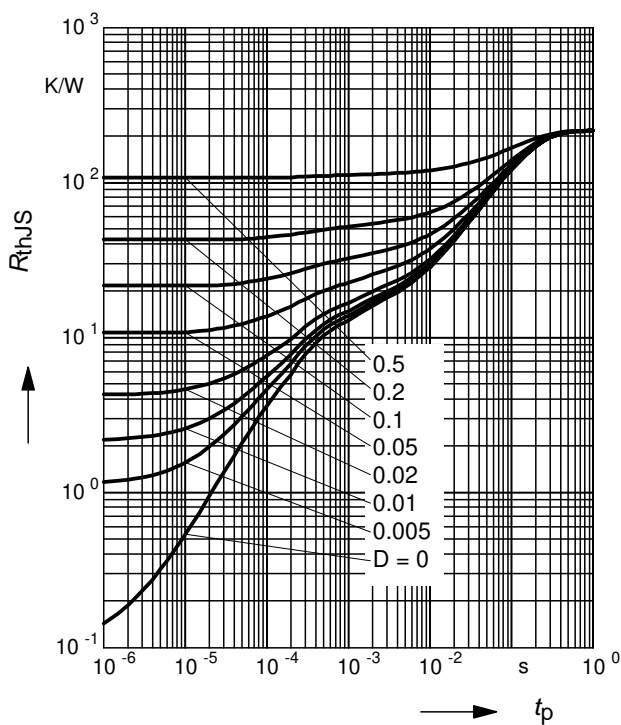
$V_{CE} = 5V$  (common emitter configuration)



**Total power dissipation  $P_{tot} = f(T_S)$**



**Permissible Pulse Load  $R_{thJS} = f(t_p)$**



**Permissible Pulse Load**

$P_{totmax} / P_{totDC} = f(t_p)$

