

**PI6C20400A**

**1:4 Clock Driver for Intel PCIe® Chipsets**

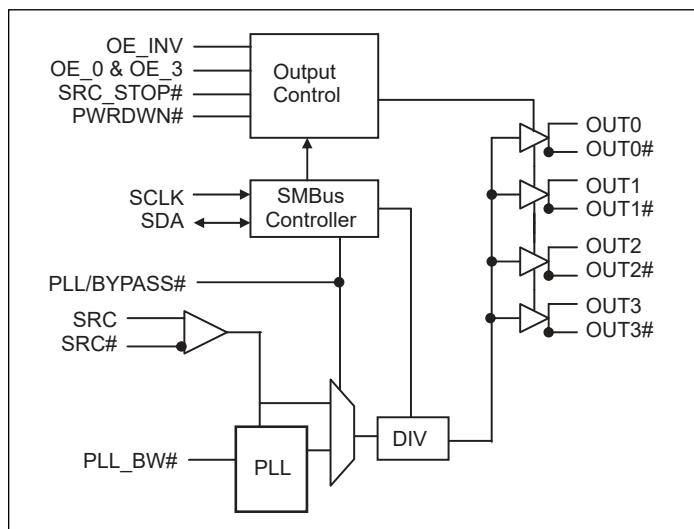
**Features**

- Phase jitter filter for PCIe® 2.0 application
- Four Pairs of Differential Clocks
- Low skew < 50ps
- Low jitter < 50ps cycle-to-cycle
- < 1 ps additive RMS phase jitter
- Output Enable for all outputs
- Outputs tristate control via SMBus
- Programmable PLL Bandwidth
- 100 MHz PLL Mode operation
- 100 - 400 MHz Bypass Mode operation
- 3.3V Operation
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.  
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free and Green):
  - 28-Pin SSOP (H28)
  - 28-Pin TSSOP (L28)

**Description**

The PI6C20400A is a PCIe® 2.0 compliant high-speed, low-noise differential clock buffer designed to be companion to PI6C410BS. The device distributes the differential SRC clock from PI6C410BS to four differential pairs of clock outputs either with or without PLL. The clock outputs are controlled by input selection of SRC\_STOP#, PWRDWN# and SMBus, SCLK and SDA. When input of either SRC\_STOP# or PWRDWN# is low, the output clocks are Tristated. When PWRDWN# is low, the SDA and SCLK inputs must be Tri-stated.

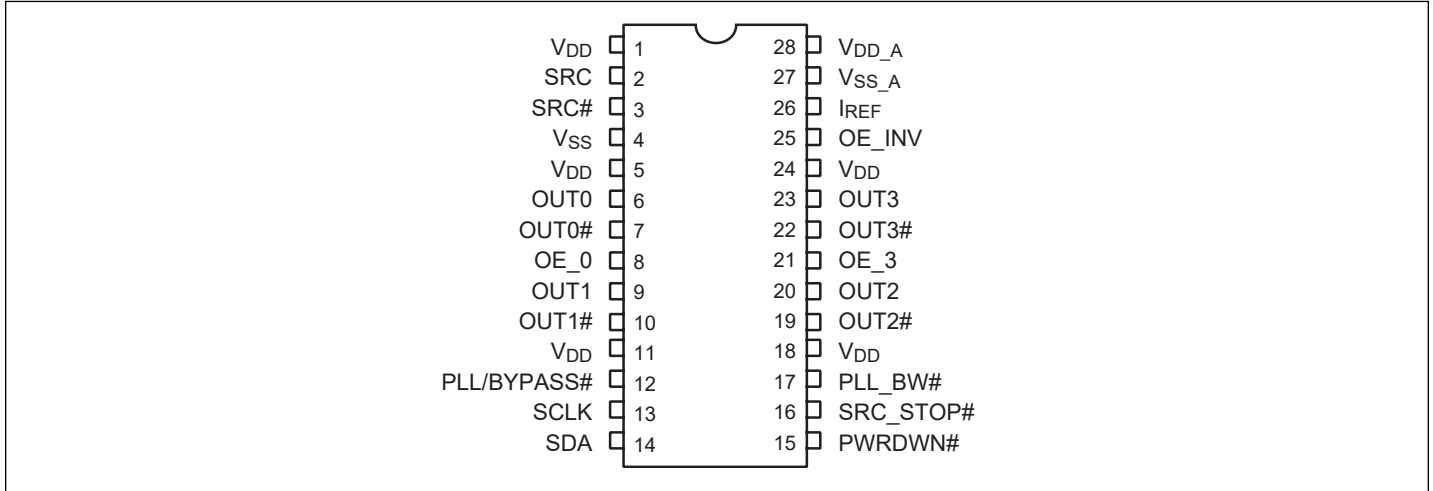
**Block Diagram**



**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
3. Halogen- and Antimony-free “Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Configuration



## Pin Descriptions

| Pin#                        | Pin Name             | Type   | Description   |
|-----------------------------|----------------------|--------|---|
| 2, 3                        | SRC, SRC#            | Input  | 0.7V Differential SRC input from PI6C410 clock synthesizer  |
| 8, 21                       | OE_0, OE_3           | Input  | 3.3V LVTTTL input for enabling outputs, active high.<br>OE_0 for OUT0 / OUT0#<br>OE_3 for OUT3 / OUT3#  |
| 25                          | OE_INV               | Input  | 3.3V LVTTTL input for inverting the OE, SRC_STOP# and PWRDWN# pins.<br>When 0 = same stage<br>When 1 = OE_0, OE_3, SRC_STOP#, PWRDWN# inverted. |
| 6, 7, 9, 10, 19, 20, 22, 23 | OUT[0:3] & OUT[0:3]# | Output | 0.7V Differential outputs   |
| 12                          | PLL/BYPASS#          | Input  | 3.3V LVTTTL input for selecting fan-out of PLL operation.   |
| 13                          | SCLK                 | Input  | SMBus compatible SCLOCK input   |
| 14                          | SDA                  | I/O    | SMBus compatible SDATA  |
| 26                          | IREF                 | Input  | External resistor connection to set the differential output current   |
| 16                          | SRC_STOP#            | Input  | 3.3V LVTTTL input for SRC stop, active low  |
| 17                          | PLL_BW#              | Input  | 3.3V LVTTTL input for selecting the PLL bandwidth   |
| 15                          | PWRDWN#              | Input  | 3.3V LVTTTL input for Power Down operation, active low  |
| 1, 5, 11, 18, 24            | V <sub>DD</sub>      | Power  | 3.3V Power Supply for Outputs   |
| 4                           | V <sub>SS</sub>      | Ground | Ground for Outputs  |
| 27                          | V <sub>SS_A</sub>    | Ground | Ground for PLL  |
| 28                          | V <sub>DD_A</sub>    | Power  | 3.3V Power Supply for PLL   |

## Serial Data Interface (SMBus)

This part is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

### Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | W/R |
|----|----|----|----|----|----|----|-----|
| 1  | 1  | 0  | 1  | 1  | 1  | 0  | 0/1 |

### Data Protocol

|           |            |     |     |                 |     |                |     |             |     |     |                 |     |          |
|-----------|------------|-----|-----|-----------------|-----|----------------|-----|-------------|-----|-----|-----------------|-----|----------|
| 1 bit     | 7 bits     | 1   | 1   | 8 bits          | 1   | 8 bits         | 1   | 8 bits      | 1   |     | 8 bits          | 1   | 1 bit    |
| Start bit | Slave Addr | R/W | Ack | Register offset | Ack | Byte Count = N | Ack | Data Byte 0 | Ack | ... | Data Byte N - 1 | Ack | Stop bit |

**Notes:**

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

### Data Byte 0: Control Register

| Bit | Descriptions  | Type | Power Up Condition      | Output(s) Affected  | Source Pin |
|-----|---|------|-------------------------|---------------------|------------|
| 0   | Outputs Mode<br>0 = Divide by 2<br>1 = Normal             | RW   | 1 = Normal              | OUT[0:3], OUT[0:3]# | NA         |
| 1   | PLL/BYPASS#<br>0 = Fanout<br>1 = PLL                      | RW   | 1 = PLL                 | OUT[0:3], OUT[0:3]# | NA         |
| 2   | PLL Bandwidth<br>0 = High Bandwidth,<br>1 = Low Bandwidth | RW   | 1 = Low                 | OUT[0:3], OUT[0:3]# | NA         |
| 3   | Reserved  |      |                         |                     | NA         |
| 4   | Reserved  |      |                         |                     | NA         |
| 5   | Reserved  |      |                         |                     | NA         |
| 6   | SRC_STOP#<br>0 = Driven when stopped<br>1 = Tristate      | RW   | 0 = Driven when stopped | OUT[0:3], OUT[0:3]# | NA         |
| 7   | PWRDWN#<br>0 = Driven when stopped<br>1 = Tristate        | RW   | 0 = Driven when stopped | OUT[0:3], OUT[0:3]# | NA         |

**Data Byte 1: Control Register**

| Bit | Descriptions                | Type | Power Up Condition | Output(s) Affected | Source Pin |
|-----|-----------------------------|------|--------------------|--------------------|------------|
| 0   | Reserved                    |      |                    |                    | NA         |
| 1   | OUTPUTS enable              | RW   | 1 = Enabled        | OUT0, OUT0#        | NA         |
| 2   | 1 = Enabled<br>0 = Disabled | RW   | 1 = Enabled        | OUT1, OUT1#        | NA         |
| 3   | Reserved                    |      |                    |                    | NA         |
| 4   | Reserved                    |      |                    |                    | NA         |
| 5   | OUTPUTS enable              | RW   | 1 = Enabled        | OUT2, OUT2#        | NA         |
| 6   | 1 = Enabled<br>0 = Disabled | RW   | 1 = Enabled        | OUT3, OUT3#        | NA         |
| 7   | Reserved                    |      |                    |                    | NA         |

**Data Byte 2: Control Register**

| Bit | Descriptions  | Type | Power Up Condition | Output(s) Affected | Source Pin |
|-----|---|------|--------------------|--------------------|------------|
| 0   | Reserved  |      |                    |                    | NA         |
| 1   | Allow control of OUTPUTS with<br>assertion of SRC_STOP# | RW   | 0 = Free running   | OUT0, OUT0#        | NA         |
| 2   | 0 = Free running<br>1 = Stopped with SRC_Stop#          | RW   | 0 = Free running   | OUT1, OUT1#        | NA         |
| 3   | Reserved  |      |                    |                    | NA         |
| 4   | Reserved  |      |                    |                    | NA         |
| 5   | Allow control of OUTPUTS with<br>assertion of SRC_STOP# | RW   | 0 = Free running   | OUT2, OUT2#        | NA         |
| 6   | 0 = Free running<br>1 = Stopped with SRC_Stop#          | RW   | 0 = Free running   | OUT3, OUT3#        | NA         |
| 7   | Reserved  |      |                    |                    | NA         |

**Data Byte 3: Control Register**

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|-----|--------------|------|--------------------|--------------------|------------|
| 0   | Reserved     | RW   |                    |                    |            |
| 1   |              | RW   |                    |                    |            |
| 2   |              | RW   |                    |                    |            |
| 3   |              | RW   |                    |                    |            |
| 4   |              | RW   |                    |                    |            |
| 5   |              | RW   |                    |                    |            |
| 6   |              | RW   |                    |                    |            |
| 7   |              | RW   |                    |                    |            |

**Data Byte 4: Pericom ID Register**

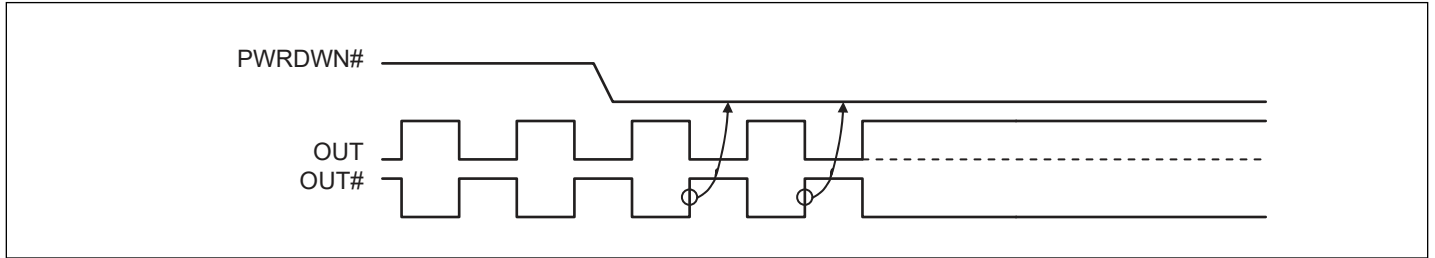
| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Pin |
|-----|--------------|------|--------------------|--------------------|-----|
| 0   | Pericom ID   | R    | 0                  | NA                 | NA  |
| 1   |              | R    | 0                  | NA                 | NA  |
| 2   |              | R    | 0                  | NA                 | NA  |
| 3   |              | R    | 0                  | NA                 | NA  |
| 4   |              | R    | 0                  | NA                 | NA  |
| 5   |              | R    | 1                  | NA                 | NA  |
| 6   |              | R    | 0                  | NA                 | NA  |
| 7   |              | R    | 0                  | NA                 | NA  |

**PI6C20400A**

**Functionality**

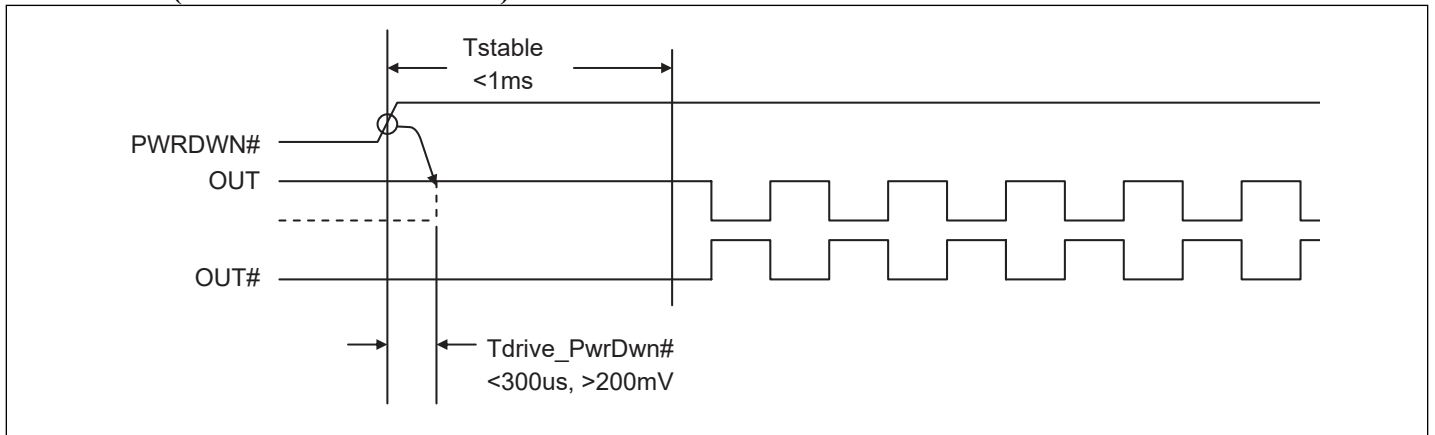
| PWRDWN# | OUT                         | OUT#   | SRC_Stop# | OUT                         | OUT#   |
|---------|-----------------------------|--------|-----------|-----------------------------|--------|
| 1       | Normal                      | Normal | 1         | Normal                      | Normal |
| 0       | $I_{REF} \times 2$ or Float | Low    | 0         | $I_{REF} \times 6$ or Float | Low    |

**Power Down (PWRDWN# assertion)**



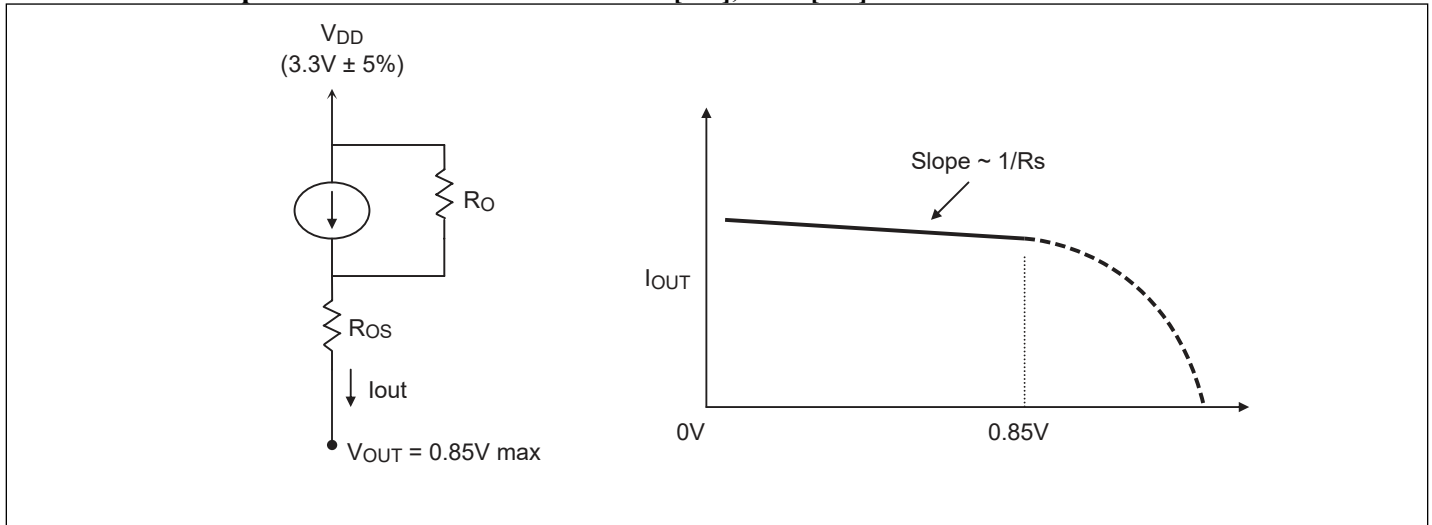
**Figure 1. Power Down Sequence**

**Power Down (PWRDWN# De-assertion)**



**Figure 2. Power Down De-assert Sequence**

**Current-mode Output Buffer Characteristics of OUT[0:3], OUT[0:3]#**



**Figure 3. Simplified Diagram of Current-mode Output Buffer**

**Differential Clock Buffer Characteristics**

| Symbol    | Minimum       | Maximum     |
|-----------|---------------|-------------|
| $R_O$     | 3000 $\Omega$ | N/A         |
| $R_{OS}$  | unspecified   | unspecified |
| $V_{OUT}$ | N/A           | 850mV       |

**Current Accuracy**

| Symbol    | Conditions              | Configuration   | Load                                      | Min.               | Max.               |
|-----------|-------------------------|---|---|--------------------|--------------------|
| $I_{OUT}$ | $V_{DD} = 3.30 \pm 5\%$ | $R_{REF} = 475\Omega \text{ 1\%}$<br>$I_{REF} = 2.32mA$ | Nominal test load for given configuration | -12% $I_{NOMINAL}$ | +12% $I_{NOMINAL}$ |

**Note:**

1.  $I_{NOMINAL}$  refers to the expected current based on the configuration of the device.

**Differential Clock Output Current**

| Board Target Trace/Term Z  | Reference R, $I_{ref} = V_{DD}/(3xRr)$                    | Output Current              | $V_{OH} @ Z$ |
|--|---|-----------------------------|--------------|
| 100 $\Omega$<br>(100 $\Omega$ differential $\approx$ 15% coupling ratio) | $R_{REF} = 475\Omega \text{ 1\%}$ ,<br>$I_{REF} = 2.32mA$ | $I_{OH} = 6 \times I_{REF}$ | 0.7V @ 50    |

## Absolute Maximum Ratings

(Over operating free-air temperature range)

| Symbol            | Parameters               | Min. | Max. | Units |
|-------------------|--------------------------|------|------|-------|
| V <sub>DD_A</sub> | 3.3V Core Supply Voltage | -0.5 | 4.6  | V     |
| V <sub>DD</sub>   | 3.3V I/O Supply Voltage  | -0.5 | 4.6  |       |
| V <sub>IH</sub>   | Input High Voltage       |      | 4.6  |       |
| V <sub>IL</sub>   | Input Low Voltage        | -0.5 |      |       |
| T <sub>s</sub>    | Storage Temperature      | -65  | 150  | °C    |
| V <sub>ESD</sub>  | ESD Protection           | 2000 |      | V     |
| T <sub>j</sub>    | Junction Temperature     |      | 125  | °C    |

**Note:**

1. Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

## DC Electrical Characteristics (V<sub>DD</sub> = 3.3±5%, V<sub>DD\_A</sub> = 3.3±5%)

| Symbol                  | Parameters                        | Condition   | Min.                  | Max.                  | Units |
|-------------------------|-----------------------------------|---|-----------------------|-----------------------|-------|
| V <sub>DD_A</sub>       | 3.3V Core Supply Voltage          |   | 3.135                 | 3.465                 | V     |
| V <sub>DD</sub>         | 3.3V I/O Supply Voltage           |   | 3.135                 | 3.465                 |       |
| V <sub>IH</sub>         | 3.3V Input High Voltage           | V <sub>DD</sub>   | 2.0                   | V <sub>DD</sub> + 0.3 |       |
| V <sub>IL</sub>         | 3.3V Input Low Voltage            |   | V <sub>SS</sub> - 0.3 | 0.8                   |       |
| I <sub>IL</sub>         | Input Leakage Current             | 0 < V <sub>IN</sub> < V <sub>DD</sub>                               | -5                    | +5                    | μA    |
| V <sub>OH</sub>         | 3.3V Output High Voltage          | I <sub>OH</sub> = -1mA  | 2.4                   |                       | V     |
| V <sub>OL</sub>         | 3.3V Output Low Voltage           | I <sub>OL</sub> = 1mA   |                       | 0.4                   |       |
| I <sub>OH</sub>         | Output High Current               | I <sub>OH</sub> = 6 x I <sub>REF</sub><br>I <sub>REF</sub> = 2.32mA | 12.2                  | 15.6                  | mA    |
| C <sub>IN</sub>         | Input Pin Capacitance             |   | 2                     | 5                     |       |
| C <sub>OUT</sub>        | Output Pin Capacitance            |   |                       | 6                     | pF    |
| L <sub>PIN</sub>        | Pin Inductance                    |   |                       | 7                     |       |
| I <sub>DD(BYPASS)</sub> | Power Supply Current (PLL Bypass) | V <sub>DD</sub> = 3.465V, F <sub>CPU</sub> = 100MHz                 |                       | 90                    | mA    |
| I <sub>DD</sub>         | Power Supply Current              | V <sub>DD</sub> = 3.465V  | Bypass mode           | 100                   |       |
|                         |                                   | F <sub>CPU</sub> = 100MHz   | PLL mode              | 130                   |       |
| I <sub>SS</sub>         | Power Down Current                | Driven outputs  |                       | 40                    |       |
| I <sub>SS</sub>         | Power Down Current                | Tristate outputs  |                       | 12                    |       |
| T <sub>A</sub>          | Ambient Temperature               |   | -40                   | 85                    | °C    |



### HCSSL Input (SRC, SRC#) Characteristics<sup>(1)</sup>

Temperature = T<sub>A</sub>; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol                      | Parameters                           | Conditions  | Min. | Typ. | Max. | Units |
|-----------------------------|--------------------------------------|---|------|------|------|-------|
| V <sub>COM</sub>            | Diff. Input Common Mode Voltage      |   | 150  |      | 900  | mV    |
| V <sub>SWING</sub>          | Diff. Input Swing Voltage            | Peak to peak value (V <sub>IHDIF</sub> - V <sub>ILDIF</sub> )         | 300  |      | 1000 | mV    |
| f <sub>INBP</sub>           | Input Frequency                      | PLL Bypass mode   | 100  |      | 400  | MHz   |
| f <sub>IN100</sub>          | Input Frequency                      | PLL mode  | 95   | 100  | 105  | MHz   |
| f <sub>MODI-PCIe</sub>      | Input SS Modulation Freq. PCIe       | Allowable frequency for PCIe applications (Triangular Modulation)     | 30   |      | 33   | kHz   |
| f <sub>MODIN-non-PCIe</sub> | Input SS Modulation Freq. non-PCIe   | Allowable frequency for non-PCIe applications (Triangular Modulation) | 0    |      | 46   | kHz   |
| t <sub>RF</sub>             | Diff. Input Slew Rate <sup>(2)</sup> | Measured differentially   | 0.4  |      |      | V/ns  |
| I <sub>IN</sub>             | Diff. Input Leakage Current          | V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND             | -5   | 0.01 | 5    | uA    |
| t <sub>DC</sub>             | Diff. Input Duty Cycle               | Measured differentially   | 45   |      | 55   | %     |
| t <sub>j-c-c</sub>          | Diff. Input Cycle to cycle jitter    | Measured differentially   |      |      | 125  | ps    |

**Note:**

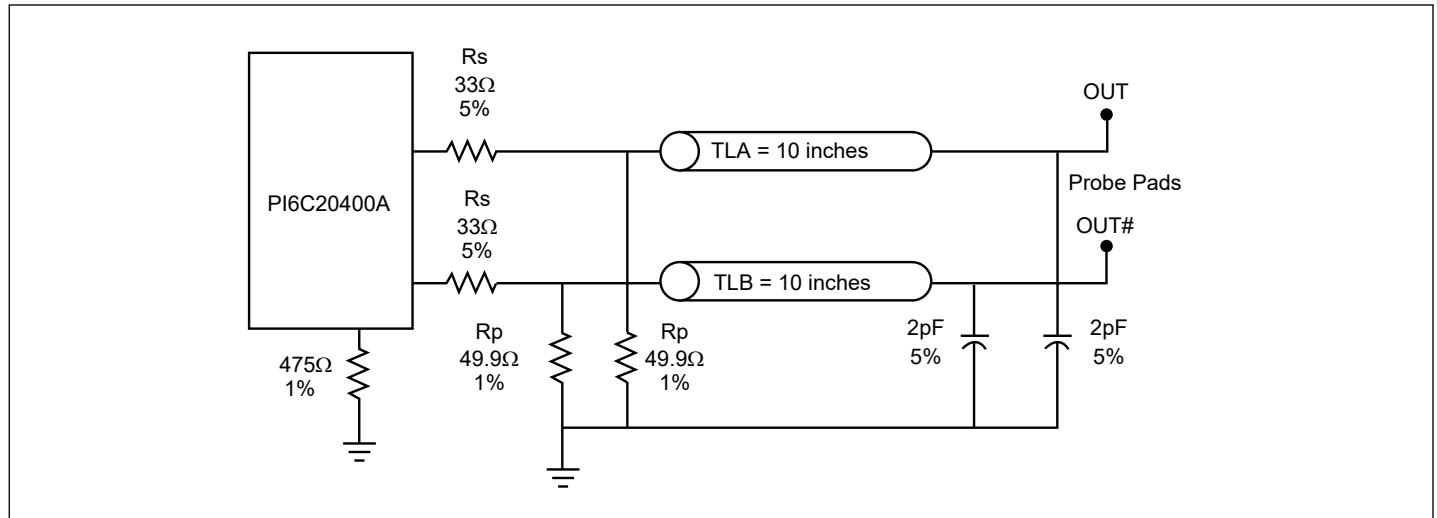
1. Guaranteed by design and characterization, not 100% tested in production
2. Slew rate measured through +/-75mV window centered around differential zero

**HCSL Output AC Switching Characteristics** ( $V_{DD} = 3.3 \pm 5\%$ ,  $V_{DDA} = 3.3 \pm 5\%$ )

| Symbol                  | Parameters                       | Condition                         | Min. | Max.      | Units | Notes |
|-------------------------|----------------------------------|-----------------------------------|------|-----------|-------|-------|
| $T_{rise} / T_{fall}$   | Rise and Fall Time               | Measured between 0.175V to 0.525V | 175  | 700       | ps    | 2     |
| $DT_{rise} / DT_{fall}$ | Rise and Fall Time Variation     |                                   |      | 125       | ps    | 2     |
| $T_{pd}$                | Propogation delay                | PLL Mode                          |      | $\pm 250$ | ps    | 6     |
|                         |                                  | Bypass Mode                       | 2.5  | 6.5       | ns    |       |
| $T_{jitter}$            | Cycle - Cycle Jitter             | OUT[0:3] & OUT[0:3]#              |      | 50        | ps    | 3, 4  |
| $V_{HIGH}$              | Voltage High including overshoot | OUT[0:3] & OUT[0:3]#              | 660  | 1150      | mV    | 2     |
| $V_{LOW}$               | Voltage Low including undershoot | OUT[0:3] & OUT[0:3]#              | -300 |           | mV    | 2     |
| $V_{cross}$             | Absolute crossing point voltages | OUT[0:3] & OUT[0:3]#              | 250  | 550       | mV    | 2     |
| $DV_{cross}$            | Total Variation of $V_{cross}$   | Over all edges                    |      | 140       | mV    | 2     |
| $T_{DC}$                | Duty Cycle                       | OUT[0:3] & OUT[0:3]#              | 45   | 55        | %     | 3     |
| $T_{jadd}$              | Additive RMS phase jitter        | For PCIe 2.0                      | <0   | 1         | ps    | 5     |

**Notes:**

1. Test configuration is  $R_s = 33.2\Omega$ ,  $R_p = 49.9\Omega$ , and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. Measurement taken using M1 data capture analysis tool.
5. Additive jitter is calculated from input and output RMS phase jitter by using PCIe 2.0 filter. ( $T_{jadd} = \sqrt{(\text{output jitter})^2 - (\text{input jitter})^2}$ )
6. Using the test configuration and data is taken at the probe pads

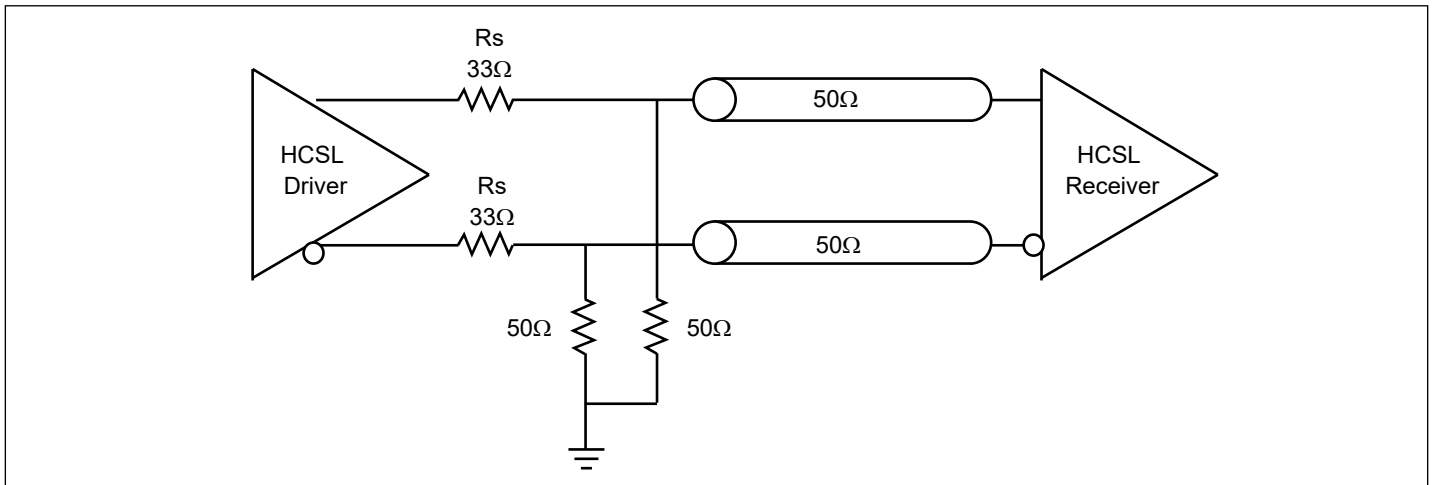


**Figure 4. Test Configuration**

## Application Information

### Termination for DC-Coupled Differential Operation

For DC-coupled operation of an HCSL driver, terminate with  $50\ \Omega$  to ground near the driver output as shown in Figure 5. Series resistors,  $R_s$ , are used to limit overshoot due to the fast transient current. Because HCSL drivers require a DC path to ground, AC coupling is not allowed between the output drivers and the  $50\ \Omega$  termination resistors.



**Figure 5. DC Coupled HCSL Operation**

### Termination for AC-Coupled Differential Operation

AC coupling allows for shifting the DC bias level (common-mode voltage) when driving different receiver standards. Because AC-coupling prevents the driver from providing a DC bias voltage at the receiver, it is important to ensure the receiver is biased to its ideal DC level. The PI6C20400A does not have an internal DC bias, therefore an external DC bias circuit to around  $350\text{mV}$  is needed when PI6C20400A is the receiver in the AC-coupled operation.

**PI6C20400A**

**Part Marking**

L Package

Y: Die Rev  
YY: Year  
WW: Workweek  
1st X: Assembly Code  
2nd X: Fab Code

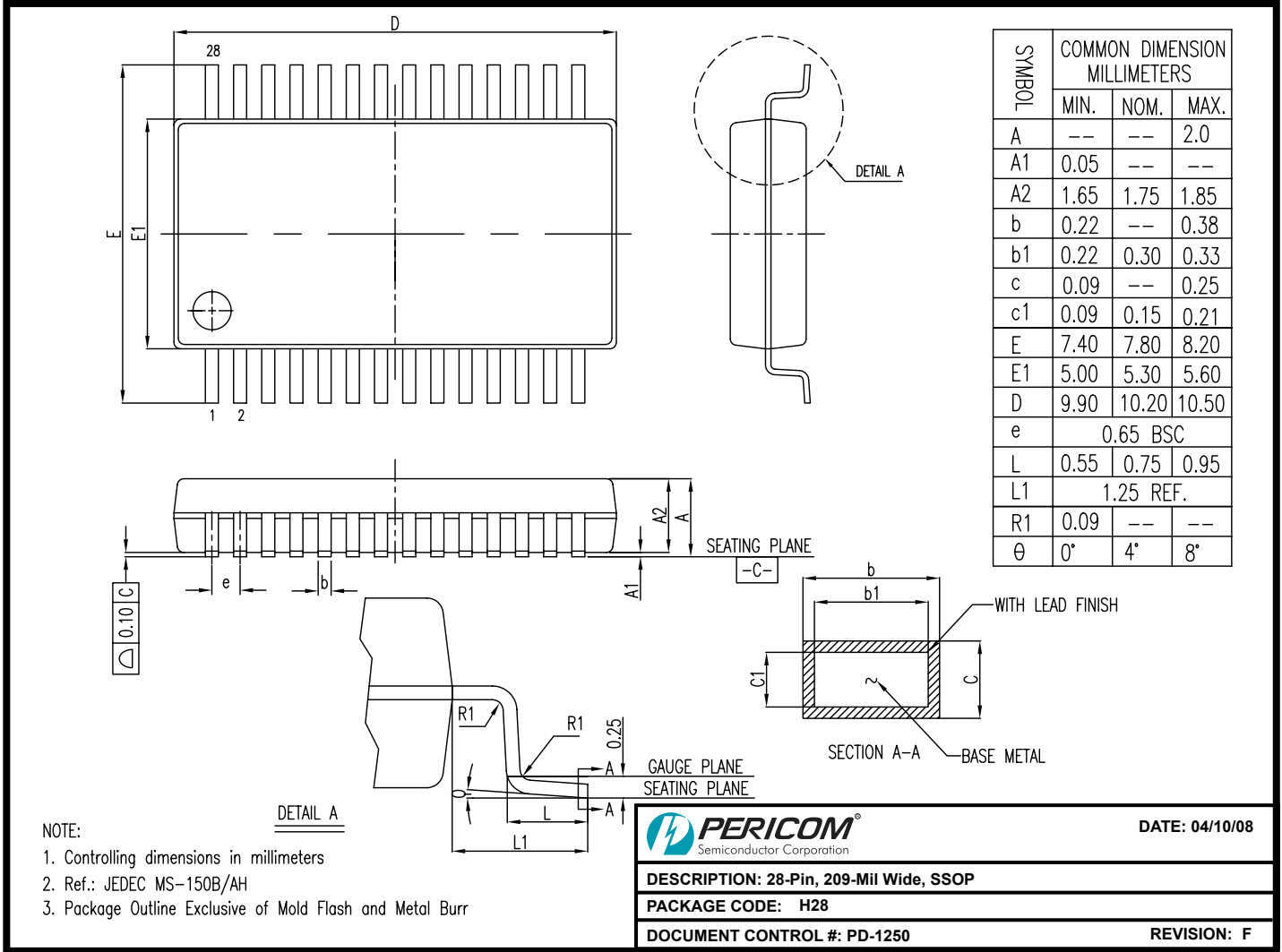
H Package

YY: Year  
WW: Workweek  
1st X: Assembly Code  
2nd X: Fab Code

**PI6C20400A**

**Packaging Mechanical**

28-SSOP (H)



08-0143

**PI6C20400A**

28-TSSOP (L)

| SYMBOLS  | MIN.     | NOM. | MAX. |
|----------|----------|------|------|
| A        | –        | –    | 1.20 |
| A1       | 0.05     | –    | 0.15 |
| A2       | 0.80     | 1.00 | 1.05 |
| b        | 0.19     | –    | 0.30 |
| c        | 0.09     | –    | 0.20 |
| D        | 9.60     | 9.70 | 9.80 |
| E1       | 4.30     | 4.40 | 4.50 |
| E        | 6.20     | 6.40 | 6.60 |
| e        | 0.65 BSC |      |      |
| L1       | 1.00 REF |      |      |
| L        | 0.45     | 0.60 | 0.75 |
| S        | 0.20     | –    | –    |
| $\theta$ | 0°       | –    | 8°   |

NOTES:  
 1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.  
 2. JEDEC MO-153F  
 3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

16-0076

|  |             |                |
|--|-------------|----------------|
|  |             | DATE: 03/31/16 |
| DESCRIPTION: 28-Pin, 173mil Wide TSSOP |             |                |
| PACKAGE CODE: L (L28)                  |             |                |
| DOCUMENT CONTROL #: PD-1313            | REVISION: F |                |

**For latest package info.**

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

| Ordering Code | Package Code | Package Description          |
|---------------|--------------|------------------------------|
| PI6C20400AHEX | H            | 28-pin, 209-mil wide (SSOP)  |
| PI6C20400ALEX | L            | 28-pin, 173-mil wide (TSSOP) |

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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