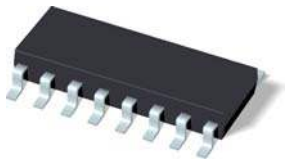
TEXAS INSTRUMENTS



UCC2585
UCC3585

SLUS304F − JULY 1999 − REVISED JANUARY 2005

LOW-VOLTAGE SYNCHRONOUS BUCK CONTROLLER

FEATURES

- **VOUT Resistor Programmable Down to 0.9 V**
- **3.3-V or 5.0-V Input Supply**
- **1% DC Accuracy**
- **High Efficiency Synchronous Switching**
- **Drives P-Channel (High Side) and N-Channel (Low Side) MOSFETs**
- **Lossless Programmable Current Limit**
- **Logic Compatible Shutdown**

APPLICATIONS

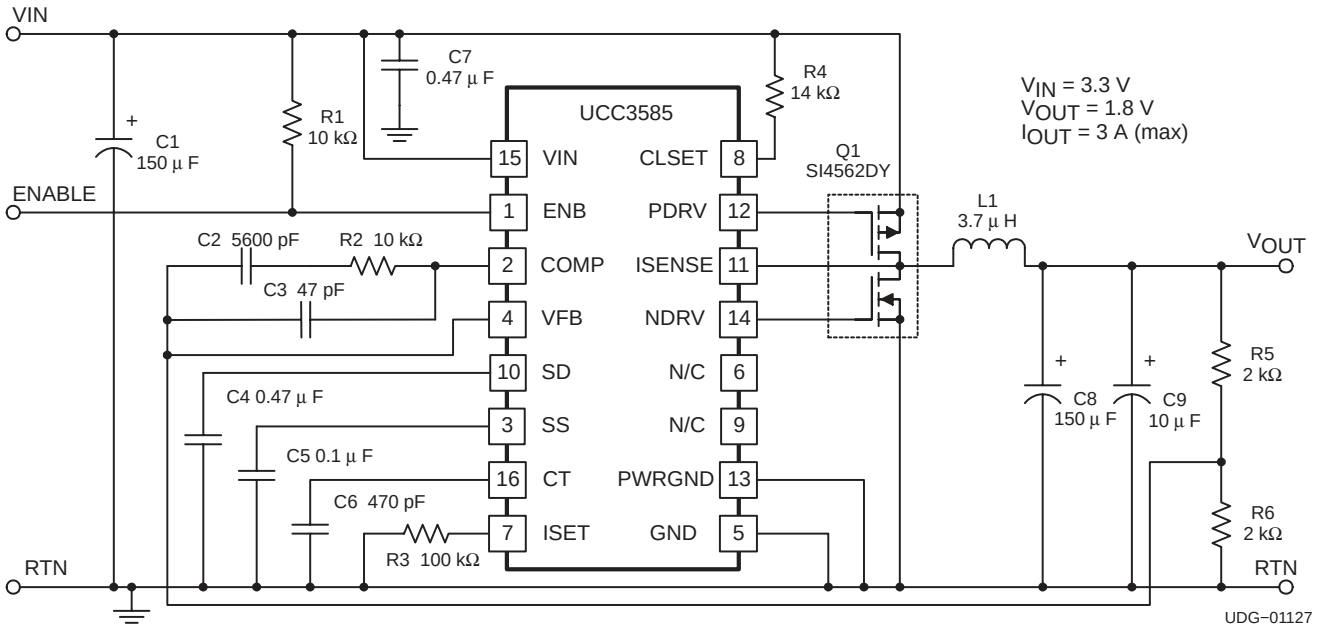
- **Local Microprocessor Core Voltage Power Supplies for Desktop and Notebook Computers**
- **DSP Core or I/O Powering**
- **High-Speed GTL Bus Regulation**

DESCRIPTION

The UCC3585 synchronous buck controller provides flexible high efficiency power conversion for output voltages as low as 0.9 V with ensured ±1% dc accuracy. With an input voltage range of 3.0 V to 5.5 V, it is the ideal choice for 3.3 V only, 5.0 V only, or other low voltage systems. The fixed frequency oscillator is capable of providing practical PWM operation to 500 kHz.

The UCC3585 drives a complementary pair of power MOSFET transistors. A P-channel on the high side, and an N-channel on the low side step down the input voltage at up to 90% efficiency.

A programmable two-level current limiting function is provided by sensing the voltage drop across the high side P-channel MOSFET. This circuit can be configured to provide pulse-by-pulse limiting, timed shutdown after seven consecutive faults, or latch-off after fault detection, allowing maximum application flexibility. The current limit threshold can be programmed over a wide range with a single resistor.



description (continued)

The UCC3585 also includes undervoltage lockout, a logic controlled enable, and softstart functions. The UCC3585 is offered in the 16-pin surface mount and through-hole packages.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Analog pins
- Minimum and maximum forced voltage (reference to GND) . . . . . –0.3 V to 6.3 V

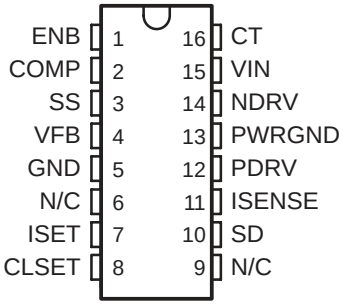
Digital pins
- Minimum and maximum forced voltage (reference to GND) . . . . . –0.3 V to 6.3 V

Power driver output pins
- Maximum forced current . . . . . ±1.0 A
- Operating junction temperature, T_J . . . . . –55°C to 125°C
- Storage temperature, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Unless otherwise noted, voltages are reference to ground and currents are positive into, negative out of, the specified terminals. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500 ns.

N, D and M PACKAGES
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		
	DIL (N)	SOIC (D)	QSOP (M)
−40°C to 85°C	UCC2585N	UCC2585D	UCC2585M
0°C to 85°C	UCC3585N	UCC3585D	UCC3585M

The M and D packages are available taped and reeled. Add an R suffix to the device type (e.g., UCC3585DR).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
N	1.1 W	11 mW/°C	610 mW	440 mW
D	830 mW	8.3 mW/°C	450 mW	330 mW
M	580 mW	5.8 mW/°C	320 mW	230 mW

electrical characteristics, these specifications hold for T_A = 0°C to 85°C for the UCC3585 and T_A = −40°C to 85°C for the UCC2585, T_A = T_J, V_{IN} = 3.3 V, V_{ENB}, V_{ISENSE} = V_{IN}, V_{FB} = 0.9 V, V_{COMP} = 1.5 V, C_T = 330 pF, R_{ISET} = 100 kΩ, R_{CLSET} = 10 kΩ, (unless otherwise noted)

input supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply current − total (active)			2.3	3.5	mA
Supply current – shutdown	ENB = 0 V		10	25	µA
VIN turnon threshold (UVLO)		1.60	1.95	2.20	V
VIN turnon hysteresis			110	200	mV

voltage amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage (internal reference)	V_{IN} = 3.0 V to 3.6 V, T_A = 25°C, See Note 1	0.891	0.9	0.909	V
	V_{IN} = 3.0 V to 3.6 V, T_A = 0°C to 85°C, See Note 1	0.889	0.9	0.911	
	V_{IN} = 3.0 V to 3.6 V, T_A = −40°C to 85°C, See Note 1	0.886	0.9	0.914	
Open loop gain	COMP = 0.5 V to 2.5 V	60	80		dB
Output voltage high	I_{COMP} = –50 µA	2.80	2.95		V
Output voltage low	I_{COMP} = 50 µA		0.10	0.25	
Output source current		–175	–300		µA
Output sink current		2.0	3.0		mA

NOTE: 1. Measured on COMP with the error amplifier in a unity gain (voltage follower) configuration.

oscillator/PWM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Initial accuracy	VIN = 3.3 V	345	420	475	kHz
	VIN = 5.0 V	345	425	485	kHz
CT ramp peak-to-valley	T_A = 0°C to 85°C	1.8	2.1	2.3	V
	T_A = −40°C to 85°C	1.7	2.1	2.3	
CT ramp peak			2.5	2.8	
CT ramp valley voltage	T_A = 0°C to 85°C	0.3	0.4		
	T_A = −40°C to 85°C	0.27	0.40		
PWM maximum duty cycle	COMP = 2.8 V, Measured on PDRV	100			%
PWM delay to outputs	COMP = 2.5 V		85	140	ns
Enable high threshold	Measured on ENB, See Note 3		2.8		V
Enable low threshold	Measured on ENB		0.5		
Softstart charge current	SS = 0 V, T_A = 0°C to 85°C	9.0	13.5	16.0	µA
	SS = 0 V, T_A = −40°C to 85°C	9.0	13.5	19.0	

NOTE: 3. Enable high threshold = (V_{IN} − 0.5).

electrical characteristics, these specifications hold for T_A = 0°C to 85°C for the UCC3585 and T_A = −40°C to 85°C for the UCC2585, T_A = T_J, V_{IN} = 3.3 V, V_{ENB}, V_{ISENSE} = V_{IN}, V_{FB} = 0.9 V, V_{COMP} = 1.5 V, C_T = 330 pF, R_{ISET} = 100 kΩ, R_{CLSET} = 10 kΩ, (unless otherwise noted)

current limit

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Comparator offset voltage			−25	0	25	mV
CLSET current	V_{IN} = 3.3 V,	T_A = 0°C to 85°C	10.0	11.5	14.0	µA
	V_{IN} = 5 V,	T_A = 0°C to 85°C	11.0	12.5	15.0	
	V_{IN} = 3.3 V,	T_A = −40°C to 85°C	9.0	11.5	14.0	
	V_{IN} = 5 V,	T_A = −40°C to 85°C	9.5	12.5	15.0	
SD sink current	SD = 2 V,	T_A = 0°C to 85°C	8.5	11.0	13.5	
	SD = 2 V,	T_A = −40°C to 85°C	7.5	11.0	13.5	
SD source current	SD = 2 V		0.7	1.1		mA
Restart threshold	Measured on SD		0.40	0.55	0.70	V

output driver

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Pullup resistance (PDRV)	–50 mA (source),	T_A = 0°C to 85°C	4.5	6.0	9.0	Ω
	–50 mA (source),	T_A = −40°C to 85°C	3.5	6.0	9.0	
Pulldown resistance (PDRV)	50 mA (sink),	T_A = 0°C to 85°C	6.0	9.0	16.5	
	50 mA (sink),	T_A = −40°C to 85°C	4.0	9.0	16.5	
Pullup resistance (NDRV)	–50 mA (source),	T_A = 0°C to 85°C	4.5	6.0	9.0	
	–50 mA (source),	T_A = −40°C to 85°C	3	6	9	
Pulldown resistance (NDRV)	100 mA (sink),	T_A = 0°C to 85°C	2.0	3.0	4.5	
	50 mA (sink),	T_A = −40°C to 85°C	1.5	3.0	4.5	
Deadtime delay (PDRV high to NDRV high)	See Note 2		150	215	250	ns
Deadtime delay (NDRV low to PDRV low)	See Note 2		70	125	175	

NOTE: 1. Measured on COMP with the error amplifier in a unity gain (voltage follower) configuration.
NOTE: 2. 50% point of PDRV rise to NDRV rise and 50% point of NDRV fall to PDRV fall.
NOTE: 3. Enable high threshold = (V_{IN} − 0.5).

pin descriptions

CLSET: CLSET is used to program the pulse-by-pulse and overcurrent shutdown levels for the UCC3585. A resistor connected between CLSET and VIN sets the over-current threshold. The over-current threshold follows the following relationship:

$$I_{CL} = \frac{\frac{1.25}{R_{ISET}} \times R_{CLSET}}{R_{DS(on)}}$$

COMP: Output of the voltage error amplifier. Loop compensation components are connected between COMP and VFB.

pin descriptions

CT: A high quality ceramic capacitor connected between this pin and ground sets the PWM oscillator frequency by the following relationship:

$$f = \frac{1}{\left(7000 \times C_T\right)}$$

The oscillator is capable of reliable operation up to 500 kHz.

ENB: A logical 1 (V_{IN} – 0.5 V) on this input will activate the output drivers. A logical zero (0.5 V) will prevent switching of the output drivers. Do not allow ENB to remain between these levels steady state.

GND: Reference level for the IC. All voltages and currents are with respect to GND.

ISENSE: ISENSE monitors the voltage dropped across the high side P-channel MOSFET switch while it is conducting. This information is used to detect overcurrent conditions by the current limit circuitry.

ISET: A resistor is connected between ISET and ground to program a precision bias for many of the UCC3585 circuit blocks. This resistor should be 100 kΩ with a maximum tolerance of 5%. 1.25 V is provided to ISET via a buffered version of the internal bandgap voltage reference. The resulting current, 1.25 V / R_{ISET}, is mirrored directly over to CLSET to program the overcurrent threshold.

NDRV: High current driver output for the low side N-channel MOSFET switch.

PDRV: High current driver output for the high side P-channel MOSFET switch.

PWRGND: High current return path for the MOSFET drivers. PWRGND and GND should be terminated together as close as possible to the device package .

SD: This pin can configure current limit to operate in any one of three different ways.

1. A forced voltage of less than 250 mV on SD inhibits the shutdown function causing pulse by pulse limiting.
2. A capacitor from SD to GND provides a controller-converter shutdown timeout after seven consecutive overcurrent signals are received by the current limit circuitry. An internal 11-μA (typ) current sink discharges the SD capacitor to the 0.55-V (typ) restart threshold. The shutdown time is given by:

$$t_{SHUT} = \frac{\left[C_{SD} \times \left(V_{IN} - 0.55\ V\right)\right]}{11\ \mu A}$$

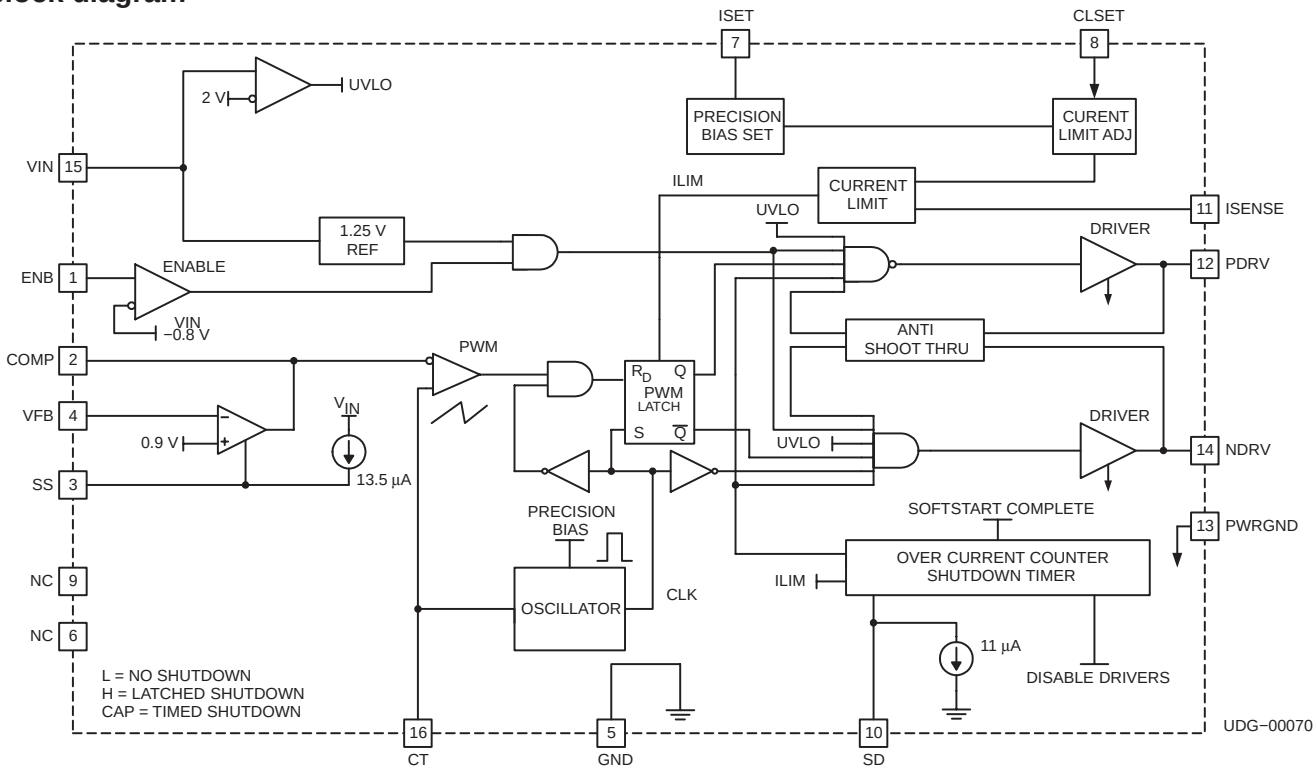
   where C_{SD} is the value of the capacitor from SD to GND, and VIN is the chip supply voltage (on pin 15). At this point, a softstart cycle is initiated, and a 1-mA current source (typ) quickly recharges SD to VIN. During softstart, pulse-by-pulse current limiting is enabled, and the 7-cycle counter is disabled until softstart is complete (i.e. charged to approximately VIN volts).
3. A forced voltage of greater than 1 V on SD will cause the UCC3585 to latch off after seven overcurrent signals are received. After the controller is latched off, SD must drop below 250 mV to restart the controller.

SS: A low leakage capacitor connected between SS and GND will provide a softstart function for the converter. The voltage on this capacitor slowly charges on start-up via an internal 13.5 μA (typ.) current source. The output of the voltage error amplifier (COMP) tracks this voltage, thereby limiting the controller duty ratio.

VFB: Inverting input to the voltage type error amplifier. The common mode input range for VFB extends from GND to 1.5 V.

VIN: Supply voltage for the UCC3585. Bypass with a 0.1-μF ceramic capacitor (minimum) to supply the peak gate drive currents required to change and discharge the power MOSFET gates. See application information for details.

block diagram



APPLICATION INFORMATION

ISET pin operation

The ISET pin develops a precision current reference for many of the UCC3585's internal circuit blocks. A resistor, R_{ISET}, connected from the ISET pin to ground sets the precision current value. The internal current reference is set by buffering the 1.25-V internal reference to the ISET pin, which results in a current of 1.25 V/R_{ISET}. The UCC3585 is designed for R_{ISET} = 100 kΩ with a maximum tolerance of 5%. Using a different resistor value results in changed parametric performance and possibly unpredictable operation.

oscillator

The oscillator frequency is programmed by a timing capacitor connected from CT to ground. The maximum recommended frequency is 500 kHz. The timing capacitor is charged and discharged by current sources derived from the ISET pin. The voltage waveform on CT is a sawtooth ramp with approximately 95% of the period spent charging the timing capacitor. Ceramic capacitors should be used, and the capacitance tolerance adds to the accuracy of the oscillator frequency. For applications that operate over a wide temperature range or where the highest accuracy is required, temperature stable ceramic capacitors such as NPO or COG dielectric should be used for the CT capacitor. The aproximate operating frequency is determined by:

$$f = \frac{1}{\left(7000 \times C_T\right)}$$

APPLICATION INFORMATION

soft-start

The SS pin provides a way to prevent overshoot of the output voltage by slowly increasing the duty cycle of the PDRV output. A capacitor on SS to ground provides a controlled start-up of the supply. During start-up the COMP pin is directly clamped to the SS pin. The SS pin has an internal current source of 13.5 μA (typical) which charges the SS capacitor. Figure 1 shows the waveforms during softstart. The SS pin charges the external capacitor to VIN volts after start-up is complete.

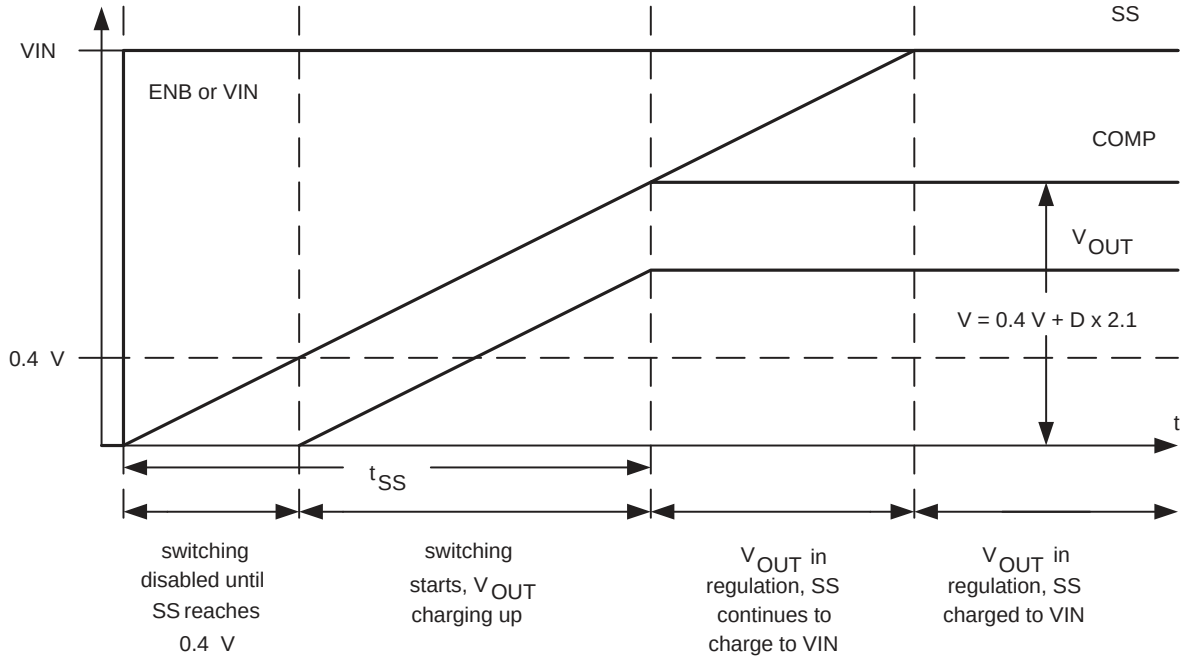


Figure 1. Waveforms During Softstart

The softstart time is approximately:

$$t_{SS} = C_{SS} \times \frac{0.4 + \left[\frac{V_{OUT}}{V_{IN}} \times 2.1\right]}{13.5\ \mu A}$$

current limit operation

The UCC3585 has a user configurable current limit for output overload protection. To reduce external component count and minimize losses, the P-channel MOSFET's $R_{DS(on)}$ is used as a current sense element. The ISENSE pin is connected to the P-channel MOSFET drain, which is internally connected to the negative input to the current-sense comparator. The positive comparator input is connected to the CLSET pin, which has an internal current sink of 11.5 μA (typical). For highest accuracy, this current sink is derived from the ISET circuitry. A resistor from VIN to CLSET sets the current limit threshold. To eliminate errors due to PCB trace impedances, the CLSET resistor should be connected directly to the P-channel MOSFET source, and the ISENSE pin should be directly connected to the P-channel MOSFET drain. Figure 2 shows a simplified diagram of the current limit circuitry.

APPLICATION INFORMATION

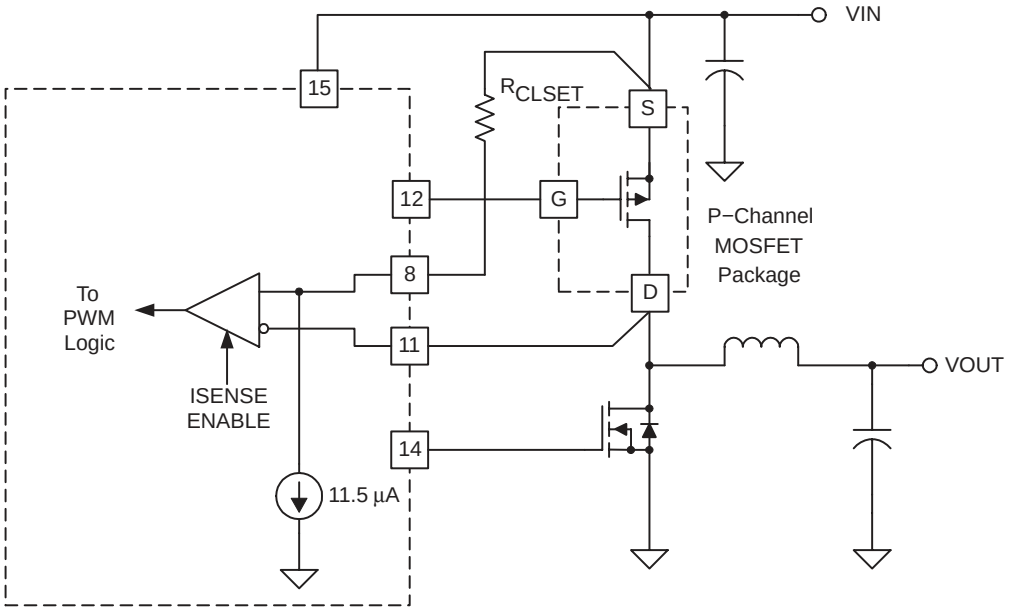


Figure 2. Current Limit Circuitry

The peak current limit is calculated using the following equation:

$$I_{CL} = \frac{\frac{1.25}{R_{ISET}} \times R_{CLSET}}{R_{DS(on)}}$$

When the $R_{DS(on)}$ of the P-channel MOSFET is used as the sense element, several issues arise. Before the current limit comparator is enabled, the P-channel MOSFET must be fully enhanced, and the drain to source voltage must be allowed to settle. The UCC3585 has an internal circuit that disables the current limit comparator, t_{ISENSE}, for a fixed time, starting at the PDRV output falling edge. It is important that no external gate resistor is used between the PDRV output and the P-channel gate. If a resistor is used, the PDRV output falls quickly, and the turnon of the P-channel MOSFET is delayed, possibly causing a false overcurrent event to be detected. Figure 3 shows the waveforms at the P-channel turnon instance and the t_{ISENSE} time interval.

APPLICATION INFORMATION

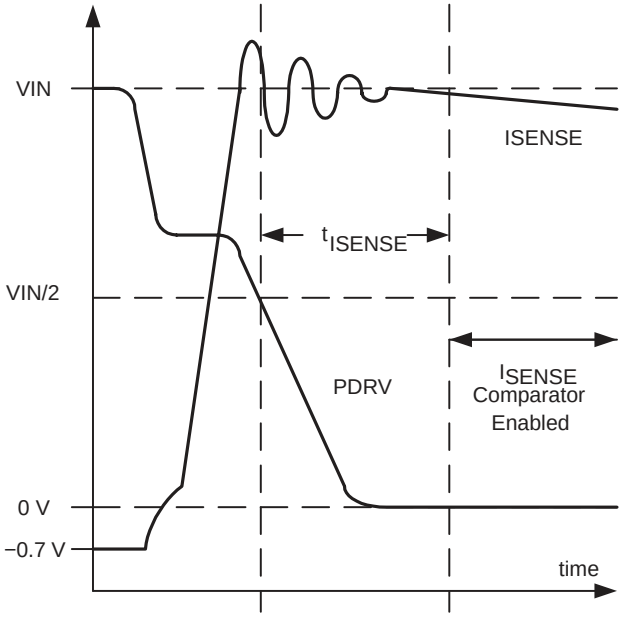


Figure 3. t_{ISENSE} Time Interval

The t_{ISENSE} time interval follows the approximate relationship:

$$t_{ISENSE} = \frac{\left(V_{BE} + 12.5\ \mu A \times R_{CLSET}\right) \times 3.2\ pF}{12.5\ \mu A}$$

As can be seen from the above equation, t_{ISENSE} is dependent upon two variables. First, t_{ISENSE} is longer for higher values of R_{CLSET}. This allows more time for ISENSE to settle, which is beneficial for supplies with a higher current limit threshold. Second, t_{ISENSE} varies with the inherent temperature dependence of the V_{BE} in the above equation. V_{BE} can be assumed to be 0.65 V at 25°C with a temperature coefficient of −2 mV/°C. Since the t_{ISENSE} time interval decreases at high temperature, operation of the supply must be verified at the maximum ambient temperature at full output load.

Another issue with using the MOSFET $R_{DS(on)}$ for the sense element is the minimum on time for the P-channel MOSFET. Since there is a blanking interval, t_{ISENSE}, there is a minimum time that the P-channel MOSFET stays on during any PWM period. The minimum on time occurs even with the power supply output shorted, experimentally the minimum on time is approximately 400 ns. When a converter is operated continuously into a shorted or overloaded output, this minimum on time results in a significant power dissipation and stress on both MOSFETs.

APPLICATION INFORMATION

A solution to this minimum on-time is a counter and time-out circuit. As described in the SD pin description, a capacitor on SD enables the time-out circuit. An internal digital counter is used to count the overcurrent events at the current-sense comparator output. When seven overcurrent conditions are reached, both MOSFET switches are turned off, the SS capacitor is discharged, and an 11 µA (typical) internal current sink discharges the SD capacitor. During this discharge time, both MOSFETs are held off, and the inductor current decays to zero. When the SD capacitor voltage reaches 0.55 V (typical), a softstart cycle restarts the converter. During softstart, the 7-cycle counter is disabled. However, the peak current limit comparator is enabled. When the SS voltage reaches the threshold equal to (V_{IN} − 0.5 V), the 7-cycle counter is enabled. By sizing the SS capacitor relative to the SD capacitor, the amount of time spent switching the MOSFETs can be reduced when the output is overloaded. If the timeout mode is used, the relative capacitance values for C_{SS} and C_{SD} must fall into the following relationship:

$$C_{SD} \leq 20 \times C_{SS}$$

This equation also states that, if the time-out mode is used, a softstart capacitor must be used. Figure 4 shows the waveforms when the converter is operated into a short circuit.

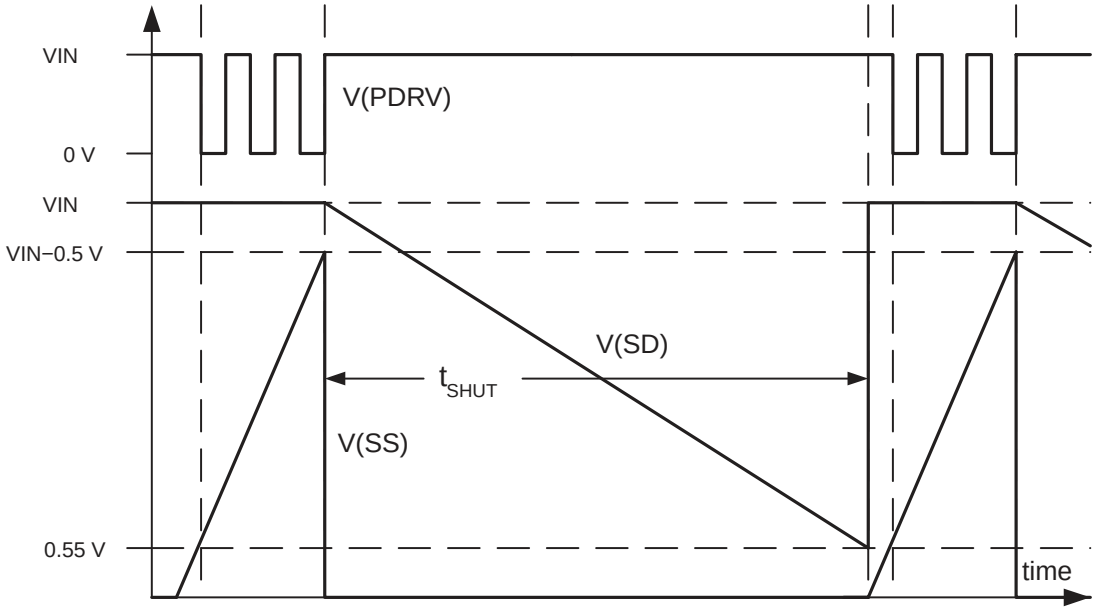


Figure 4. Converter Operated Into Short Circuit

APPLICATION INFORMATION

VIN bypass capacitor selection

A ceramic capacitor must be used across VIN to GND on the UCC3585. This capacitor supplies the transient currents required to turn on and off both power MOSFETs. It is important to select a high enough capacitance value to keep the peak-to-peak ripple voltage at VIN below 100 mV. The maximum peak-to-peak ripple on VIN is somewhat arbitrary, and 100 mV is used as an estimate. Knowing the P-channel total gate charge, Q_P and the total gate charge for the N-channel MOSFET, Q_N, the minimum capacitance can be found:

$$C_{VIN(min)} = \frac{Q_P + Q_N}{100\ mV}$$

An estimate of Q_P can be found from the manufacturer's data sheet curve for gate charge vs gate to source voltage. Since the N-channel MOSFET is switched with essentially zero volts across it, a better estimation of Q_N is found by multiplying the input capacitance, C_{ISS} and the V_{IN} voltage. Because C_{ISS} is voltage dependent, it is important to use the C_{ISS} value for approximately zero volts drain to source. This gives a more accurate estimation of the N-channel gate charge.

power MOSFET drivers

The UCC3585 contains two high current power MOSFET drivers. The source and sink current capability of these drivers has been sized to allow operation without external gate resistors. The P-channel driver has approximately three times stronger source current than sink current. This intentionally slows down the turnon of the P-channel MOSFET, which reduces the reverse recovery snap of the N-channel MOSFET body diode. The N-channel driver has a stronger sink current than source current which aids in keeping the N-channel MOSFET off when the P-channel MOSFET is turned on. Adding a gate resistor from NDRV to the N-channel MOSFET gate makes the N-channel more sensitive to dV/dt induced turnon and should be avoided. The MOSFET drivers have lower resistance at VIN = 5 V as compared to VIN = 3.3 V. At VIN = 5 V, the drivers have approximately 60% of the resistance specified at VIN = 3.3 V.

operation over wide VIN ranges

It is possible to design UCC3585 based supplies to operate over both the 3.3-V and 5-V input ranges. The resulting V_{IN} range can be as wide at 3.0 V to 5.5 V. For a successful design, several design steps must be taken. First, both MOSFETs should have $R_{DS(on)}$ rated at 2.7 V or 2.5 V. This assures reasonable efficiency at the lowest input voltage. Second, the current limit threshold should be set at the minimum input voltage. At the minimum input voltage, the P-channel MOSFET has maximum $R_{DS(on)}$. As VIN is increased to 5.5 V, the $R_{DS(on)}$ decreases considerably. The effect of this reduction in $R_{DS(on)}$ is a higher current limit. Also, note that critical parameters, such as CLSET current and oscillator frequency are specified at both 3.3 V and 5.0 V.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC3585D	NRND	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	UCC3585D	
UCC3585DG4	NRND	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	UCC3585D	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

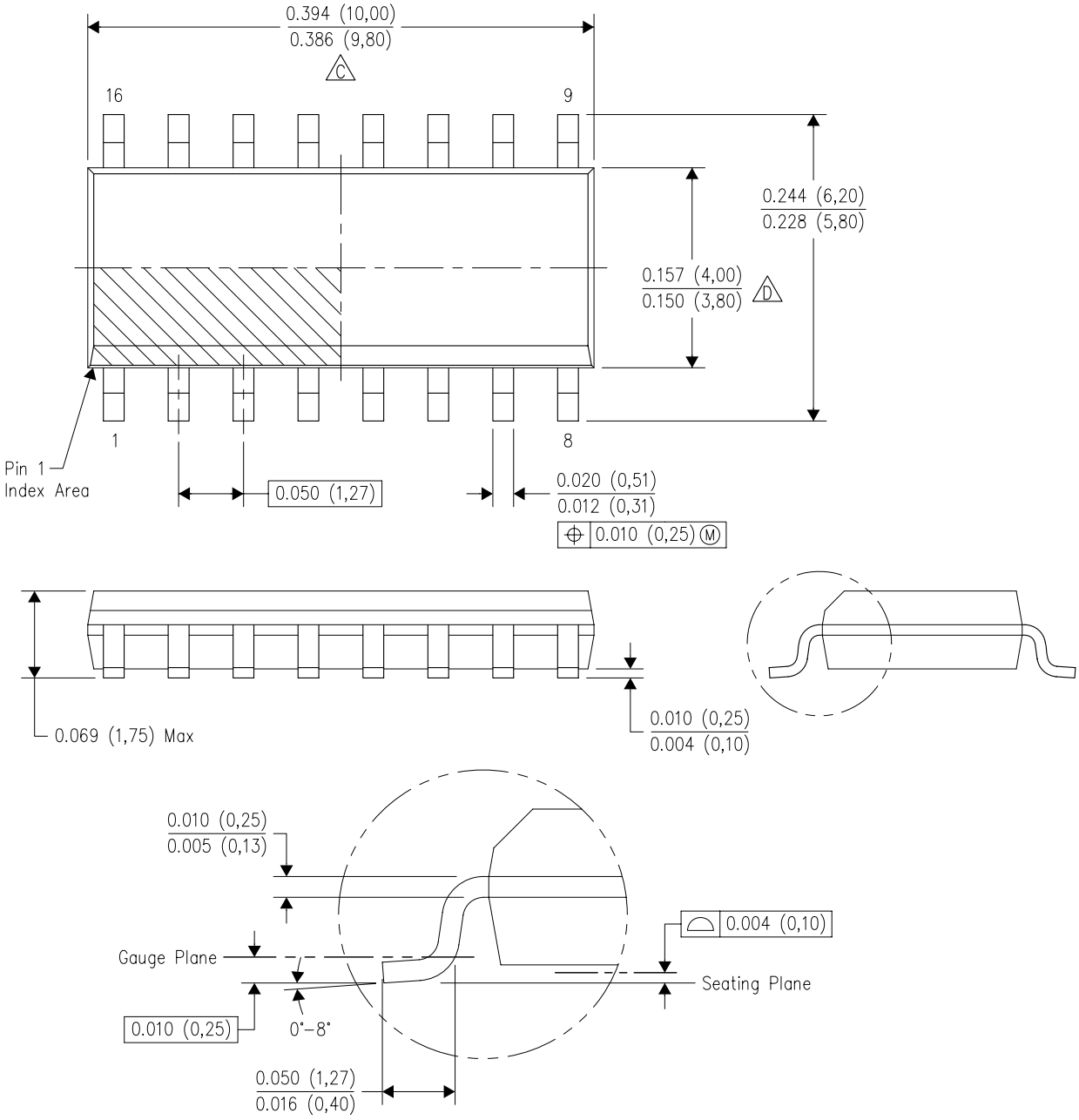
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

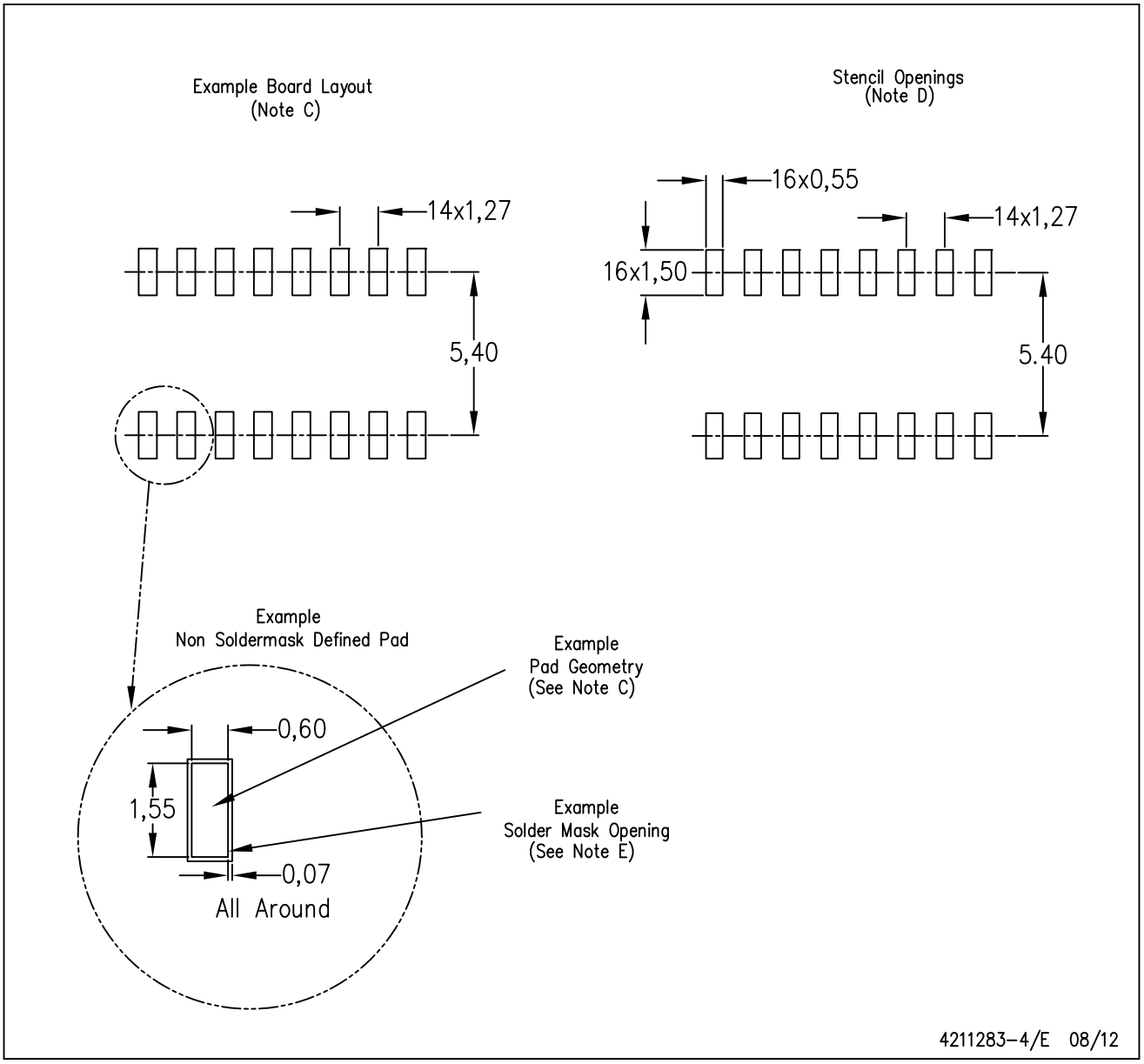
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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