

D40D SeriesFile Number **2334**

T-33-05

**1-Ampere Silicon N-P-N
Power Transistors**

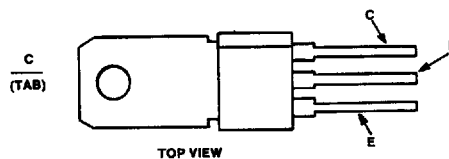
Complementary to the D41D Series

Features:

- High free-air power dissipation
- Low collector saturation voltage (0.5V typ. @ 1.0A I_C)
- Excellent linearity
- Fast switching

The D40D-series of silicon n-p-n power transistors are designed for various specific and general purpose applications, such as: output and driver stages of amplifiers operating at frequencies from DC to greater than 1 MHz; series, shunt and switching regulators; and low and high frequency inverters/converters.

These devices are supplied in the JEDEC TO-202AB plastic package.

TERMINAL DESIGNATIONS

92CS-43222

JEDEC TO-202AB**MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$) (unless otherwise specified)**

RATING	SYMBOL	D40D1, 2	D40D4, 5	D40D7, 8	UNITS
Collector-Emitter Voltage	V_{CEO}	30	45	60	Volts
Collector-Emitter Voltage	V_{CES}	45	60	75	Volts
Emitter Base Voltage	V_{EBO}	5	5	5	Volts
Collector Current — Continuous	I_C	1	1	1	A
Peak ⁽¹⁾	I_{CM}	1.5	1.5	1.5	
Base Current — Continuous	I_B	0.5	0.5	0.5	A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.67	1.87	1.67	Watts
@ $T_C = 25^\circ\text{C}$		6.25	6.25	6.25	
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	75	75	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	20	20	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: $\frac{1}{8}$ " from Case for 5 Seconds	T_L	+260	+260	+260	$^\circ\text{C}$

(1) Pulse Test Pulse Width = 300ms Duty Cycle $\leq 2\%$.

ELECTRICAL CHARACTERISTICS (T_C = 25°C) (unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS⁽¹⁾ HARRIS SEMICOND SECTOR T-33-05					
Collector-Emitter Sustaining Voltage (I _C = 10mA)	D40D1, 2 D40D4, 5 D40D7, 8	V _{CEO(sus)}	30 45 60	— — —	Volts
Collector Cutoff Current (V _{CE} = Rated V _{CEO}) (V _{CE} = Rated V _{CES})	T _C = 25°C T _C = 150°C	I _{CES}	— —	— 1.0	μA
Emitter Cutoff Current (V _{EB} = 5V)		I _{EBO}	—	—	0.1 μA

SECOND BREAKDOWN

Second Breakdown with Base Forward Biased	FBSOA	SEE FIGURE 4
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ON CHARACTERISTICS⁽¹⁾

DC Current Gain (I _C = 100mA, V _{CE} = 2V)	D40D1, 4, 7 D40D2, 5, 8	h _{FE}	50 120	— —	150 360	—
(I _C = 1A, V _{CE} = 2V)	D40D1, 4, 7 D40D2 D40D5, 8	h _{FE}	10 20 10	— — —	— — —	—
Collector-Emitter Saturation Voltage (I _C = 500mA, I _B = 50mA)	D40D1, 2, 4, 5 D40D7, 8	V _{CE(sat)}	— —	— —	0.5 1.0	Volts
Base-Emitter Saturation Voltage (I _C = 500mA, I _B = 50mA)		V _{BE(sat)}	—	—	1.5	Volts

DYNAMIC CHARACTERISTICS

Collector Capacitance (V _{CB} = 10V, f = 1MHz)	C _{CB0}	—	8	—	pF
Current-Gain — Bandwidth Product (I _C = 20mA, V _{CE} = 10V)	f _T	—	200	—	MHz

SWITCHING CHARACTERISTICS

Resistive Load	I _C = 1A, I _{B1} = I _{B2} = 0.1A	t _d + t _r	t _s	t _f	Unit
Delay Time + Rise Time	V _{CC} = 30V, t _p = 25 μsec	—	25	—	nS
Storage Time		—	200	—	
Fall Time		—	50	—	

(1) Pulse Test PW = 300ms Duty Cycle ≤ 2%.

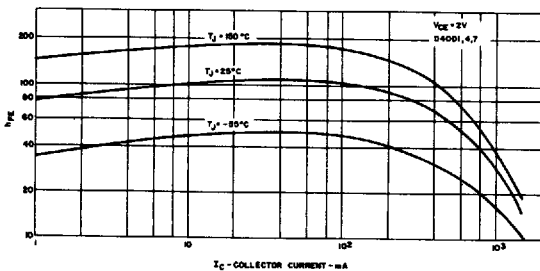


FIG. 1

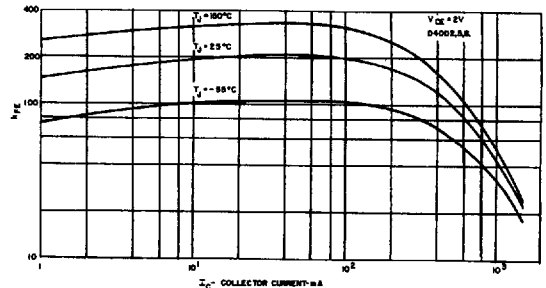


FIG. 2

TYPICAL HFE VS I_C

2-509

POWER TRANSISTORS

T-33-05

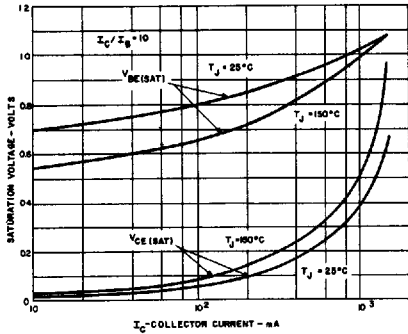


FIG. 3 TYPICAL SATURATION VOLTAGE CHARACTERISTICS

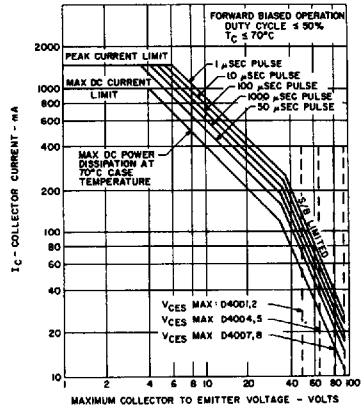


FIG. 4 SAFE REGION OF OPERATION

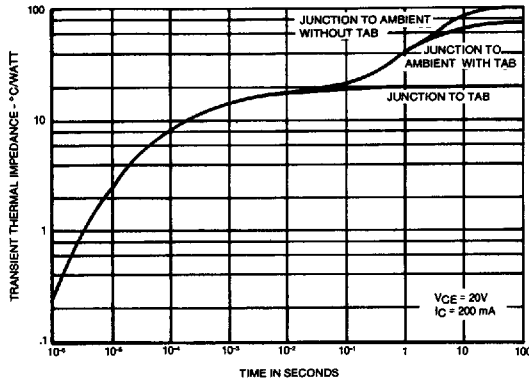


FIG. 5 MAXIMUM TRANSIENT THERMAL IMPEDANCE