



# PMN40SNA

60 V, N-channel Trench MOSFET

8 April 2021

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Very fast switching
- Extended temperature range  $T_j = 175\text{ °C}$
- Trench MOSFET technology
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

## 4. Quick reference data

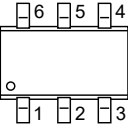
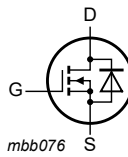
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	4.7	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 4.7\text{ A}; T_j = 25\text{ °C}$	-	29	36	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>SC-74; TSOP6 (SOT457)</p>	
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMN40SNA	SC-74; TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMN40SNA	H6

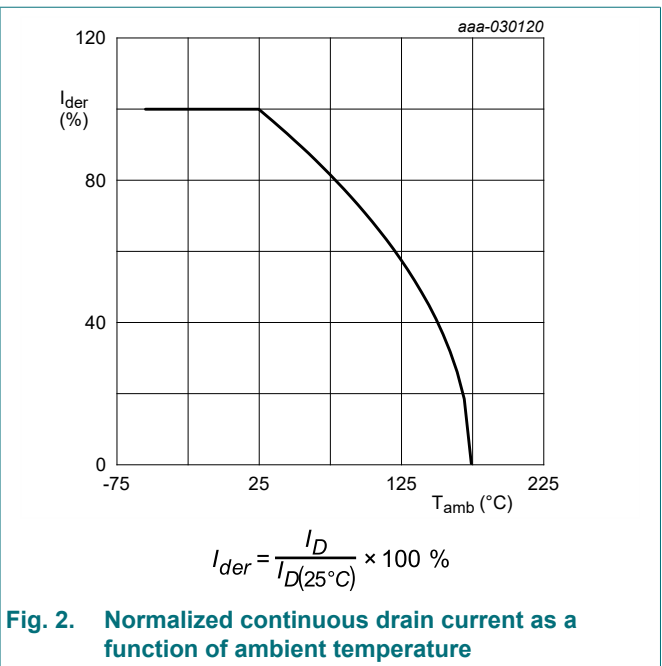
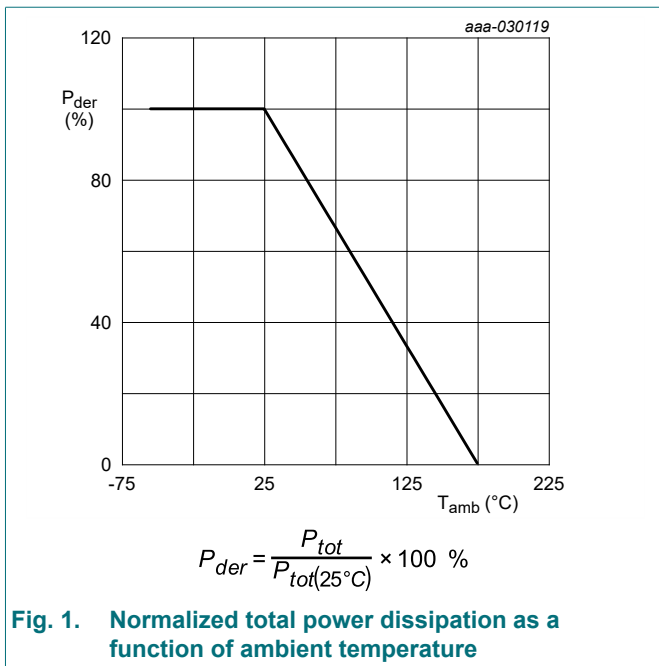
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	60	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C	[1]	-	4.7	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 100 °C	[1]	-	3	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	19	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	650	mW
			[1]	-	1.7	W
		T <sub>sp</sub> = 25 °C		-	7.5	W
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>amb</sub>	ambient temperature			-55	175	°C
T <sub>stg</sub>	storage temperature			-65	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	1.7	A
<b>ESD maximum rating</b>						
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[3]	-	500	V
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = 1 A; DUT in avalanche (unclamped)		-	30	mJ

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.



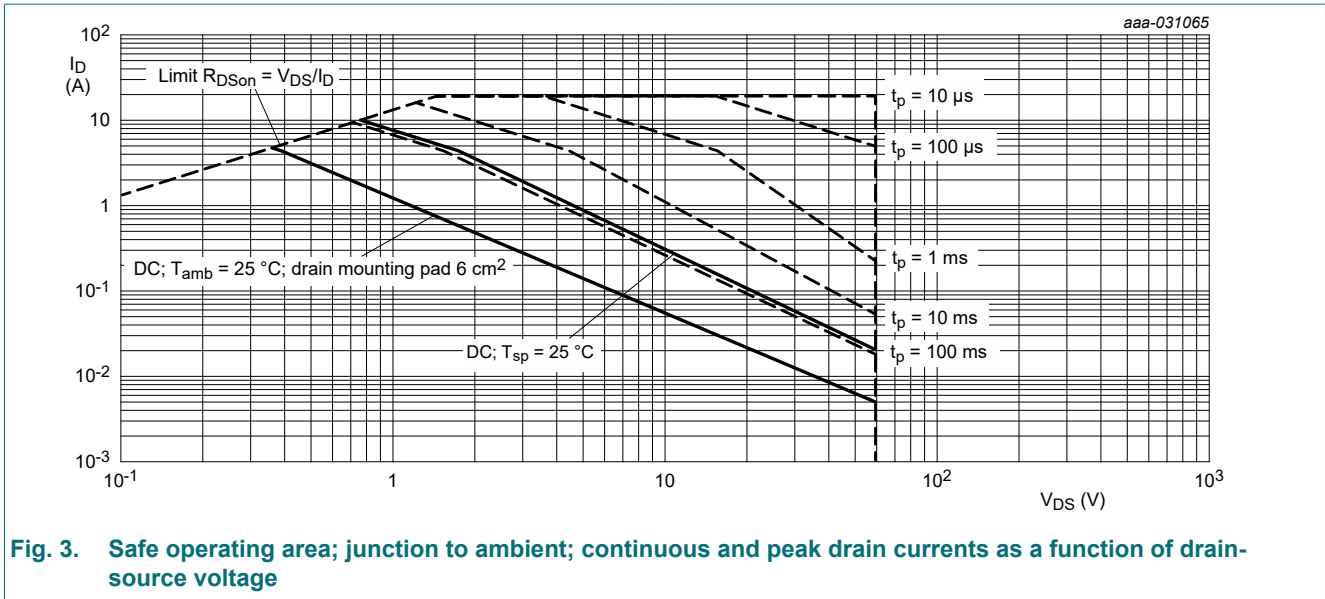


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	200	230	K/W
			[2]	-	78	90	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	15	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

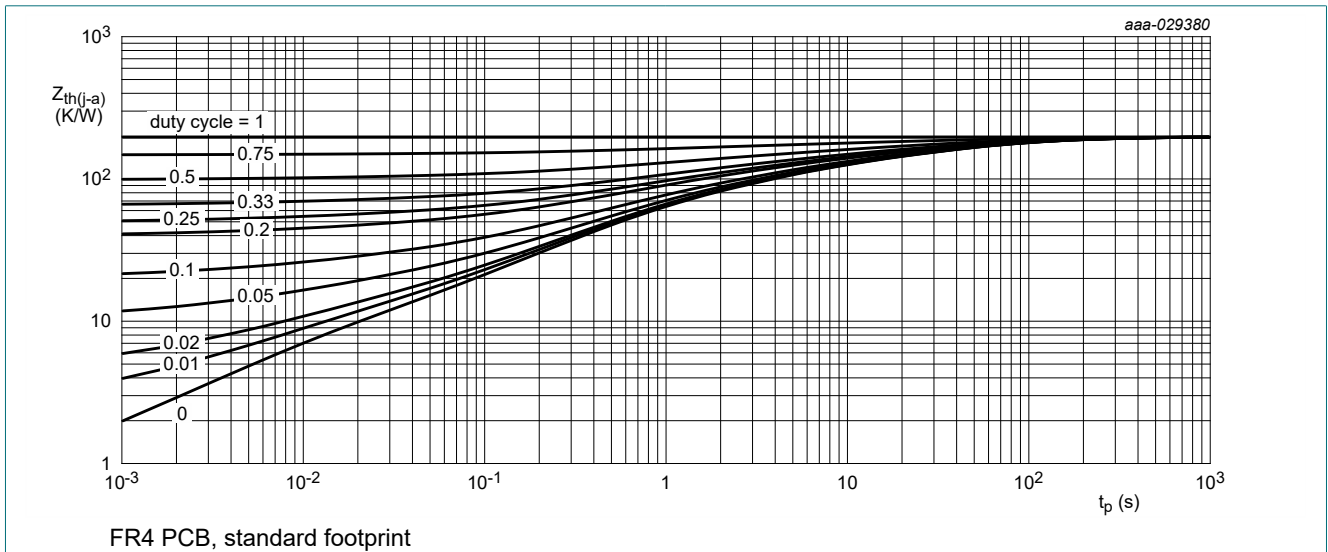


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

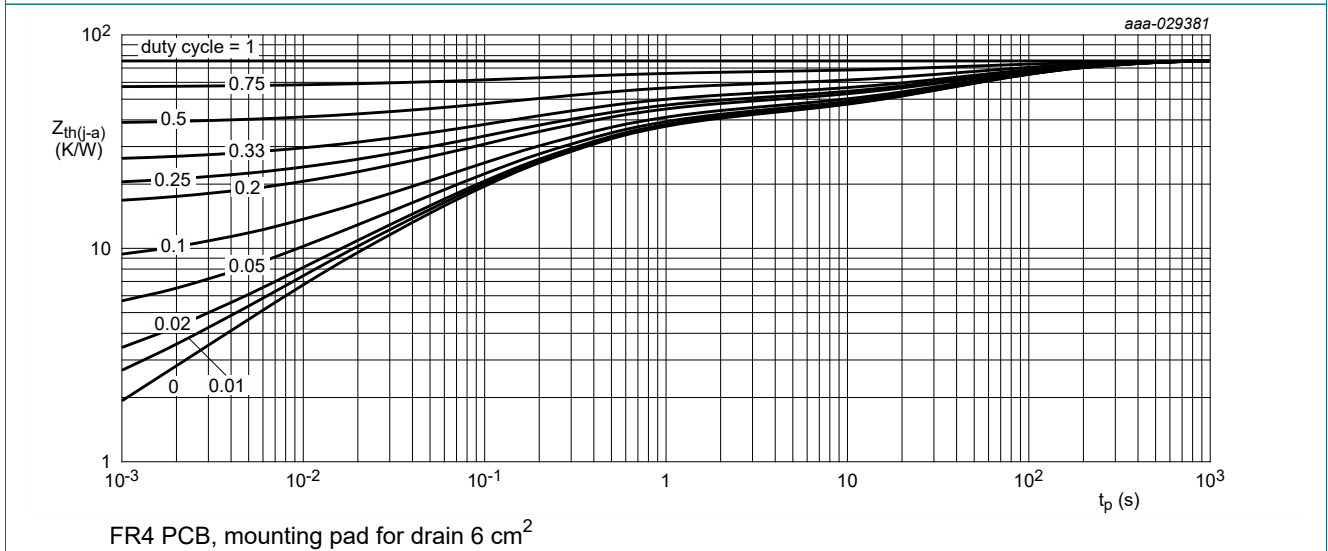


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	2.4	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 4.7 A; T_j = 25 \text{ }^\circ C$	-	29	36	m $\Omega$
		$V_{GS} = 10 V; I_D = 4.7 A; T_j = 175 \text{ }^\circ C$	-	61	76	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 V; I_D = 4.4 A; T_j = 25 \text{ }^\circ C$	-	8	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.7	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V; I_D = 4.4 A; V_{GS} = 10 V; T_j = 25 \text{ }^\circ C$	-	9	14	nC
$Q_{GS}$	gate-source charge		-	1.7	-	nC
$Q_{GD}$	gate-drain charge		-	2.8	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 30 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	453	-	pF
$C_{oss}$	output capacitance		-	62	-	pF
$C_{rss}$	reverse transfer capacitance		-	42	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V; I_D = 4.2 A; V_{GS} = 10 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	6	-	ns
$t_r$	rise time		-	7	-	ns
$t_{d(off)}$	turn-off delay time		-	11	-	ns
$t_f$	fall time		-	5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 1.7 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 1.7 A; di_S/dt = -100 A/\mu s;$	-	12	-	ns
$Q_r$	recovered charge	$V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 \text{ }^\circ C$	-	6	-	nC

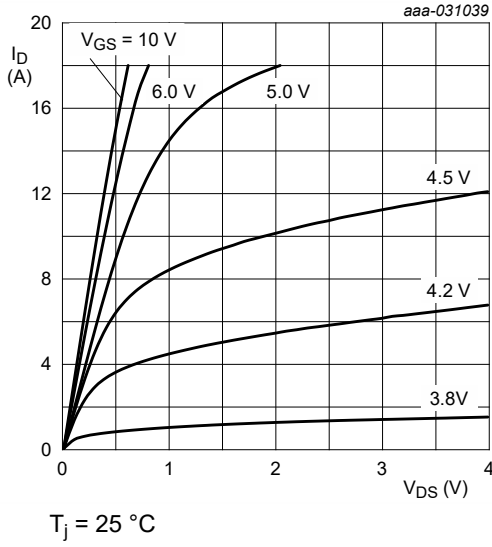


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

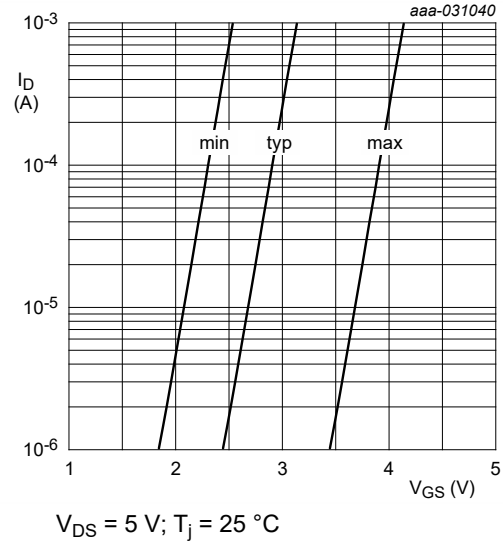


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

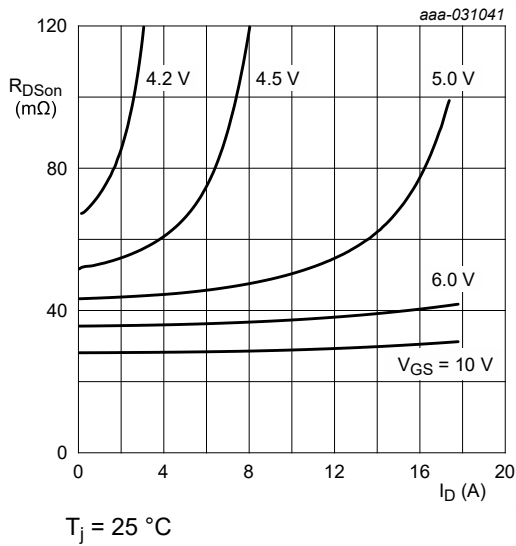


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

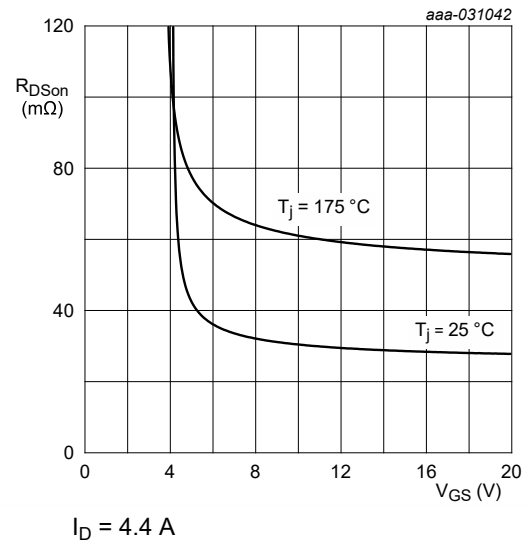


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

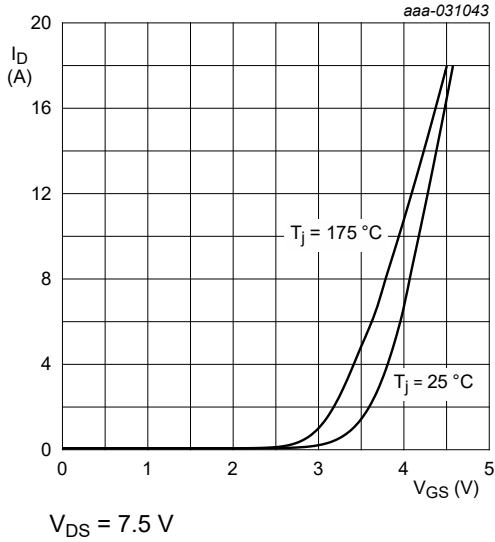
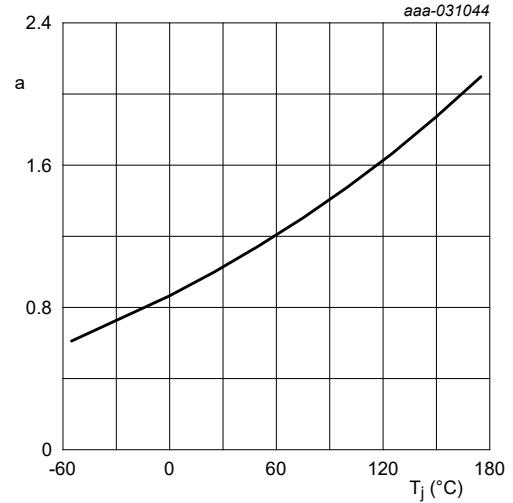
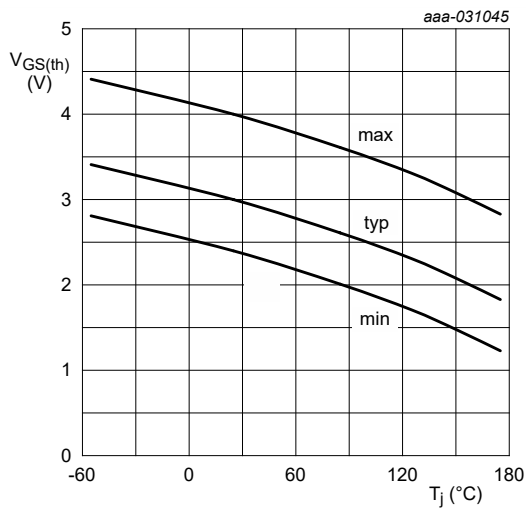


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



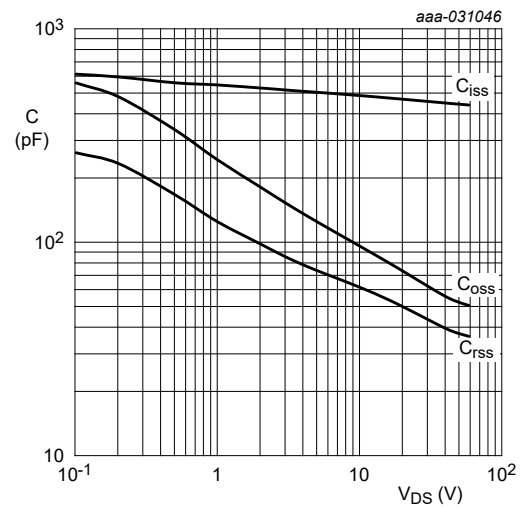
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



$I_D = 250\text{ }\mu\text{A}; V_{DS} = V_{GS}$

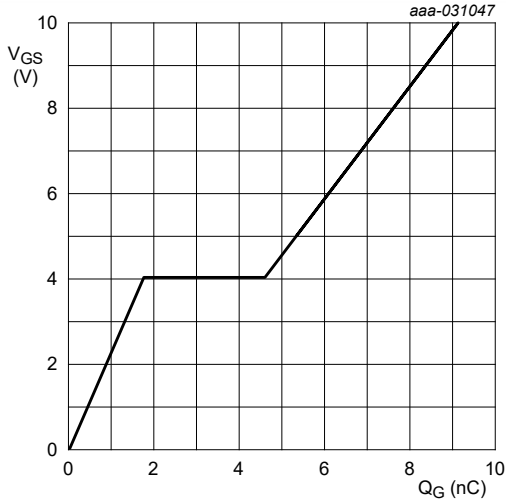
Fig. 12. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$

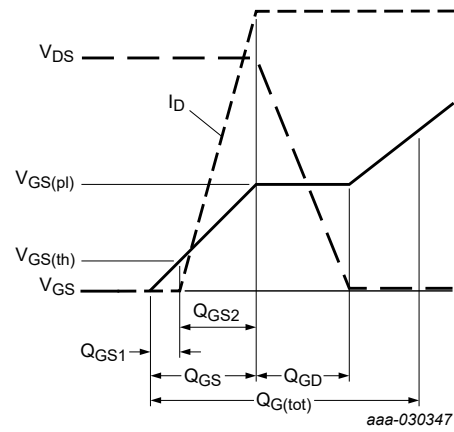
Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



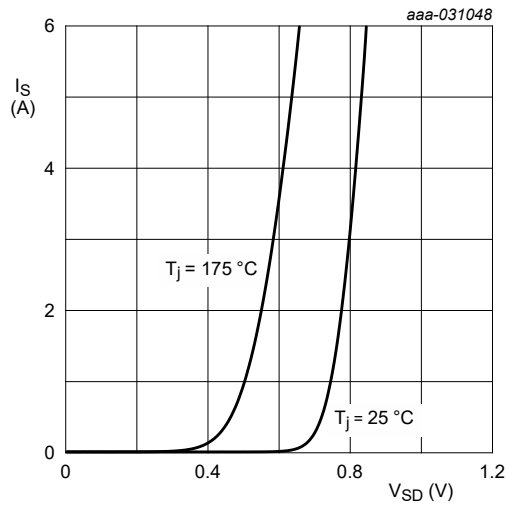


$V_{DS} = 30\text{ V}$ ;  $I_D = 4.4\text{ A}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**



**Fig. 15. Gate charge waveform definitions**



$V_{GS} = 0\text{ V}$

**Fig. 16. Source current as a function of source-drain voltage; typical values**

## 11. Test information

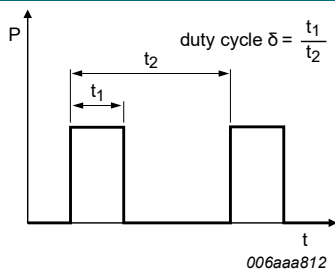


Fig. 17. Duty cycle definition

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

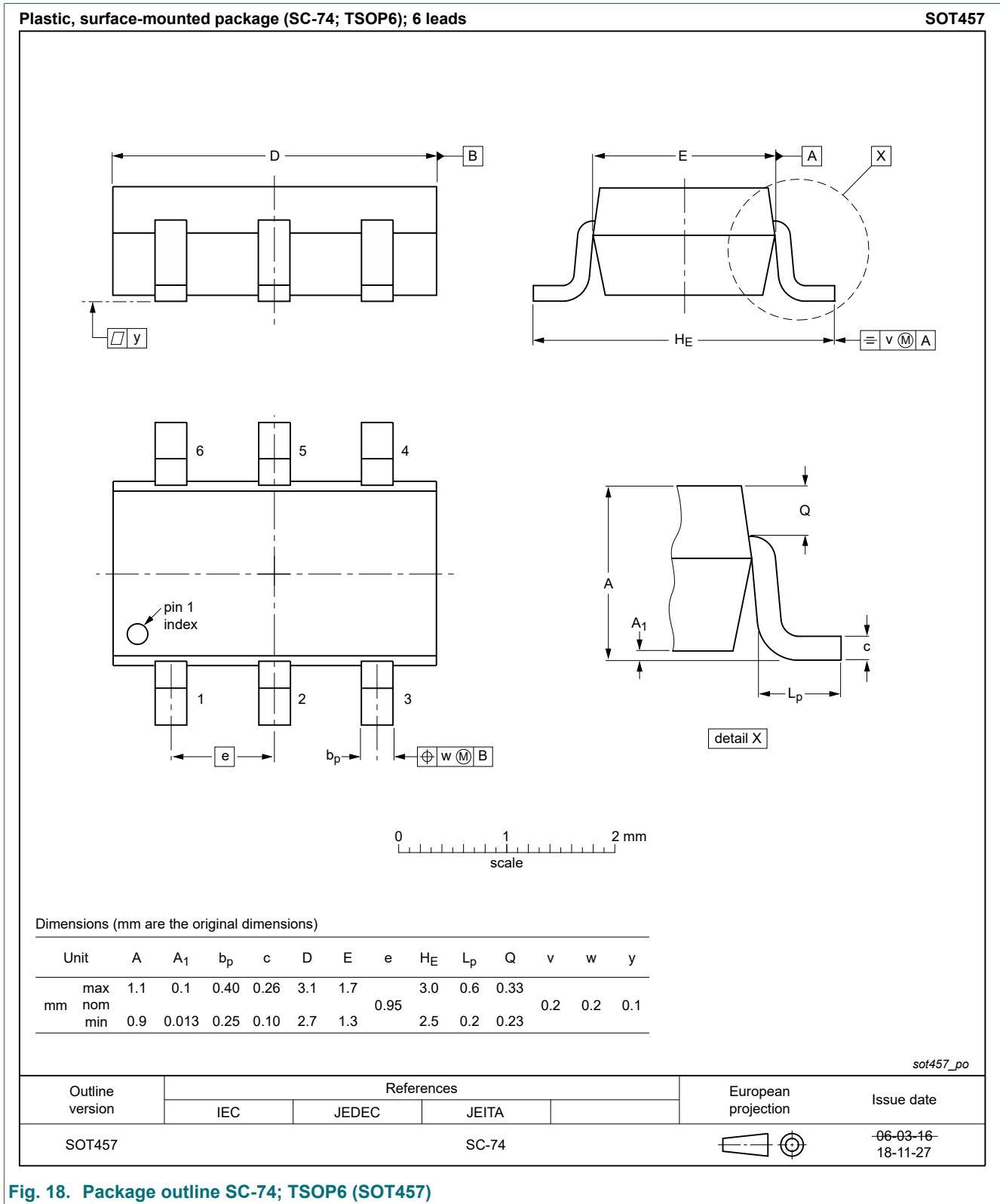


Fig. 18. Package outline SC-74; TSOP6 (SOT457)

### 13. Soldering

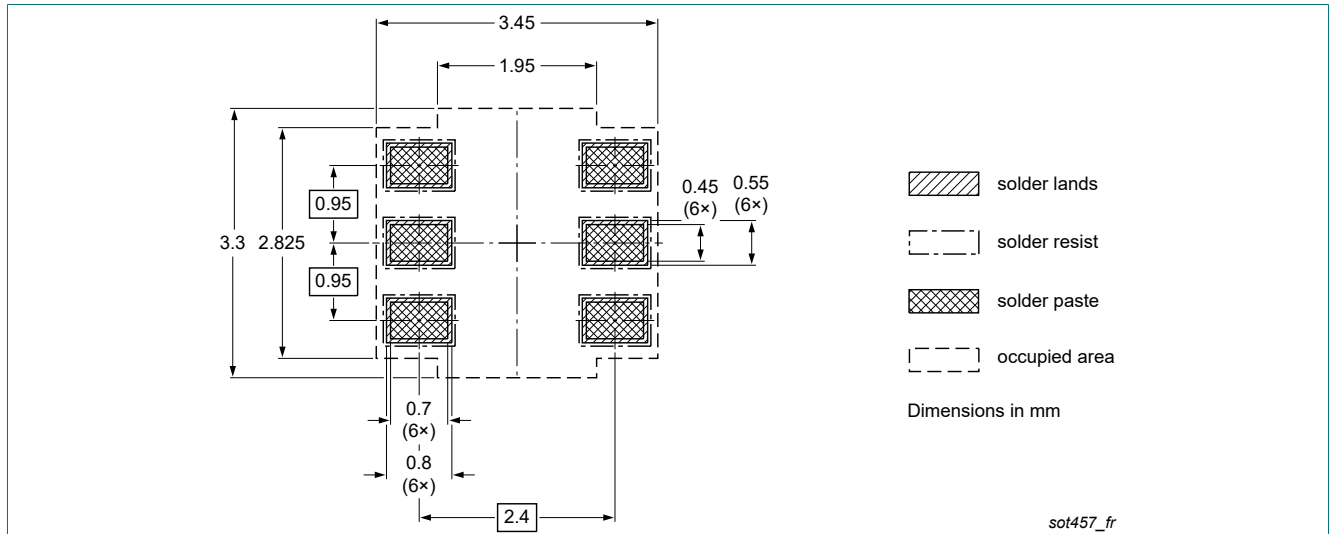


Fig. 19. Reflow soldering footprint for SC-74; TSOP6 (SOT457)

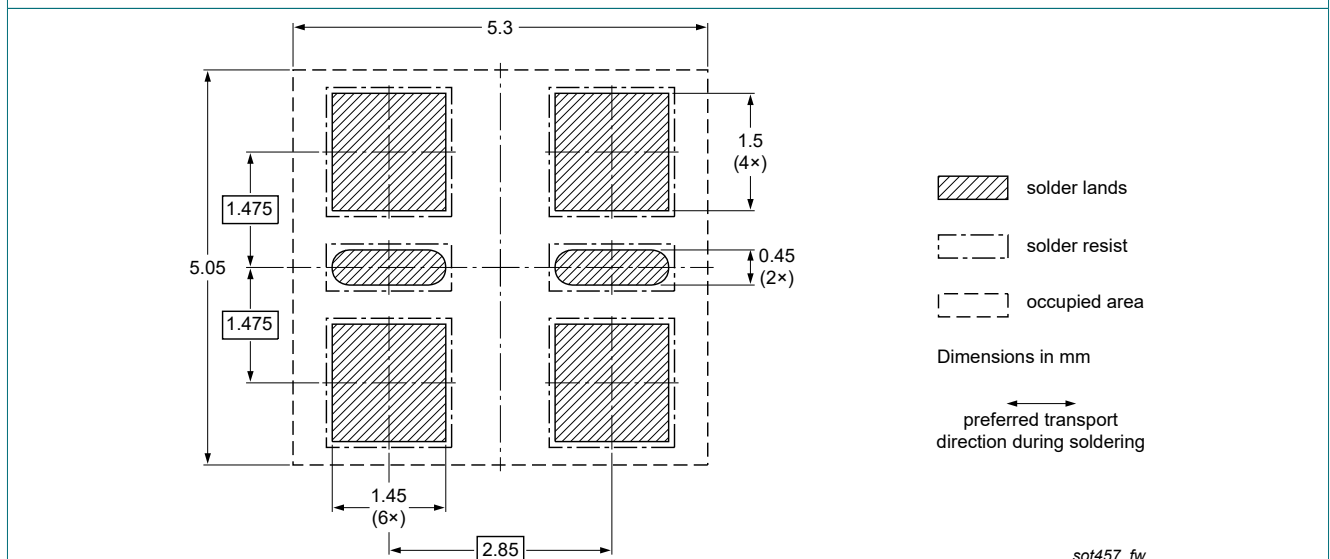


Fig. 20. Wave soldering footprint for SC-74; TSOP6 (SOT457)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMN40SNA v.2	20210408	Product data sheet	-	PMN40SNA v.1
Modifications:	• Chapter "Limiting values": Typo correction at parameter $P_{tot}$			
PMN40SNA v.1	20200311	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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