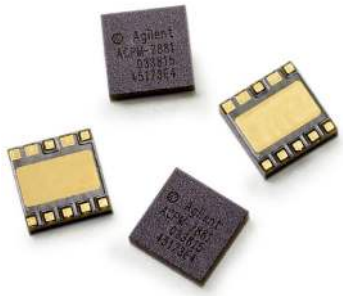
ACPM - 7881
W-CDMA Power Amplifer

Data Sheet



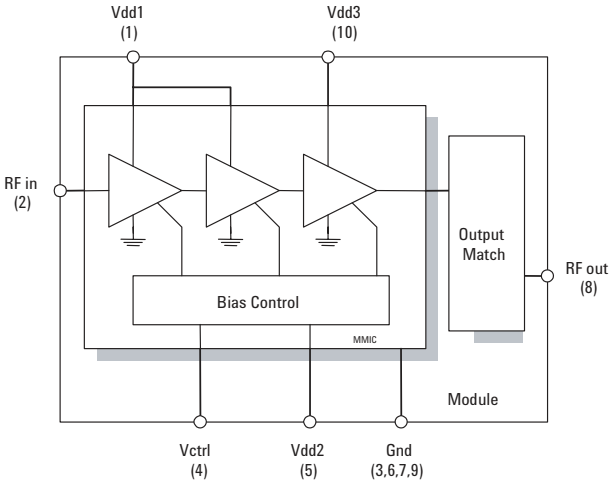
Description

The ACPM-7881 is a high performance W-CDMA power amplifier module offered in a 4x4x1.1mm package. Designed around Avago Technologies' GaAs Enhancement Mode pHEMT process, the ACPM-7881 offers premium power added efficiency and linearity in a very small form factor. The PA is fully matched to 50 Ohms on the input and output.

The amplifier has excellent ACLR and efficiency performance at max Pout, 28.5dBm, and low quiescent current (50mA) with a single bias control voltage, Vctrl = 2.0V. No regulated voltages are required to set the bias, Vdd2 can be connected directly to the battery.

Designed in a surface mount RF package, the ACPM-7881 is very cost and size competitive.

Functional Block Diagram



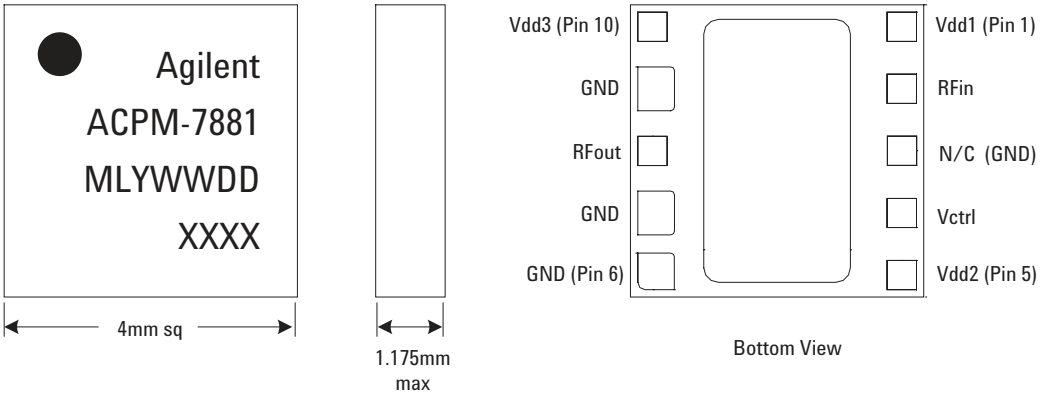
Features

- Operating frequency: 1920 - 1980 MHz
- 28.5 dBm Linear Output Power @ 3.5V
- High Efficiency 46% PAE
- Single bias, low quiescent current (50mA)
- Internal 50 ohm matching networks for both RF input & output
- No regulated voltages required
- 3.2 - 4.5 V linear operation
- 4.0 x 4.0mm SMT Package
- Low package profile, 1.1mm

Applications

- W-CDMA Handsets
- Data Cards
- PDAs

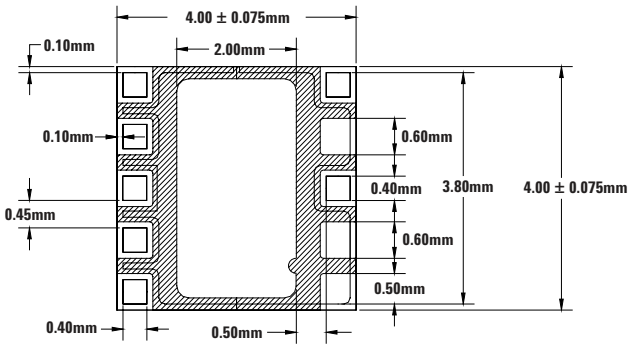
Package Diagram



Pin Description Table

Pin Number	Pin Label	Description	Function
1	Vdd1	Supply bias	1st and 2nd stages drain bias, nominally 3.5V
2	RFin	RF input	W-CDMA signal input, internally grounded through inductor. External DC block needed if DC voltage present on input trace.
3	N/C	No internal connection	Recommend ground connection on PCB
4	Vctrl	Control voltage	Output level control, nominally 2V
5	Vdd2	Supply bias	Bias circuit supply, > 2.5V; nominally 2.85V. Does not require a regulated input and can be connected directly to the battery, if desired.
6	Gnd	Ground	
7	Gnd	Ground	
8	RFout	RF output	W-CDMA signal, requires external DC block
9	Gnd	Ground	
10	Vdd3	Supply bias	3rd stage drain bias, nominally 3.5V

Package Dimensions



Viewed down through top of package

Marking Notes :

Row 3:
- ML = Manufacturing Location
  (PM = Avago Technologies Malaysia)
- Y = Year
- WW = Work Week
- DD = Date Code

Row 4:
- XXXX = Trace Code
  (Avago Technologies internal reference)

Maximum Ratings Table

Parameter	Min.	Max.
Supply voltage, Vdd1 and Vdd3		5.0 V
Supply voltage, Vdd2	-1 V	5.0 V
Analog control voltage	-1 V	3.0 V
RF input power		+5 dBm
Operating case temperature		+90 °C
Load VSWR		12:1
Storage temperature (case temperature)	-30 °C	+100 °C

Notes:
1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Avoid electrostatic discharge on I/O pins

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.
Supply voltage, Vdd1 and Vdd3	1.0 V	3.5 V	4.5 V
Supply voltage, Vdd2	2.6 V	2.85 V	4.5 V
Control voltage	1.9 V	2.0 V	2.1 V
Case temperature	-20 °C		+85 °C

Electrical Characteristics

Unless Otherwise Specified: f=1920-1980MHz, Vdd1=Vdd3=3.5V, Vdd2=2.85V, Vctrl=2.0V, Pout=28.5dBm, Ta=25°C, Zin/Zout = 50Ω

Parameter	**Min.**	**Typ.**	**Max.**	**Units**
Leakage Current, Idd1,2,3; Vctrl=0 V, RF Off		20	50	uA
Control Current, Ictrl; Vctrl=2.0 V	75	110	145	uA
Bias Current, Idd2; Vctrl=2 V, Vdd2=2.85 V		6	10	mA
Quiescent Current, Idd1,3; RF Off Vctrl=2.0 V		50	80	mA
At Pout=28.5dBm				
Supply current Idd1+Idd3		435	490	mA
PAE including Vdd1,2,3	41	46		%
Gain	26.5	29	31.5	dB
Input VSWR		1.1	2.0:1	-
ACLR				
5MHz offset		-42	-38	dBc/3.84MHz
10MHz offset		-54	-48	dBc/3.84MHz
2nd Harmonic		-50	-40	dBc/1MHz
3rd Harmonic		-60	-45	dBc/1MHz
Noise Power in Receive band, 2110 to 2170MHz Pout = -50dBm to 28.5dBm		-140	-138	dBm/Hz
Noise Figure	2.1	3.1	4.1	dB
Stability, no spurious under conditions: VSWR=4:1, all phases 3<Vdd<4.5, -50 dBm to 28.5 dBm			-60	dBc
At Pout=16dBm				
Supply current Idd1+Idd3		120	145	mA
PAE including Vdd1,2,3	7.5	9.0		%
Gain		29		dB
ACLR				
5MHz offset		-42	-38	dBc/3.84MHz
10MHz offset		-55	-48	dBc/3.84MHz

PA Operation/Shutdown Logic: DC signals

	Vctrl	**Vdd2**
Operational Mode	2.0V typ	2.6 ~ 3.5V (2.85V typ)
Shutdown	< 0.2V	0 ~ 4.5 V

Performance Graphs

Unless Otherwise Specified: f=1920-1980MHz, Vdd1=Vdd3=3.5V, Vdd2=2.85V, Vctrl=2.0V, Pout=28.5dBm, Ta=25°C, Zin/Zout = 50Ω

Data measured at 1920MHz

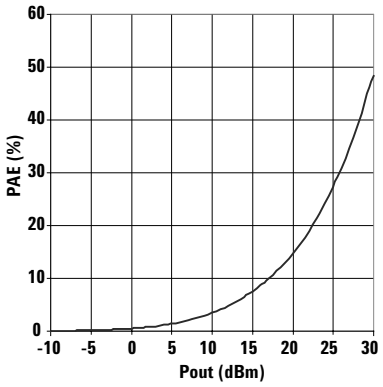


Figure 1. PAE vs Pout

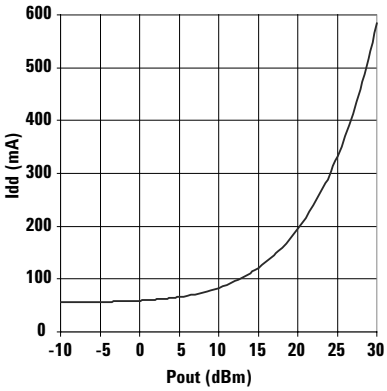


Figure 2. Total Idd vs Pout

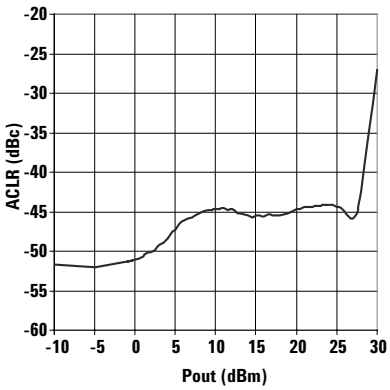


Figure 3. ACLR1 vs Pout

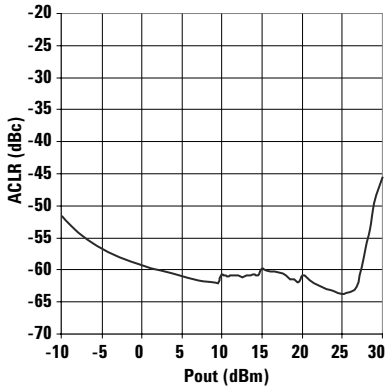


Figure 4. ACLR2 vs Pout

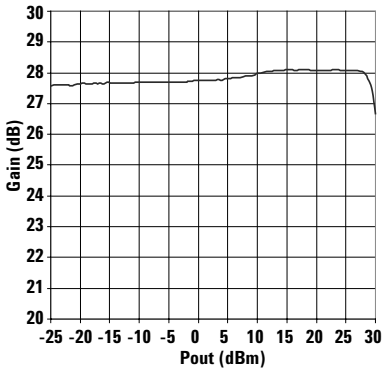


Figure 5. Gain vs Pout

Data measured at 1950MHz

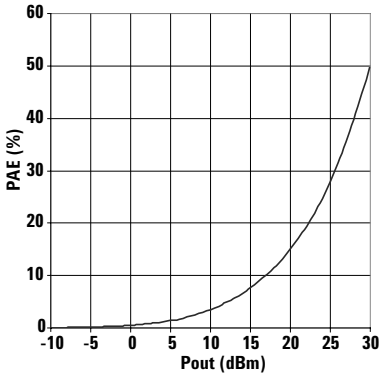


Figure 6. PAE vs Pout

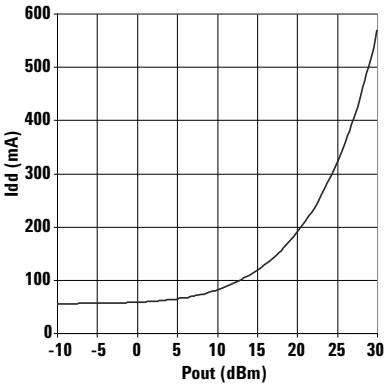


Figure 7. Total Idd vs Pout

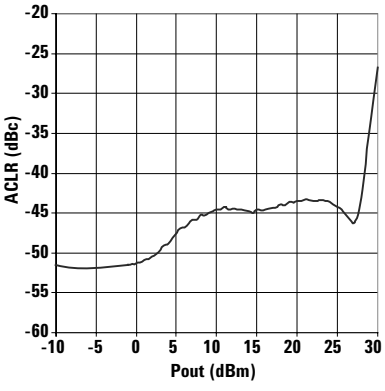


Figure 8. ACLR1 vs Pout

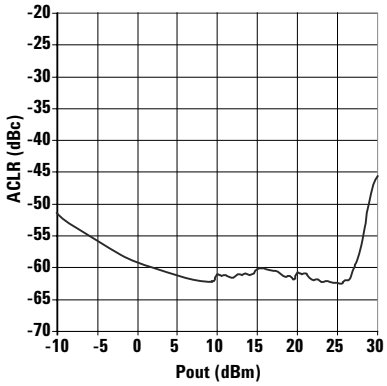


Figure 9. ACLR2 vs Pout

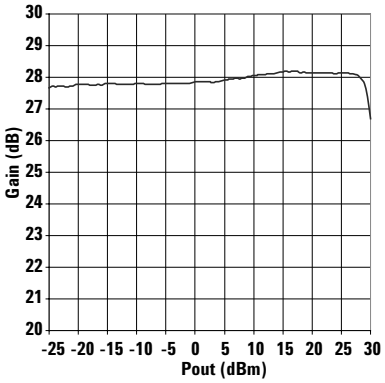


Figure 10. Gain vs Pout

Data measured at 1980MHz

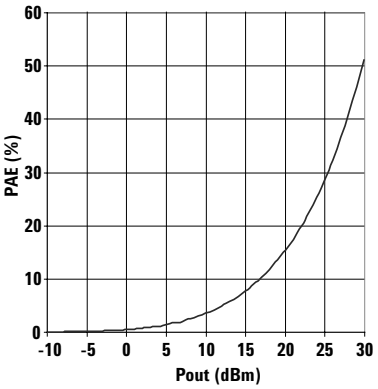


Figure 11. PAE vs Pout

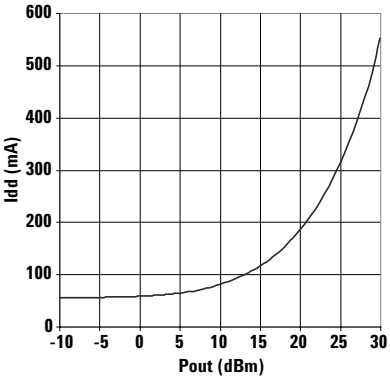


Figure 12. Total Idd vs Pout

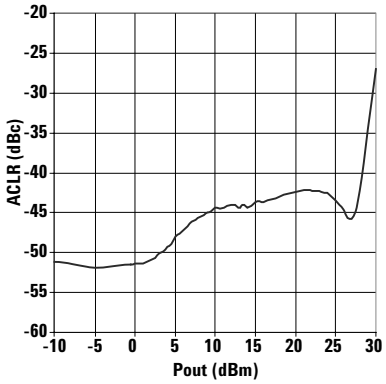


Figure 13. ACLR1 vs Pout

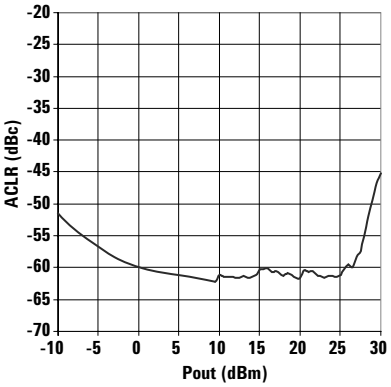


Figure 14. ACLR2 vs Pout

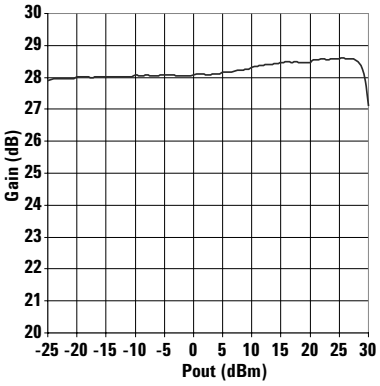


Figure 15. Gain vs Pout

ESD Sensitivity Level

Human Body Model
(EIA/JESD22-A114B): Class 1A (250Vmin, less than 500V)

Machine Model
(EIA/JESD22-A115A): Class A (50Vmin, less than 200V)

Notes:
ESD Sensitivity level for Human Body Model and Machine Model necessitate the following
handling precautions:

1. Ensure Faraday cage or conductive shield bag is used during transportation processes.
2. If the static charge at SMT assemble station is above the device sensitivity level, place an ionizer near to the device for charge neutralization purposes.
3. Personal grounding must be worn at all times when handling the devices.

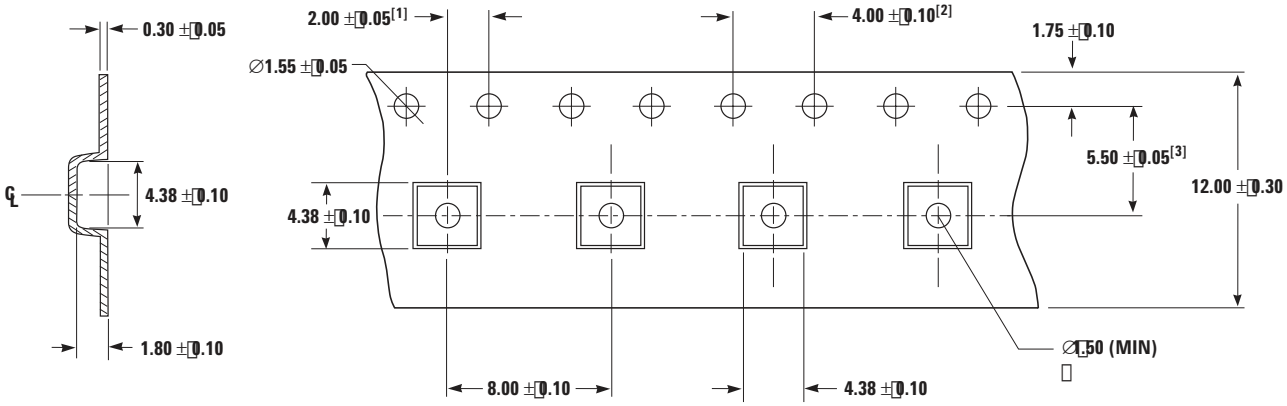
Moisture Sensitivity Classification: Class 3

Preconditioning per JESD22-A113-D Class 3 was performed on all devices prior to reliability testing.

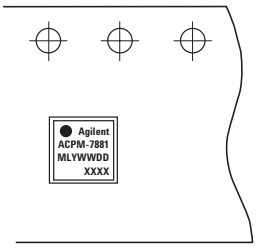
ACPM-7881 is a moisture sensitive component. It's important that the parts are handled under precaution and a proper manner. The handling, baking and out-of-pack storage conditions of the moisture sensitive components are described in IPC/JEDC S-STD-033A. Avago Technologies recommends utilizing the standard precautions listed below.

1. Calculated Shelf Life in Sealed Bag: 12 months at < 40°C and < 90% Relative Humidity (RH)
2. Peak Package Body Temperature: 250°C
3. After bag is opened, devices that will be subjected to reflow solder of other high temperature process must be:
   a. Mounted within 168 hours of factory condition ≤ 30°C / 60% RH
   b. Stored at <10% RH if not used
4. Devices require baking, before mounting if:
   a. Humidity indicator card is > 10% when read at 23 ± 5°C immediately after moisture barrier bag is opened.
   b. Items 3a or 3b is not met
5. If baking is required, please refer to J-STD-033 standard for low temperature (40°C) baking requirement in Tape/Reel form.

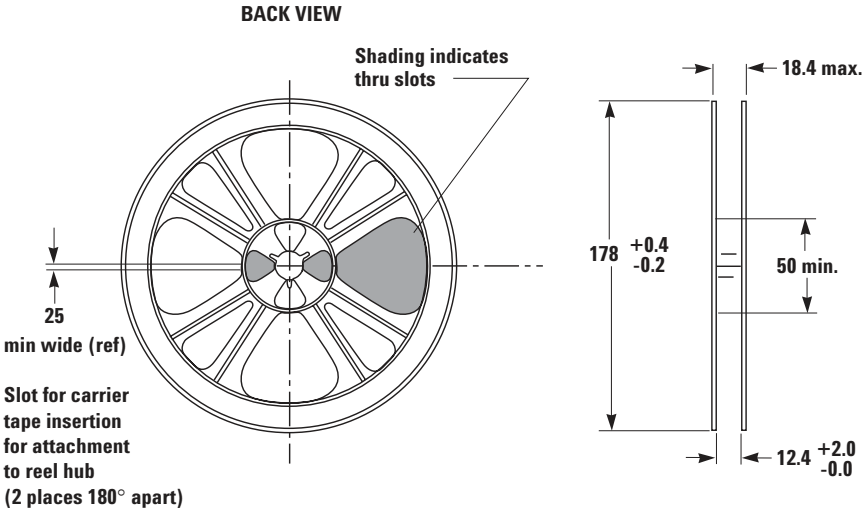
Tape Dimensions and Orientation

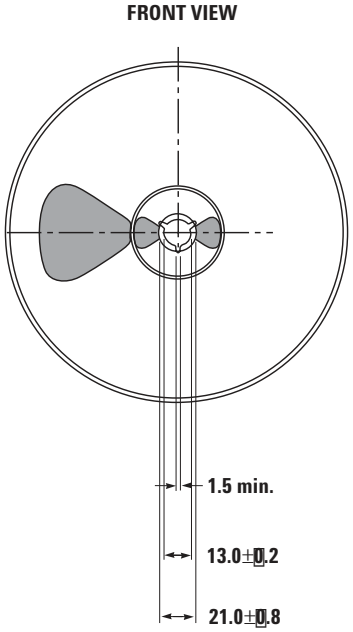


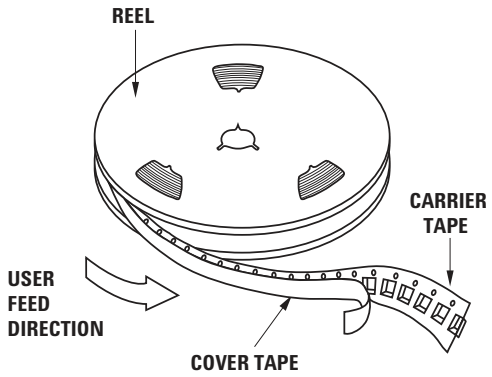
Notes:
1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ± 0.2 mm
3. All dimensions in millimeters unless otherwise stated.



Reel Dimensions and Orientation







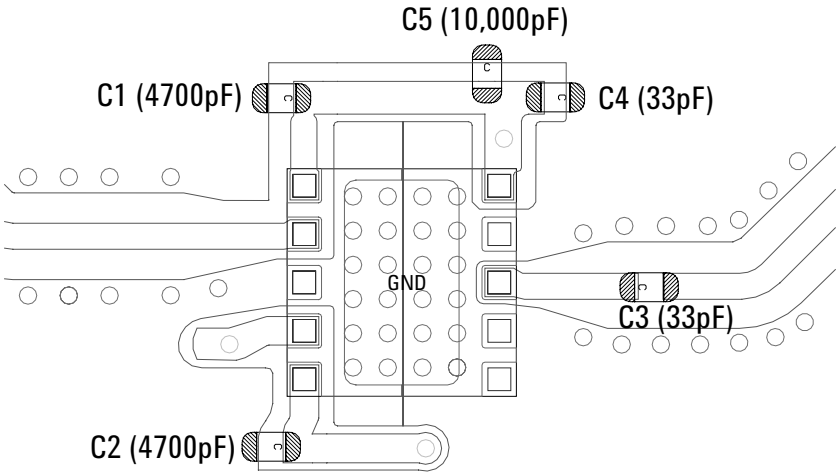
Notes:

1. Reel shall be labeled with the following information (as a minimum).
   a. manufacturers name or symbol
   b. Agilent Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance shall be issued and accompany each shipment of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm).

Order Information

Part Number	No. of Devices	Container
ACPM-7881-BLK	100	Bulk
ACPM-7881-TR1	1000	7″Tape and Reel

Suggested Board Implementation



Notes:

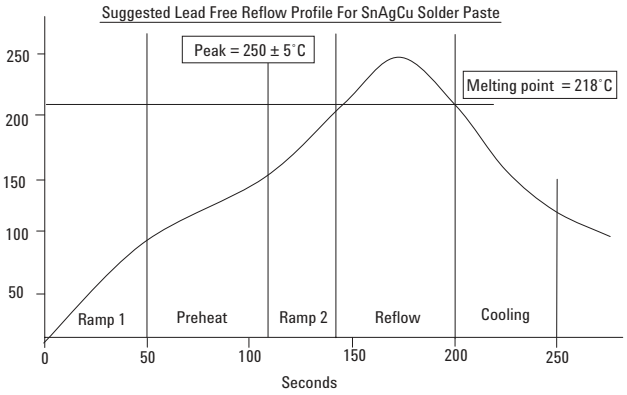
1. All decoupling capacitors should be placed as close to the power module as possible.
2. RFin (Pin 2) has a grounded inductor inside package as a matching element. An external series capacitor is needed if a DC voltage is present.
3. An additional battery bypass capacitor should be placed on bias line before the battery terminal, but does not need to be immediately adjacent to the PA module. The bypass capacitor should be a large value, nominally between 2.2uF and 4.7uF.
4. Trace impedance on RF lines should be 50Ω.

Solder Reflow Profile

The most commonly used solder reflow method is accomplished in a belt furnace using convection heat transfer. This profile is designed to ensure reliable finished joints. However, the profile indicated will vary among different solder pastes from different manufacturers and is shown here for reference only.

Other factors that can affect the profile include the density and types of components on the board, type of solder used and type of board or substrate material being used. The profile shows the actual temperature that should occur on the surface of a test board at or near the central of the solder joint. For this type of reflow soldering, the circuit board and solder joints are first to get heated up. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs thermal energy efficiently and distributes this heat to the components.

Reflow temperature profiles designed for tin/lead alloys will need to be revised accordingly to cater for the melting point of the lead free solder being 34°C (54°F) higher than that of tin/lead eutectic or near-eutectic alloys. In addition, the surface tension of molten lead free solder alloys is significantly higher than the surface tension for tin/lead alloys and this can reduce the spread of lead free solder during reflow.



Lead Free Reflow Profile General Guidelines

i. Ramp 1

Ramp to 100°C. Maximum slope for this zone is limited to 2°C/sec. Faster heating with ramp higher than 2°C may result in excessive solder balling and slump.

ii. Preheat

Preheat setting should range from 100 to 150°C over a period of 60 to 120 seconds depending on the characteristics of the PCB components and the thermal characteristics of the oven. If possible, do not prolong preheat as it will cause excessive oxidation to occur to the solder powder surface.

iii. Ramp 2

The time in this zone should be kept below 35 seconds to reduce the risk of flux exhaustion. The ramp up rate should be 2°C/sec from 150°C to re-flow at 217°C. It is important that the flux medium retains its activity during this phase to ensure the complete coalescence of the solder particles during re-flow.

iv. Reflow

The peak reflow temperature is calculated by adding ~32°C to the melting point of the alloy. Lead free solder paste melts at 218°C and peak reflow temperature is 218°C + 32°C = 250°C (±5°C). Note that total time over 218°C is critical and should typically be 60 – 150 seconds. This period determines the appearance of the solder joints. Excessive time above reflow may cause a dull finish and charred of flux residues. Insufficient time above reflow may lead to poor wetting and improperly fused (cloudy) flux residues.

v. Cooling

Maximum slope for cooling is limited to 3°C/sec. More rapid cooling may cause solder joints crack while cooling at a slower rate will increase the likelihood of a crystalline appearance on the solder joints (dull finish).

PCB Design Guidelines

The recommended ACPM-7881 PCB land pattern is shown in Figure 16. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding / bridging.

Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 17. The stencil has a solder paste deposition opening that is approximately 80% of the PCB pad. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100mm (4 mils) or 0.127mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline. The combined PCB and stencil layout is shown in Figure 18.

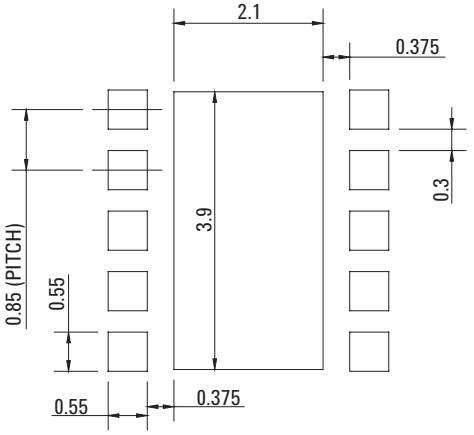


Figure 16. PCB land pattern (dimensions in mm)

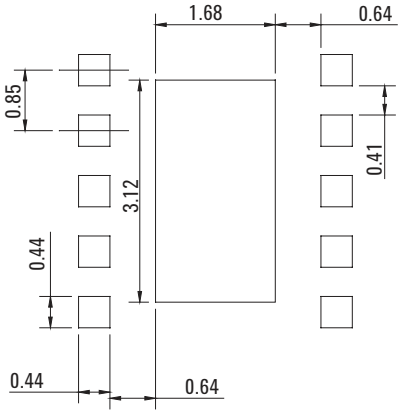


Figure 17. Stencil outline drawing (dimensions in mm)

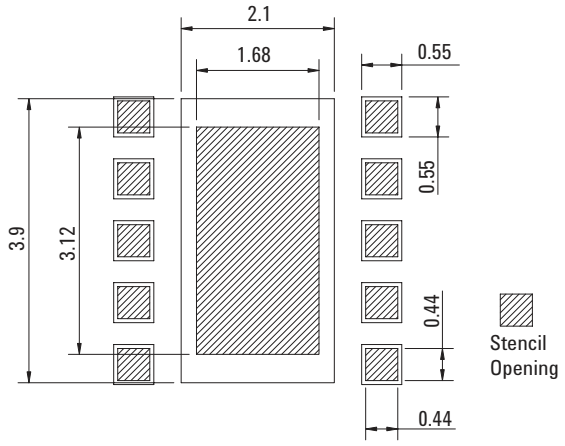


Figure 18. Combined PCB and stencil layouts (dimensions in mm)

Solder Paste Recommendation

The ACPM-7881 package is a lead free package that was proven to pass MSL3 when reflowed under lead free solder reflow profile. The recommended lead free solder for SMT reflow is Sn-Ag-Cu (95.5% Tin, 3.8% Silver, 0.7% Copper) or other similar Sn-Ag-Cu solders. This lead free solder paste has a melting point of 218°C (423°F), the ternary eutectic of Sn-Ag-Cu system, giving it the advantage of being the lowest melting lead free alternative. This temperature is still low enough to protect from damaging the internal circuitry during solder reflow operations provided the exposure time at peak reflow temperatures is not too excessive.

In certain situations, the designer may use leaded solder paste for reflow. The recommended solder for mounting ACPM-7881 package is Sn63 (63% Sn, 37% Pb). It is a eutectic compound with a typical melting point of 183°C.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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