19-1667; Rev 0; 4/00

MAXIM

1.8GHz to 2.5GHz Direct Downconversion Receivers

General Description

The MAX2700/MAX2701 are highly integrated direct downconversion (zero-IF) receivers designed for wideband wireless local loop (WLL) systems operating in the 1.8GHz to 2.5GHz band. The MAX2700/MAX2701s' zero-IF architecture eliminates the need for IF downconversion stages and the use of an IF SAW filter. This reduces the overall receiver cost by reducing the component count and required board space.

The MAX2700/MAX2701 have three main blocks: low-noise amplifier (LNA), quadrature downconverter, and baseband variable gain amplifiers (VGAs). The LNA is a single-ended amplifier with selectable gain and shutdown options. It provides a high input third-order intercept point (IP3), which reduces cross-modulation and gain compression due to high-level RF interference. The quadrature downconverter section consists of two highly linear double-balanced mixers driven by an external local oscillator (LO) with a selectable LO doubler. The double-balanced mixers are optimized to provide high input IP3 and minimum added noise. The mixers' high input second-order intercept point (IIP2) helps minimize receiver desensitization due to high-level AM-modulated interferers.

The two baseband VGAs in each channel provide 80dB of total maximum gain and greater than 60dB of gain control. The first AGC amplifier is optimized for low noise, low power dissipation, and high linearity over the entire gain range to ensure high gain compression performance. An external lowpass filter between baseband VGAs provides the required channel selectivity at the adjacent channel. An integrated gain offset correction loop circuit provides <0.3dB amplitude mismatch between the I and Q channels.

The MAX2700/MAX2701 operate from a single +2.7V to +3.3V power supply, drawing only 165mA of supply current and 20µA in shutdown mode. Both devices are available in small 48-pin TQFP packages with exposed paddle (EP) for optimum high-frequency performance.

Applications

Wireless Local Loop

Wideband Direct-Sequence Spread-Spectrum Systems

Two-Way MMDS

Wideband 2.4GHz ISM Radios

Digital Microwave Radios

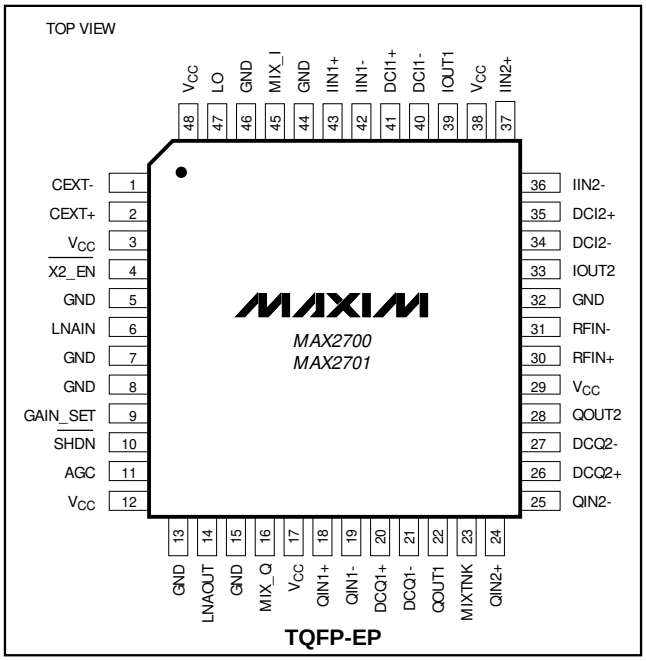
Features

- **Input Frequency Range**
  1.8GHz to 2.1GHz (MAX2700)
  2.1GHz to 2.5GHz (MAX2701)
- **Cascaded Performance at 1960 MHz**
  3.5dB Noise Figure
  -7.5dBm Input IP3 at Maximum Gain
- **LNA with Selectable Gain and Shutdown Option**
- **High Linearity Direct I/Q Downconverter**
- **Wideband LO Quadrature Generator**
- **3dB Baseband Channel Bandwidth of At Least 56MHz**
- **Variable Gain Baseband Amplifiers with >60dB Control Range**
- **Baseband Gain Offset Correction Loop**
- **+2.7V to +3.3V Single-Supply Operation**
- **Small 48-pin TQFP-EP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2700ECM	-40°C to 85°C	48 TQFP-EP
MAX2701ECM	-40°C to 85°C	48 TQFP-EP

Pin Configuration



TQFP-EP

1.8GHz to 2.5GHz Direct Downconversion Receivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
RF Signals
  P_{RFIN}, P_{LNAIN}, P_{LO} .....+15dBm
Baseband Signals
  IIN1+ to IIN1-, IIN2+ to IIN2-,
  QIN1+ to QIN1-, QIN2+ to QIN2- .....±2V
Input Voltages
  AGC, GAIN_SET, $\overline{SHDN}$, $\overline{X2\_EN}$,
  CEXT_, RFIN_, LO, LNAIN, IIN_ _,
  QIN_ _, DCI_ _, DCQ_ _ to GND .....-0.3V to (V_{CC} + 0.3V)
Input Current
  AGC.....±50mA
  All Digital Inputs.....±10mA
Continuous Power Dissipation (T_A = +70°C)
  48-Pin TQFP-EP (derate 27mW/°C above +70°C) 2000mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +2.7V to +3.3V, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, V_{AGC} = 1.25V, CEXT+ connected to CEXT-; no RF input signals applied; RFIN, LNAIN, LO inputs are terminated with 50Ω, LNAOUT connected to V_{CC} through a 10nH inductor; MIX_I, MIX_Q, QIN1+, QIN1-, QOUT1, IIN1+, IIN1-, IOUT1, QIN2+, QIN2-, QOUT2, IIN2+, IIN2-, IOUT2 pins are unconnected; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C.)

PARAMETERS	CONDITIONS			MIN	TYP	MAX	UNITS
SUPPLY							
Supply Voltage				2.7		3.3	V
Operating Supply Current	T_A = +25°C	LNA enabled	MAX2700		165	215	mA
			MAX2701		167	220	
		LNA disabled	MAX2700		155	200	
			MAX2701		156	205	
	T_A = -40°C to +85°C	LNA enabled	MAX2700			230	
			MAX2701			235	
		LNA disabled	MAX2700			210	
			MAX2701			215	
Shutdown Supply Current	$\overline{SHDN}$ = GND, V_{AGC} = 0.5V				20	100	µA
CONTROL INPUTS/OUTPUTS							
Input Logic Voltage High				2			V
Input Logic Voltage Low						0.6	V
Input Bias Current	$\overline{SHDN}$, $\overline{X2\_EN}$, GAIN_SET			-1		0.5	µA
	AGC, +0.5 < V_{AGC} < +2.0V			-22		12	
	AGC, V_{AGC} = 0.5V, $\overline{SHDN}$ = GND			-2		2	
DC Output Voltage	MIX_I, MIX_Q				1.2		V
	IOUT1, QOUT1				1.1		
	IOUT2, QOUT2				1.25		

AC ELECTRICAL CHARACTERISTICS

(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
LNA STAGE						
Operating Frequency Range (Note 1)	MAX2700		1800		2100	MHz
	MAX2701		2100		2500	
Power Gain (Note 2)	MAX2700, f_{LNAIN} = 1960MHz	GAIN_SET = V_{CC}	13.5	17.1	19.5	dB
		GAIN_SET = GND	-7.5	-1.9	2	
	T_A = -40°C to 85°C	GAIN_SET = V_{CC}	13		20	
		GAIN_SET = GND	-8		2.5	
	MAX2701, f_{LNAIN} = 2400MHz	GAIN_SET = V_{CC}	13	16.5	18.5	
		GAIN_SET = GND	-6	-1.8	0.5	
	T_A = -40°C to 85°C	GAIN_SET = V_{CC}	12.5		19	
		GAIN_SET = GND	-6.5		1.0	
Noise Figure	MAX2700, f_{LNAIN} = 1960MHz	GAIN_SET = V_{CC}		2.0		dB
		GAIN_SET = GND		15.8		
	MAX2701, f_{LNAIN} = 2400MHz	GAIN_SET = V_{CC}		2.3		
		GAIN_SET = GND		16.7		
Input Third-Order Intercept (Note 3)	MAX2700, f_{LNAIN} = 1960MHz	GAIN_SET = V_{CC}		+2.7		dBm
		GAIN_SET = GND		+5.1		
	MAX2701, f_{LNAIN} = 2400MHz	GAIN_SET = V_{CC}		+3.8		
		GAIN_SET = GND		+4.3		
Reverse Isolation	1800MHz to 2500MHz, GAIN_SET = V_{CC} or GND			28		dB
Isolation	LNAIN to LO, f_{LNAIN} = 1800MHz to 2500MHz			30		dB
	LNAOUT to RFIN, f_{LNAIN} = 1800 MHz to 2500 MHz			44		
VSWR	At LNA input, with external matching circuit at LNAIN	MAX2700 GAIN_SET = V_{CC}		1.1		–
		GAIN_SET = GND		1.8		
		MAX2701 GAIN_SET = V_{CC}		1.3		
		GAIN_SET = GND		2.1		
	At LNA output, with external matching circuit at LNAOUT	MAX2700 GAIN_SET = V_{CC}		1.7		
		GAIN_SET = GND		1.6		
		MAX2701 GAIN_SET = V_{CC}		1.2		
		GAIN_SET = GND		1.4		
MIXER STAGE (Differential RF input to mixer I/Q outputs with external balun and matching circuit to 50Ω)						
Frequency Range (Notes 1, 2)	MAX2700		1800		2100	MHz
	MAX2701		2100		2500	
Voltage Gain	MAX2700, f_{RFIN} = 1960 MHz		16	19.3	21.5	dB
	MAX2701, f_{RFIN} = 2400 MHz		14.5	18.1	20	
DSB Noise Figure	MAX2700, f_{RFIN} = 1960MHz			11.0		dB
	MAX2701, f_{RFIN} = 2400MHz			12.8		

1.8GHz to 2.5GHz Direct Downconversion Receivers

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
Input Third-Order Intercept (Note 4)	MAX2700, f_{LO} = 980MHz			+6.3		dBm
	MAX2701, f_{LO} = 1200MHz			+6.5		
Input Second-Order Intercept (Note 5)	MAX2700			+28.3		dBm
	MAX2701			+38		
VSWR	With 50Ω external matching at RFIN+/ RFIN-	MAX2700		1.5		–
		MAX2701		1.2		
Isolation (RFIN to MIX_I/Q)	MAX2700	f_{RFIN} = 1800MHz to 2100MHz		35		dB
		f_{RFIN} ≤20MHz		28		
	MAX2701	f_{RFIN} = 2100MHz to 2500MHz		22		
		f_{RFIN} ≤20MHz		12		
Isolation (RFIN to LO)	MAX2700, f_{RFIN} = 1800MHz to 2100MHz			38		dB
	MAX2701, f_{RFIN} = 2100MHz to 2500MHz			45		
Isolation (LO to RFIN)	MAX2700	f_{LO} = 900MHz to 1050MHz, $\overline{X2\_EN}$ = GND		49		dB
		f_{LO} = 900MHz to 1050MHz, $\overline{X2\_EN}$ = GND, isolation at 2 x F_{LO}		43		
		f_{LO} = 1800MHz to 2100MHz, $\overline{X2\_EN}$ = V_{CC}		33		
	MAX2701	f_{LO} = 1050MHz to 1250MHz, $\overline{X2\_EN}$ = GND		60		
		f_{LO} = 1050MHz to 1250MHz, $\overline{X2\_EN}$ = GND, isolation at 2 x F_{LO}		44		
		f_{LO} = 2100MHz to 2500MHz, $\overline{X2\_EN}$ = V_{CC}		70		
Mixer Spurious Suppression	2 x LO - RF (Note 6)			60		dBc
Baseband Bandwidth	MIX_I/Q	-1dB bandwidth (Note 2)	37	69		MHz
		-3dB bandwidth		170		
Gain Mismatch	ΔG_V(I-Q) (between mixer I and Q channels)	Baseband frequency = 125kHz		0.1	0.7	dB
		Up to -1dB baseband width (Note 2)		0	0.7	

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
Group Delay	t_{gd}, RFIN to MIX_I/Q, frequency up to -1dB baseband width			1.8		ns
Differential Group Delay (Note 2)	Δt_{gd} (between mixer I and Q channels)				1	ns
Output Impedance	Z_{out}, MIX_I, MIX_Q, frequency up to -1dB baseband width			1.4		Ω
Mixer Output Level (Note 2)	MIX_I, MIX_Q, baseband output at -1dB compression point		1.4	2.1		Vp-p
LO DOUBLER, LO BUFFER, QUADRATURE GENERATOR						
LO Frequency Range (Notes 1, 2)	$\overline{X2\_EN}$ = GND	MAX2700	900		1050	MHz
		MAX2701	1050		1250	
	$\overline{X2\_EN}$ = V_{CC}	MAX2700	1800		2100	
		MAX2701	2100		2500	
LO Input Power (Note 7)	$\overline{X2\_EN}$ = V_{CC} or GND		-16	-13	-10	dBm
LO VSWR	MAX2700	f_{LO} = 900MHz to 1050MHz, $\overline{X2\_EN}$ = GND		2.0		–
		f_{LO} = 1800MHz to 2100MHz, $\overline{X2\_EN}$ = V_{CC}		1.8		
	MAX2701	f_{LO} = 1050MHz to 1250MHz, $\overline{X2\_EN}$ = GND		1.7		
		f_{LO} = 2100MHz to 2500MHz, $\overline{X2\_EN}$ = V_{CC}		2.0		
Quadrature Error	$\lvert\Delta\phi\rvert$, MIX_I to MIX_Q			1.5	4.5	degrees
BASEBAND STAGE 1 (IIN1 TO IOUT1, QIN1 TO QOUT1)						
Channel Bandwidth	-1dB bandwidth (Note 2)		14	26		MHz
	-3dB bandwidth			56		
Input Impedance	IIN1+, IIN1-, QIN1+, QIN1-, single-ended			1.9		kΩ
Input Impedance Mismatch	Between IIN1+ and QIN1+			4		Ω
Voltage Gain (G_V)	V_{AGC} = 0.5V		-1.5	2.2	6	dB
	V_{AGC} = 2.0V		37	40	42	
Voltage Gain Mismatch	Mismatch between IIN1 to IOUT1 and QIN1 to QOUT1, 0.5V < V_{AGC} < 2 V			0.2		dB
VGA1 Gain Slope	Guaranteed Monotonic over 0.5V < V_{AGC} < 2V, V_{AGC} = 1.25V			34		dB/V
Noise Figure	Z_S = 1.1kΩ (Note 8)	V_{AGC} = 2.0V		7.5		dB
		V_{AGC} = 0.5V		34		
Phase Shift (Note 2)	For 10dB of gain (with AGC)			0.5	0.9	degrees

1.8GHz to 2.5GHz Direct Downconversion Receivers

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
Group Delay	IIN1+ to IOUT1, up to -1dB frequency			1.6		ns
	QIN1+ to QOUT1, up to -1dB frequency			1.6		
Group Delay Mismatch (Note 2)	Between I and Q channel from 100kHz up to -1dB			0.3	1.3	ns
Output Impedance	IOUT1, QOUT1, up to -1dB bandwidth			7		Ω
Output Impedance Mismatch	Between IOUT1 and QOUT1, up to -1dB bandwidth			1		Ω
Output Voltage (Note 2)	At -1dB compression point, IOUT1, QOUT1		0.7	1.1		Vp-p
BASEBAND STAGE 2 (IIN2+ TO IOUT2, QIN2+ TO QOUT2)						
Channel Bandwidth	-1dB bandwidth (Note 2)		19	34		MHz
	-3dB bandwidth			63		
Input Impedance	IIN2+, IIN2-, QIN2+, QIN2-, single-ended			2.1		KΩ
Input Impedance Mismatch	Between IIN2+ and QIN2+			1.5		Ω
Voltage Gain (G_v)	V_{AGC} = 0.5V		-0.6	4.4	9.5	dB
	V_{AGC} = 2.0V		37	39	42	
Voltage Gain Mismatch (Note 2)	Mismatch between IIN2 to IOUT2 and QIN2 to QOUT2, 0.5V < V_{AGC} < 2V	Gain Correction Disabled		0.9		dB
		Gain Correction Enabled (2dB initial mismatch)		0.3		
VGA2 Gain Slope	Guaranteed monotonic over 0.5V < V_{AGC} <2V, V_{AGC} =1.25V			30		dB/V
Noise Figure	Z_S = 1.1kΩ	V_{AGC} = 2.0V		14		dB
		V_{AGC} = 0.5V		47		
Phase shift (Note 2)	For 10dB of gain			0.2	1.4	degrees
Group Delay	IIN2+ to IOUT2, QIN2+ to QOUT2, up to -1dB Frequency			1.7		ns
Group Delay Mismatch (Note 2)	Between I and Q channel from 100kHz up to -1dB frequency			0.2	2.0	ns
Output Impedance	IOUT2 , QOUT2, up to -1dB bandwidth			4.0		Ω
Output Impedance Mismatch	Between IOUT2 and QOUT2, up to -1 dB bandwidth			4.0		Ω
Output Voltage (Note 2)	At -1dB compression point, IOUT2 , QOUT2		1.2	1.9		Vp-p

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Ripple Rejection	V_{CC} = 3.0V + 100mV_{PP} frequency = 100 to 300kHz, V_{OUT} = 0.3Vp-p, (Note 9)	Mixer		57		dBc
		VGA1		35		
		VGA2		28		

Note 1: This is the recommended operating frequency range. The parts have been characterized over the specified frequency range. Operation outside this range is possible but not guaranteed.

Note 2: Guaranteed by design and characterization.

Note 3: LNA is matched at input and output to 50Ω; f_1 = 1960MHz, f_2 = 1965MHz for MAX2700; f_1 = 2400MHz, f_2 = 2405MHz for MAX2701; P_{IN} = -30dBm per tone.

Note 4: Mixer IIP3 test. For MAX2700, RFIN is matched to 50Ω at 1960MHz. At RFIN, apply f_1 = 1964.2MHz, f_2 = 1968.2MHz, P_{IN} = -25dBm per tone, and measure IM3 product power level at 200kHz. For MAX2701, RFIN is matched to 50Ω at 2400MHz. At RFIN, apply f_1 = 2404.2MHz, f_2 = 2408.2MHz, P_{IN} = -25dBm per tone, and measure IM3 product power level at 200kHz.

Note 5: Mixer IIP2 test. For MAX2700, RFIN is matched to 50Ω at 1960MHz. At RFIN, apply f_1 = 1964.2MHz, f_2 = 1968.2MHz, P_{IN} = -25dBm per tone, and measure IM2 product power level at 4MHz. For MAX2701, RFIN is matched to 50Ω at 2400MHz. At RFIN, apply f_1 = 2404.2MHz, f_2 = 2408.2MHz, P_{IN} = -25dBm per tone, and measure IM2 product power level at 4MHz.

Note 6: Mixer spurious attenuation response. Mixer is matched to 50Ω at 1800MHz and F_{LO} = 900MHz (LO doubler enabled). F_{RFIN} = 1801MHz, P_{RFIN} = -85dBm, F_{SPUR} = 3601.5MHz, P_{SPUR} = -60dBm. Measure IF at 1MHz and spurious at 1.5MHz at the output. For better than 38dBc spurious attenuation response, output spurious level should be at least 10dB lower than the IF signal level. In the (2 x LO) - (1 x RF) spurious product notation, LO denotes the frequency of the final LO driving the I/Q mixers inputs.

Note 7: Mixer gain specifications are production tested over LO power range.

Note 8: A filter output impedance of 1.1kΩ can directly drive the VGA inputs since there is minimal mismatch loss between source and VGA input impedance.

Note 9: Electrolytic bypass cap to V_{CC} not connected.

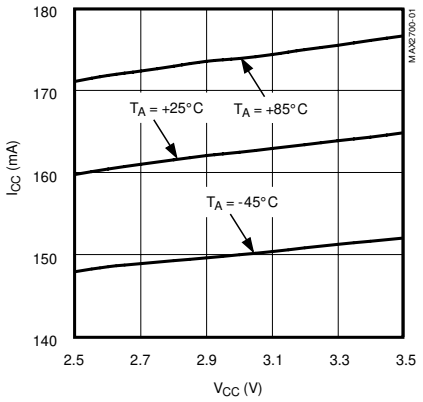
1.8GHz to 2.5GHz Direct Downconversion Receivers

Typical Operating Characteristics

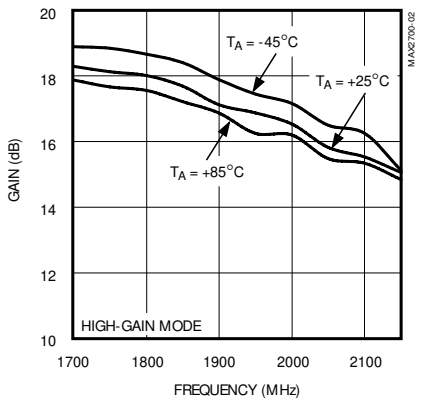
(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

MAX2700

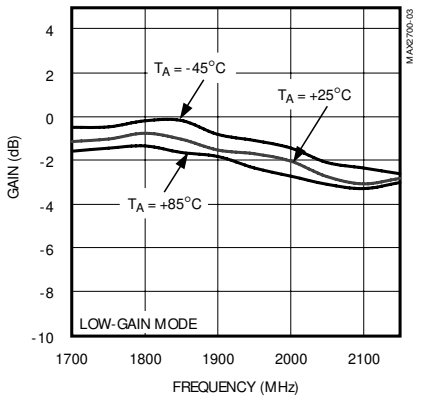
I_{CC} vs. V_{CC} vs. TEMPERATURE



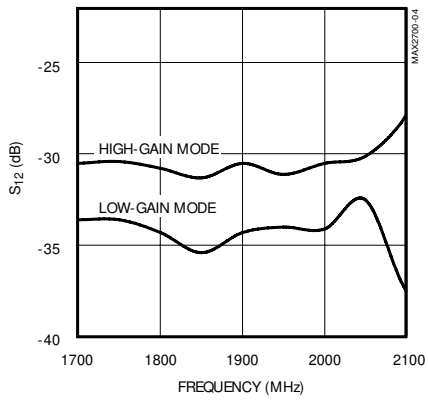
LNA GAIN vs. FREQUENCY vs. TEMPERATURE



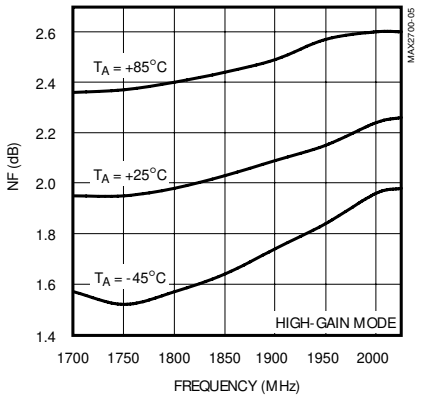
LNA GAIN vs. FREQUENCY vs. TEMPERATURE



LNA REVERSE ISOLATION vs. FREQUENCY vs. GAIN MODE



LNA NOISE FIGURE vs. FREQUENCY vs. TEMPERATURE

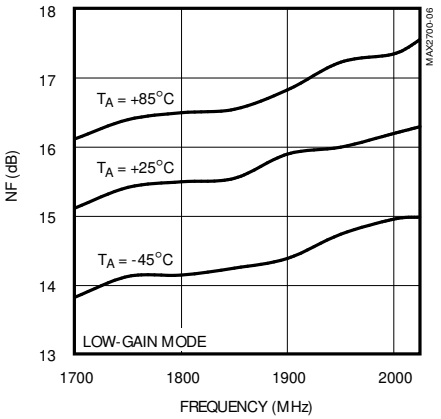


Typical Operating Characteristics (continued)

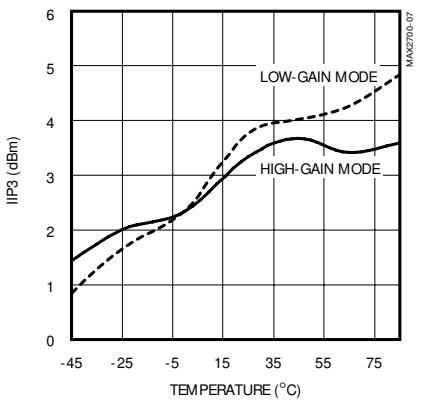
(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

MAX2700

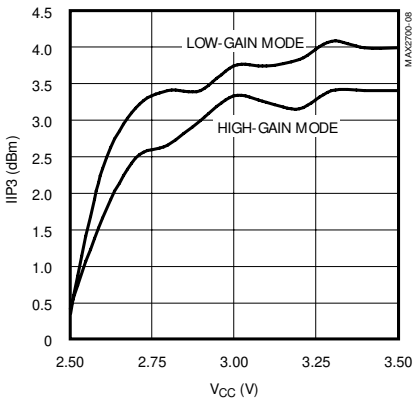
LNA NOISE FIGURE vs. FREQUENCY vs. TEMPERATURE



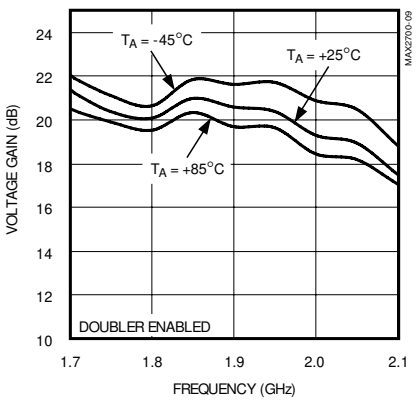
LNA IIP3 vs. TEMPERATURE



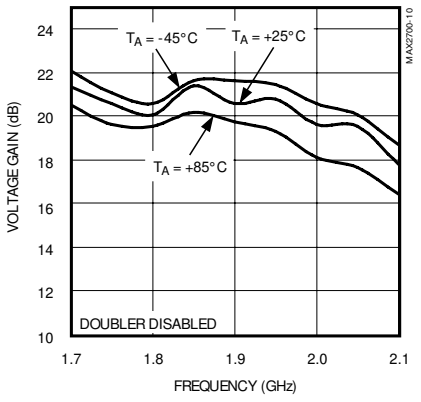
LNA IIP3 vs. V_{CC}



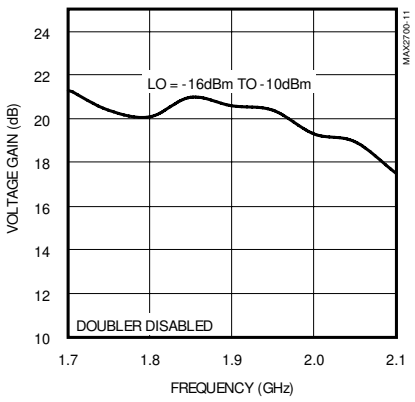
MIXER VOLTAGE GAIN vs. FREQUENCY vs. TEMPERATURE



MIXER VOLTAGE GAIN vs. FREQUENCY vs. TEMPERATURE



MIXER VOLTAGE GAIN vs. FREQUENCY vs. LO POWER



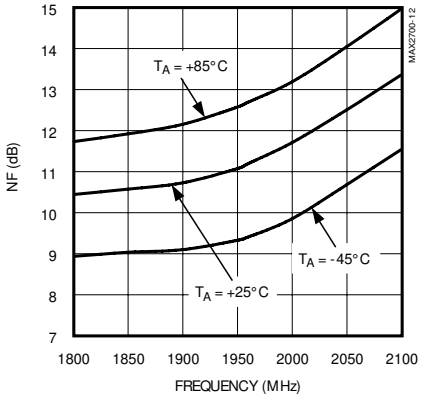
1.8GHz to 2.5GHz Direct Downconversion Receivers

Typical Operating Characteristics (continued)

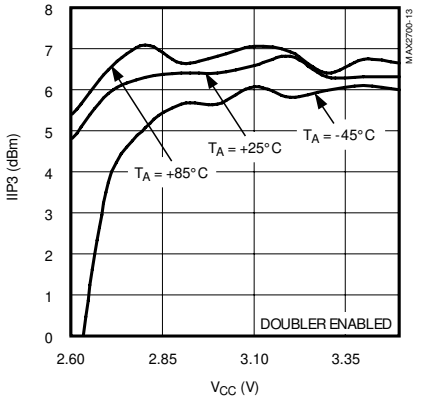
(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

MAX2700

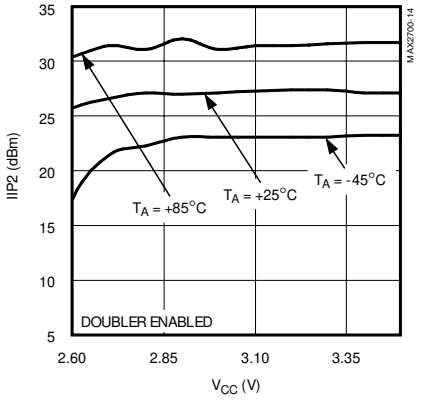
DSB MIXER NOISE FIGURE vs. FREQUENCY vs. TEMPERATURE



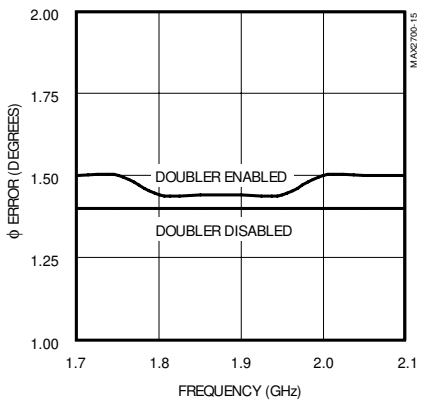
MIXER IIP3 vs. V_{CC} vs. TEMPERATURE



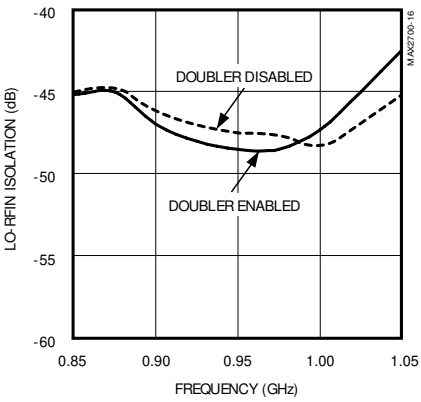
MIXER IIP2 vs. V_{CC} vs. TEMPERATURE



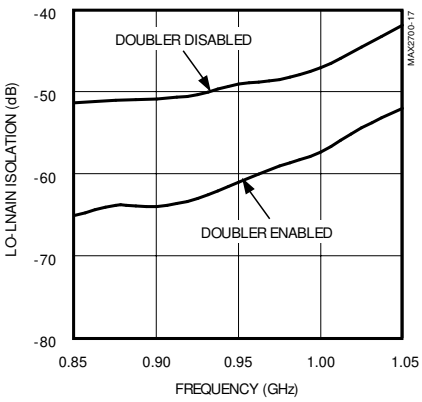
ϕ ERROR vs. LO FREQUENCY



LO-RFIN ISOLATION vs. LO FREQUENCY (INCLUDING BALUN)



LO-LNAIN ISOLATION vs. LO FREQUENCY

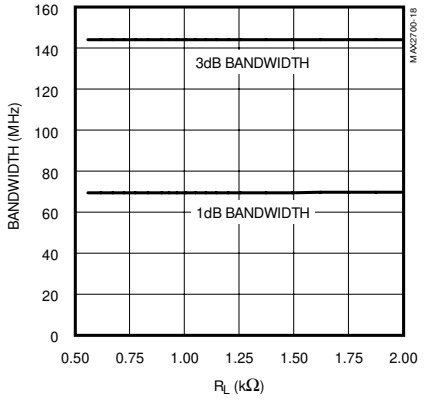


Typical Operating Characteristics (continued)

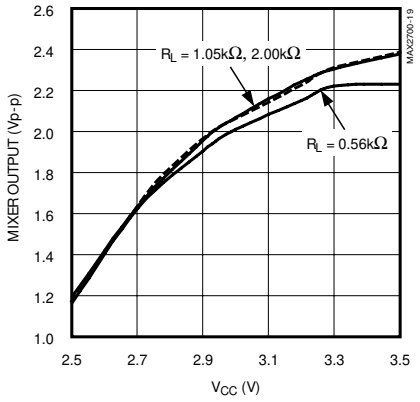
(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

MAX2700

MIXER BASEBAND BANDWIDTH vs. R_L

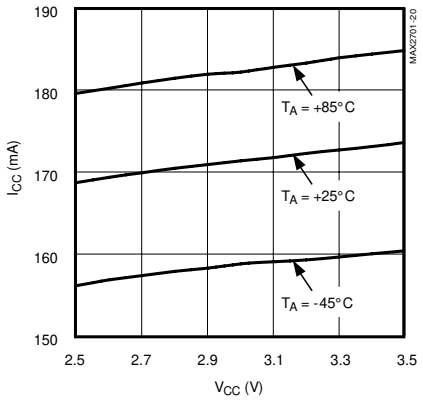


MIXER'S OUTPUT 1dB COMPRESSION POINT vs. V_{CC} vs. R_L

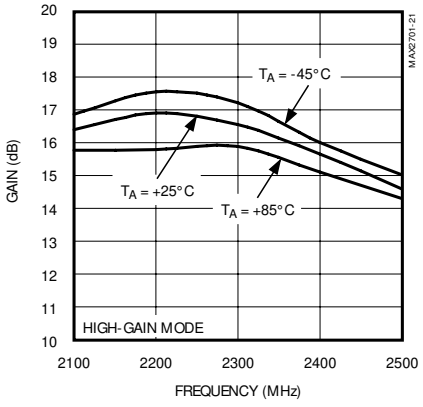


MAX2701

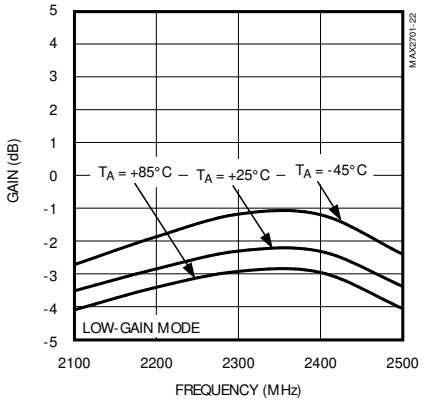
I_{CC} vs. V_{CC} vs. TEMPERATURE



LNA GAIN vs. FREQUENCY vs. TEMPERATURE



LNA GAIN vs. FREQUENCY vs. TEMPERATURE



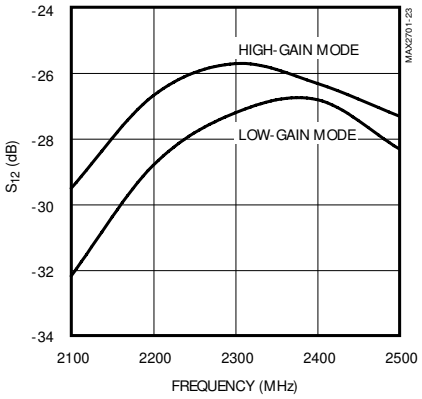
1.8GHz to 2.5GHz Direct Downconversion Receivers

Typical Operating Characteristics (continued)

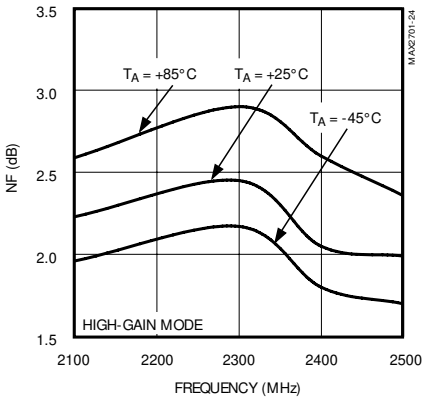
(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

MAX2701

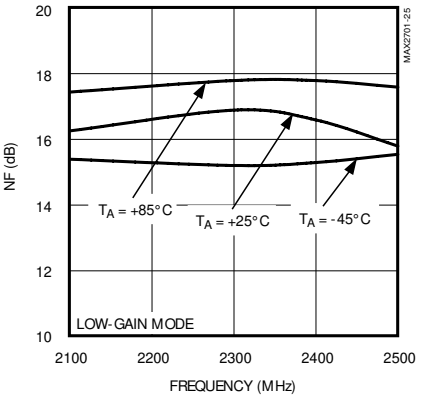
LNA REVERSE ISOLATION vs. FREQUENCY



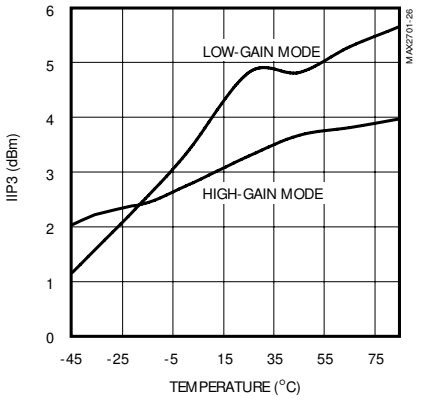
LNA NOISE FIGURE vs. FREQUENCY vs. TEMPERATURE



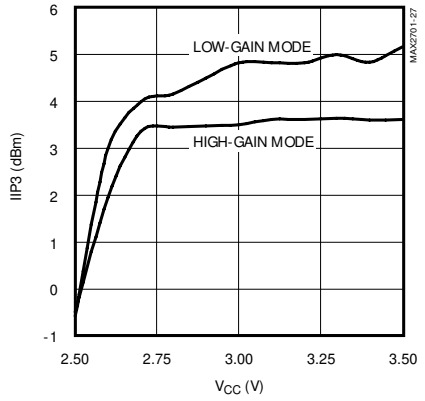
LNA NOISE FIGURE vs. FREQUENCY vs. TEMPERATURE



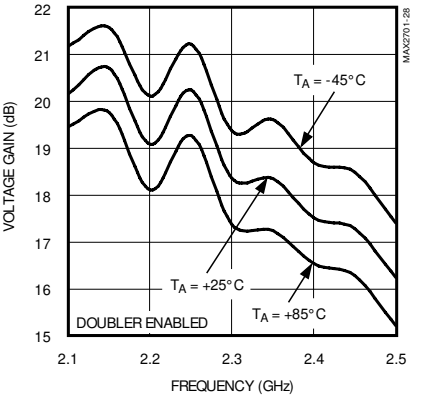
LNA IIP3 vs. TEMPERATURE



LNA IIP3 vs. V_{CC}



MIXER VOLTAGE GAIN vs. FREQUENCY vs. TEMPERATURE

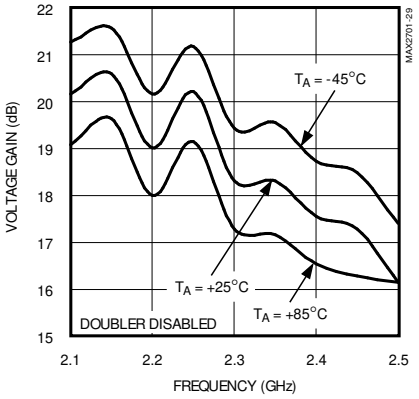


Typical Operating Characteristics (continued)

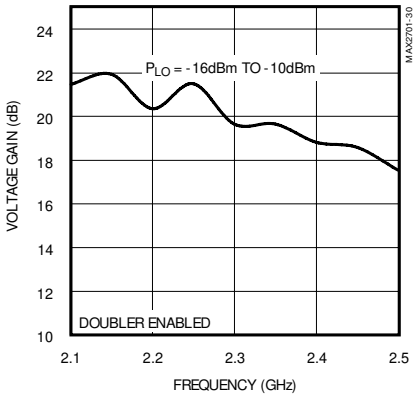
(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

MAX2701

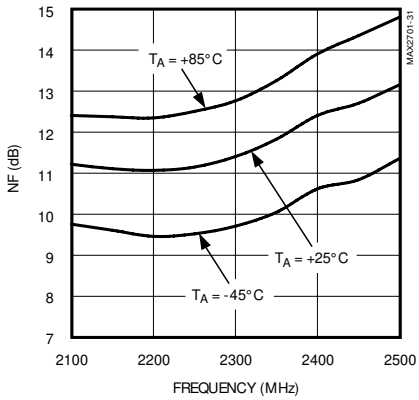
MIXER VOLTAGE GAIN vs. FREQUENCY vs. TEMPERATURE



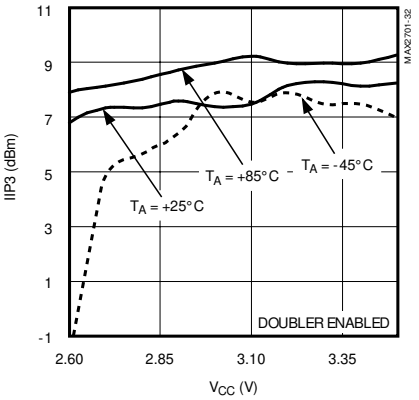
MIXER VOLTAGE GAIN vs. FREQUENCY vs. LO POWER



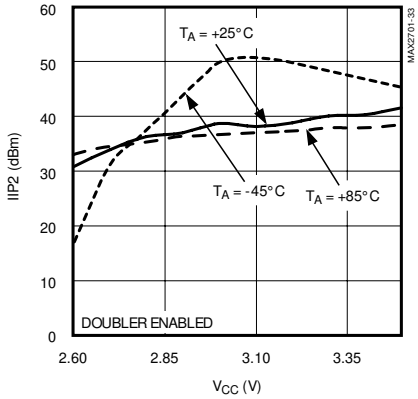
DSB MIXER NOISE FIGURE vs. FREQUENCY vs. TEMPERATURE



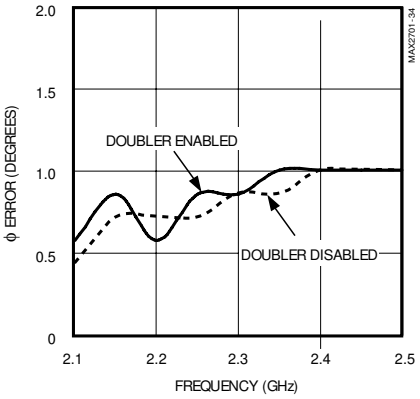
MIXER IIP3 vs. V_{CC} vs. TEMPERATURE



MIXER IIP2 vs. V_{CC} vs. TEMPERATURE



ϕ ERROR vs. LO FREQUENCY



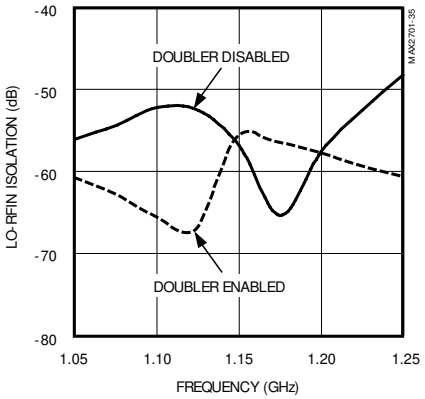
1.8GHz to 2.5GHz Direct Downconversion Receivers

Typical Operating Characteristics (continued)

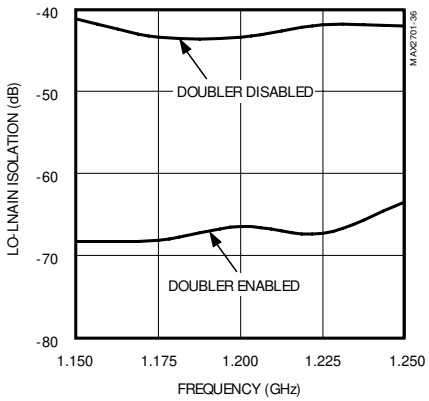
(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

MAX2701

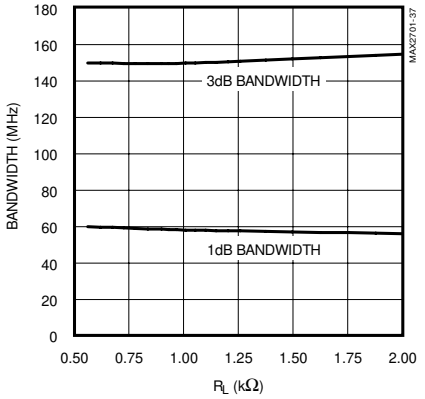
LO-RF ISOLATION vs. LO FREQUENCY (INCLUDING BALUN)



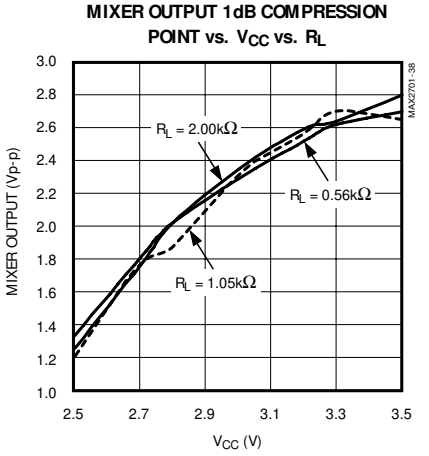
LO-LNAIN ISOLATION vs. LO FREQUENCY



MIXER BASEBAND BANDWIDTH vs. R_L



MIXER OUTPUT 1dB COMPRESSION POINT vs. V_{CC} vs. R_L

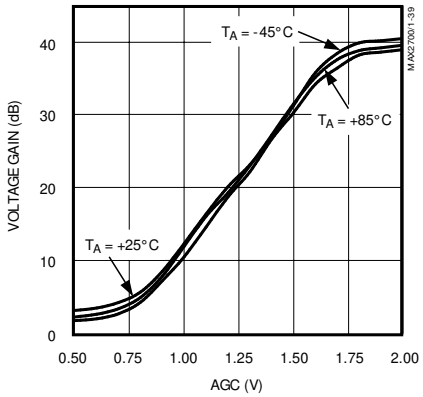


Typical Operating Characteristics (continued)

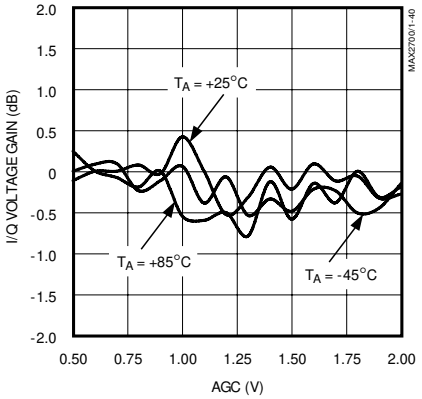
(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

MAX2700/MAX2701

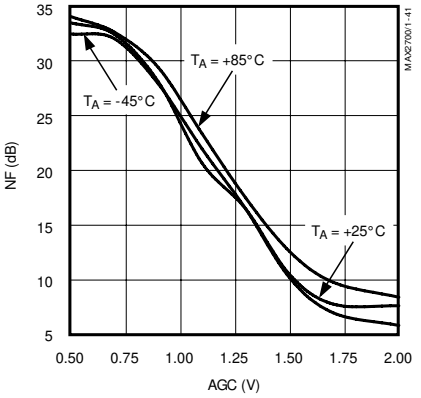
AGC VOLTAGE GAIN vs. AGC VOLTAGE vs. TEMPERATURE



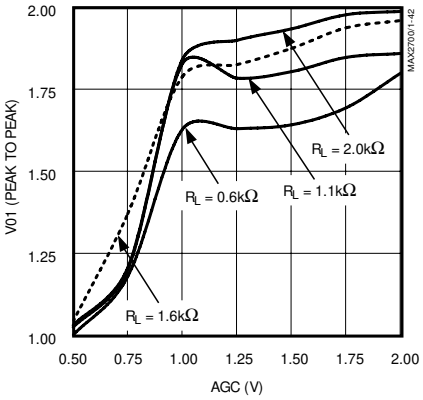
I/Q VOLTAGE GAIN MISMATCH vs. TEMPERATURE



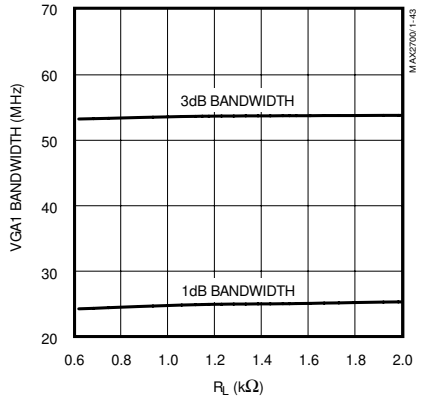
VGA1 NOISE FIGURE vs. AGC VOLTAGE vs. TEMPERATURE



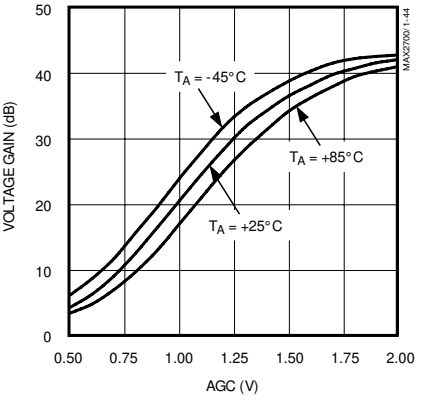
VGA1 VGA OUTPUT 1dB COMPRESSION POINT vs. AGC VOLTAGE vs. RL



VGA1 BANDWIDTH vs. R_L



VGA2 VOLTAGE GAIN vs. AGC VOLTAGE vs. TEMPERATURE



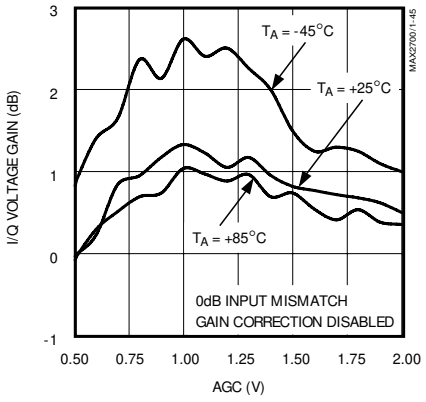
1.8GHz to 2.5GHz Direct Downconversion Receivers

Typical Operating Characteristics (continued)

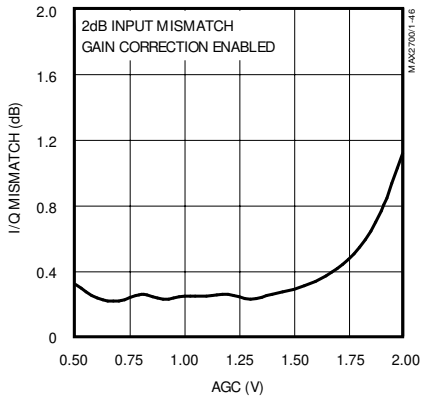
(MAX2700/MAX2701 EV kit (Figure 3), V_{CC} = +3.0V, T_A = +25°C, $\overline{SHDN}$ = GAIN_SET = V_{CC}, $\overline{X2\_EN}$ = GND, CEXT+ connected to CEXT-, P_{LO} = -13dBm, F_{LO} = 980MHz (MAX2700) and 1200MHz (MAX2701), P_{LNAIN} = -30dBm, P_{RFIN} = -25dBm, LNAIN and RFIN (single-ended input to balun) driven from 50Ω source, LNAOUT terminated into load; MIX_I, MIX_Q AC-coupled to 2kΩ load; IIN1+, QIN1+, IIN2+, QIN2+ driven from 1.1kΩ AC-coupled source; IOUT1, QOUT1 AC-coupled to 2kΩ; IOUT2, QOUT2 AC-coupled to 100Ω; input to VGAs, 20mVp-p at 1MHz tone, set V_{AGC} = 1.25V, unless otherwise noted.)

MAX2700/MAX2701

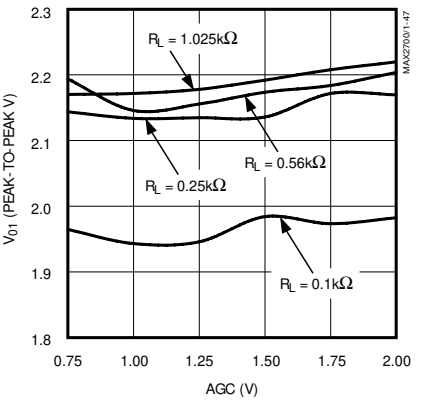
VGA2
I/Q VOLTAGE GAIN MISMATCH vs. TEMPERATURE



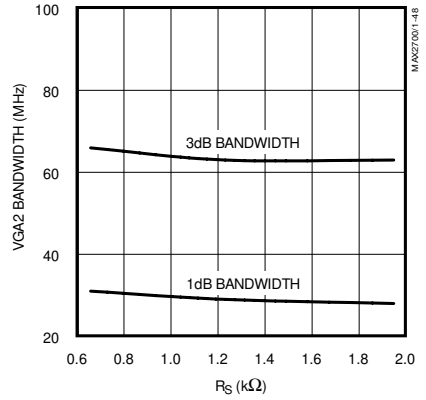
VGA2
I/Q VOLTAGE GAIN MISMATCH WITH GAIN CORRECTION



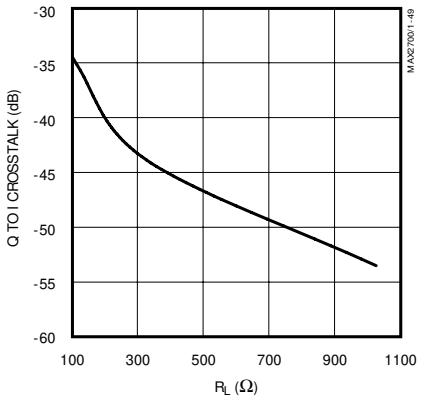
VGA2
VGA OUTPUT 1dB COMPRESSION POINT vs. AGC VOLTAGE vs. R_L



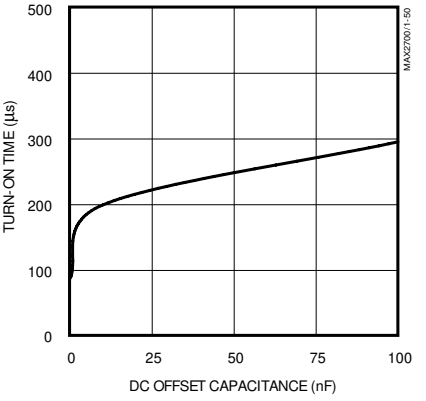
VGA2
BANDWIDTH vs. R_S



VGA2
Q TO I CROSSTALK vs. R_L



COMBINED VGA1 AND VGA2 TURN-ON TIME vs. DC OFFSET CAPACITANCE*



*C19, C23, C30, C36 in the EV kit schematic in Figure 3 represent DC offset capacitors.

Time from $\overline{SHDN}$ = GND to $\overline{SHDN}$ = V_{CC}, until DC quiescent point settles within 10% of static DC quiescent point.

Pin Description

PIN	NAME	FUNCTION
1	CEXT-	Inverting Input Port of VGA2 I/Q Gain Imbalance Correction Circuitry. Connect an external capacitor between CEXT- and CEXT+ to activate the circuit. Short CEXT- to CEXT+ to disable.
2	CEXT+	Noninverting Input Port of VGA2 I/Q Gain Imbalance Correction Circuitry. Connect an external capacitor between CEXT+ and CEXT- to activate the circuit. Short CEXT- to CEXT+ to disable.
3, 12, 17, 29, 38, 48	V_{CC}	Supply Voltage. Bypass V_{CC} to GND with capacitors as close to pin as possible.
4	$\overline{X2}\_\overline{EN}$	Logic-Level Enable for Doubler Circuitry. Drive logic low to turn on the doubler ($f_{LO} = f_{RFIN/2}$). Drive logic high to bypass the doubler ($f_{LO} = f_{RFIN}$).
5, 7, 8, 13, 15, 32, 44, 46	GND	Ground. Connect to ground plane with minimal inductance.
6	LNAIN	LNA Input. Connect to GND to turn the LNA off. Off-chip 50Ω match required.
9	GAIN_SET	LNA Gain Select Input. Drive logic high to select the high-gain mode. Drive logic low to select low-gain mode.
10	$\overline{SHDN}$	Shutdown Control Input. Drive logic low to enable shutdown mode.
11	AGC	Automatic Gain-Control Input for AGC. Bypass this pin with a 1000pF capacitor to GND to minimize coupling.
14	LNAOUT	LNA Output. This pin requires an external pullup inductor and off-chip 50Ω match.
16	MIX_Q	Mixer Q-Channel Baseband Output. Connect external series capacitor to AC-couple the output to the load.
18	QIN1+	Noninverting VGA1, Q-Channel Baseband Input
19	QIN1-	Inverting VGA1, Q-Channel Baseband Input
20	DCQ1+	Noninverting Offset Correction Input for Q-Channel VGA1 Amplifier
21	DCQ1-	Inverting Offset Correction Input for Q-Channel VGA1 Amplifier
22	QOUT1	Q-Channel VGA1 Amplifier Baseband Output
23	MIXTNK	Inductive Common-Mode Degeneration Pin for Mixer Stages
24	QIN2+	Noninverting VGA2, Q-Channel Baseband Input
25	QIN2-	Inverting VGA2, Q-Channel Baseband Input
26	DCQ2+	Noninverting Offset Correction Input for Q-Channel VGA2 Amplifier
27	DCQ2-	Inverting Offset Correction Input for Q-Channel VGA2 Amplifier
28	QOUT2	Q-Channel VGA2 Amplifier Baseband Output
30	RFIN+	I/Q Mixers Inverting Input. For narrow frequency bands between 1.8GHz and 2.5GHz, port must be matched using external matching components.

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Pin Description (continued)

PIN	NAME	FUNCTION
31	RFIN-	I/Q Mixers Noninverting Input. For narrow frequency bands between 1.8GHz and 2.5GHz, port must be matched using external matching components.
33	IOUT2	I-Channel VGA2 Baseband Output
34	DCI2-	Inverting Offset Correction Input for I-Channel VGA2 Amplifier
35	DCI2+	Noninverting Offset Correction Input for I-Channel VGA2 Amplifier
36	IIN2-	Inverting VGA2, I-Channel Baseband Input
37	IIN2+	Noninverting VGA2, I-Channel Baseband Input
39	IOUT1	I-Channel VGA1 Amplifier Baseband Output
40	DCI1-	Inverting Offset Correction Input for I-Channel VGA1 Amplifier
41	DCI1+	Noninverting Offset Correction Input for I-Channel VGA1 Amplifier
42	IIN1-	Inverting VGA1, I-Channel Baseband Input
43	IIN1+	Noninverting VGA1, I-Channel Baseband Input
45	MIX_I	Mixer I-Channel Baseband Output. Connect external series capacitor to AC-couple the output to the load.
47	LO	LO Input. Internally matched to 50Ω.

Detailed Description

The MAX2700/MAX2701 consist of five major blocks: LNA, I/Q direct demodulator, VGAs, gain correction, and bias circuits.

Low-Noise Amplifier

The LNA is a two-gain-level amplifier with low noise figure and high IIP3. Connect GAIN_SET to GND to switch the amplifier to a low-gain mode that provides an accurate gain step. High IIP3 minimizes the cross-modulation between TX power leakage and close-in interferers at the RX input. The LNA can be turned off independent of the other functional blocks by connecting LNAIN to GND. External matching is required to match the input and output to 50Ω. The LNA in Figures 1 and 2 is matched to 1960MHz and 2400MHz over a narrow bandwidth.

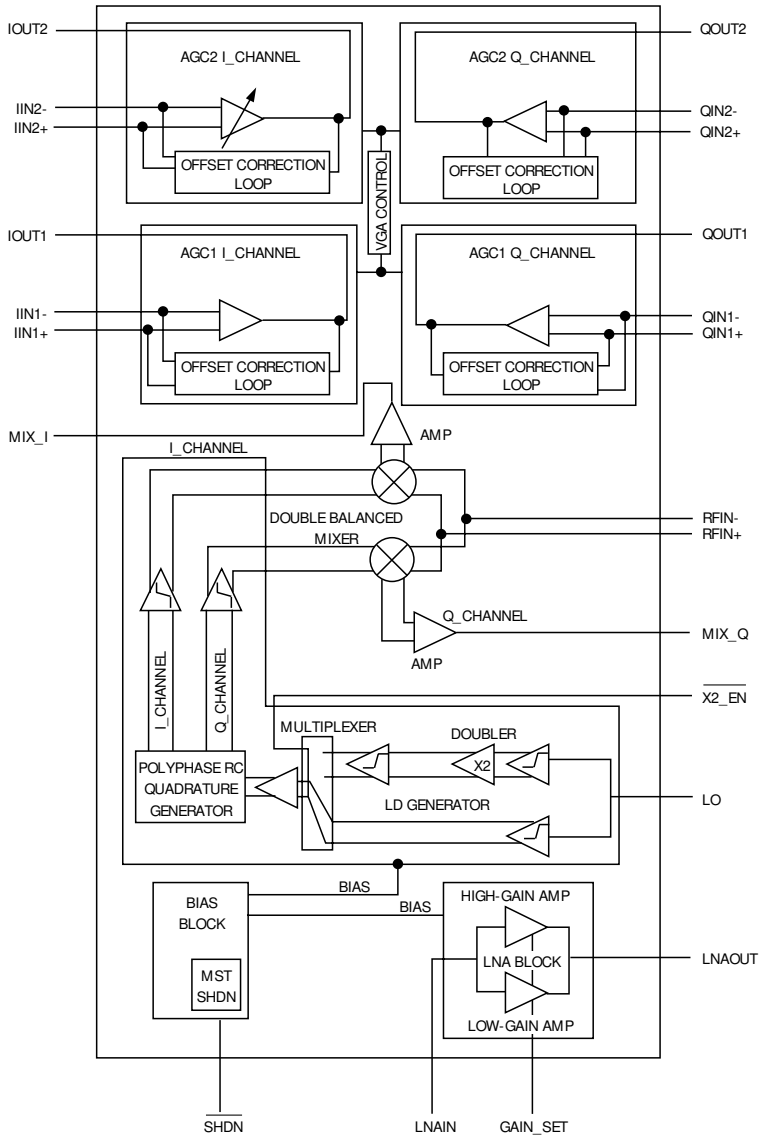
I/Q Demodulator

The direct I/Q demodulator downconverts the RF signal directly to baseband I and Q signals. This architecture's main advantage is that the received signal is amplified and filtered at baseband rather than at some high intermediate frequency. This eliminates the need for an expensive IF SAW filter and the IF oscillator. Furthermore, the direct conversion scheme eliminates the need for image rejection, thereby relaxing the bandpass filter selectivity requirements following the LNA. The direct downconverter consists of highly linear double-balanced I/Q mixers, an LO frequency doubler option, an LO quadrature generator, and baseband I/Q buffer amplifiers driven by the mixers' outputs.

In a direct downconversion receiver, I/Q mixers have more stringent requirements on mixer output linearity since they need to handle large voltage swings at baseband due to close-in interferers. The RF signal is applied to the differential input (RFIN+, RFIN-) of the direct downconversion receiver through an off-chip balun. The differential input structure results in a higher common-mode rejection for second-order nonlinearity generated in the receiver's front end. The differential input requires matching to appropriate impedance of the balun. Some applications may require a bandpass filter between the LNA and the mixer, as shown in Figures 1 and 2, to attenuate the residual transmit power leakage and out-of-band spurious signals.

The mixer baseband buffers amplify the mixer I and Q differential outputs and convert them to single-ended outputs (MIX_I, MIX_Q). These buffer amplifiers have

Functional Diagram



very low output impedance (<2Ω). The smallest load that should be used is 600Ω. At the output of the I/Q mixers' buffers, baseband lowpass filters should be used to provide adjacent and alternate channel selectivity. This reduces the level of adjacent channel and close-in interferers to the input of the following baseband amplifier.

The LO signal is applied externally to the LO input port. An LO doubler circuit doubles the LO signal frequency before it is applied to the mixer LO port. Connect $\overline{X2\_EN}$ to ground to enable the LO doubler circuit. With this circuit enabled, the required LO frequency is half that of the RF carrier frequency. Connect $\overline{X2\_EN}$ to V_{CC} to disable the frequency doubler circuit and the LO frequency is the same as the RF carrier frequency. The half LO frequency scheme results in the use of lower frequency and lower cost VCOs. It also reduces the LO leakage to the receiver's input. The mixer is guaranteed

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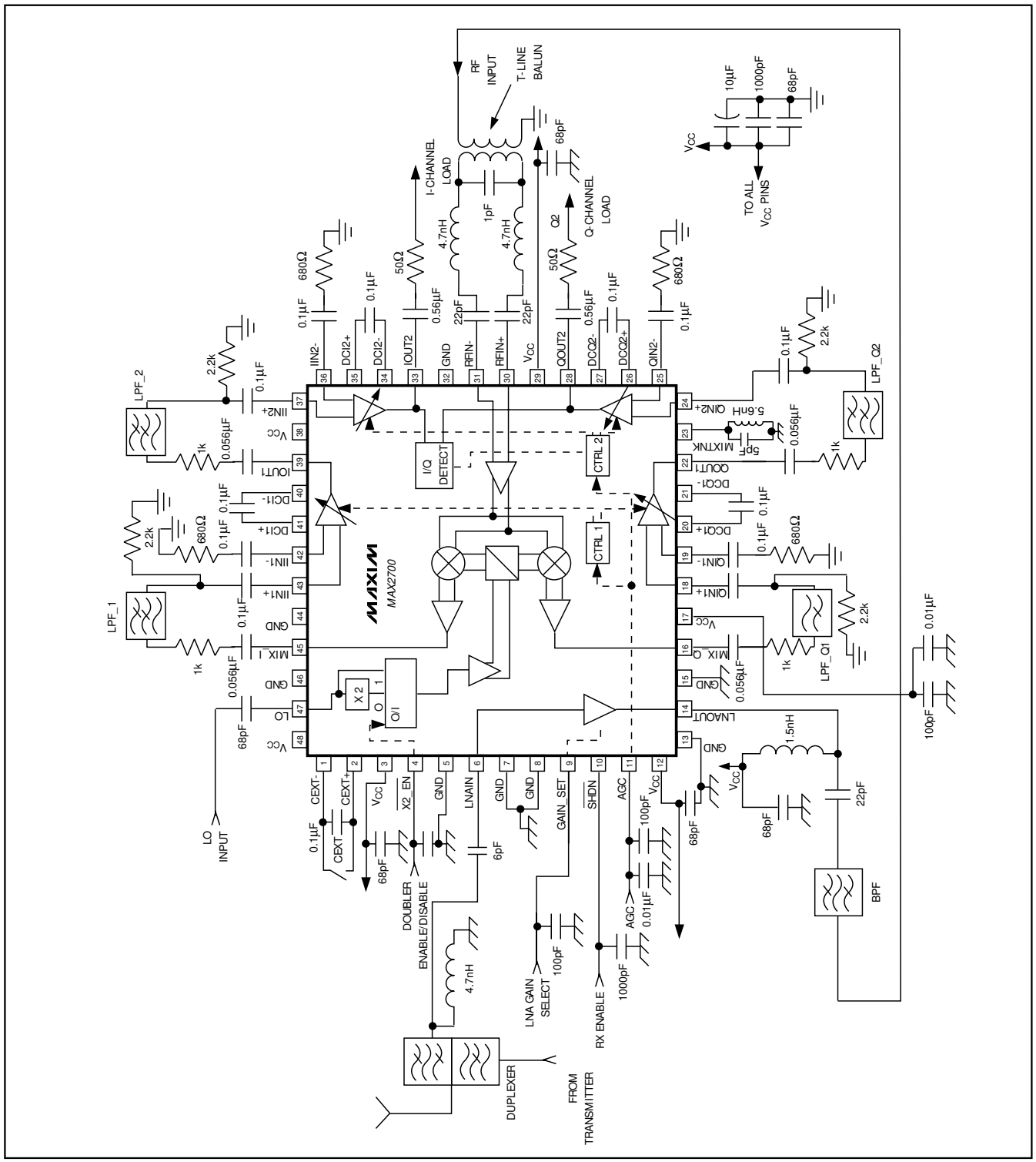

Figure 1. MAX2700 Typical Operating Circuit (1960MHz)

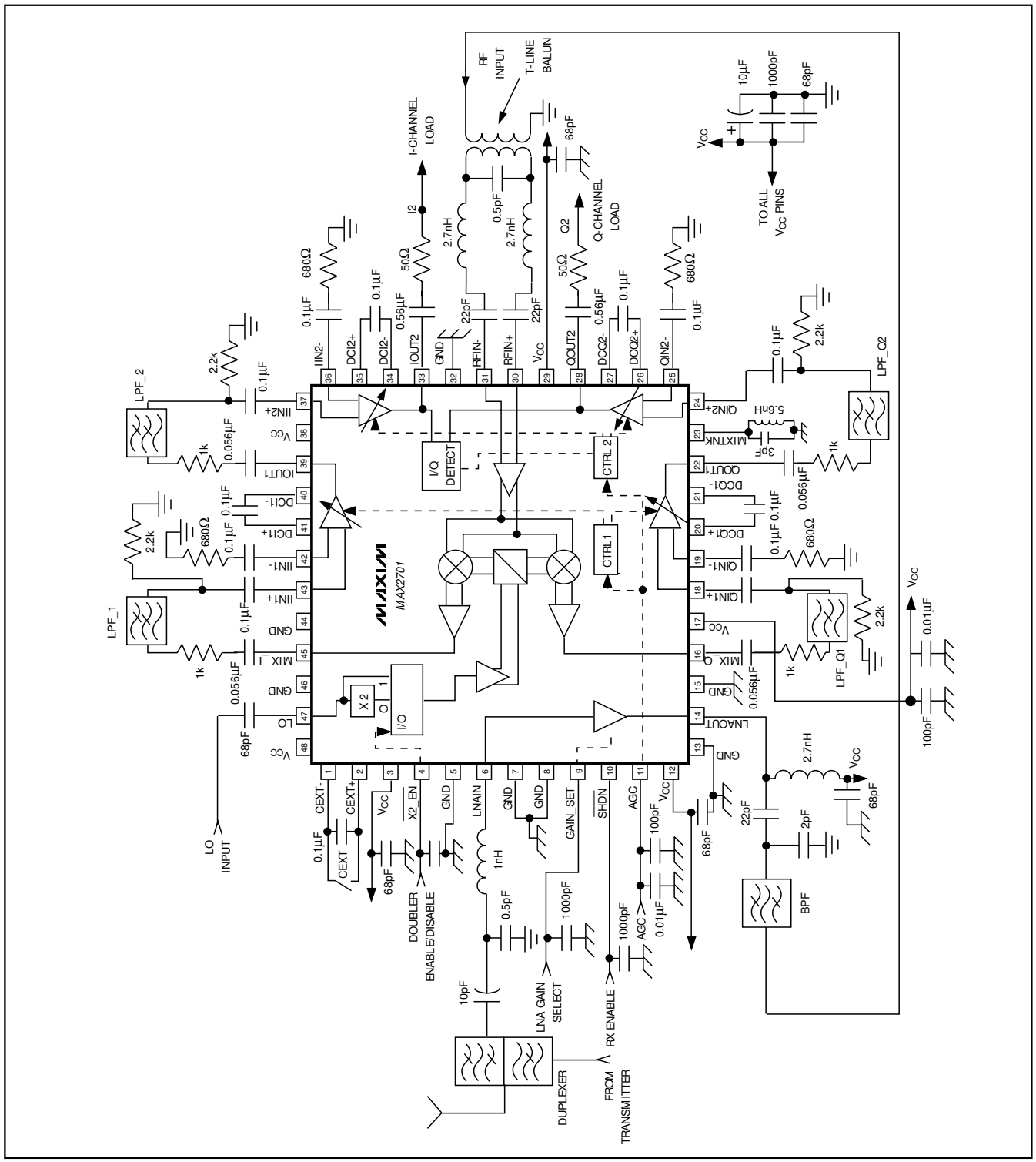

Figure 2. MAX2701 Typical Operating Circuit (2400MHz)

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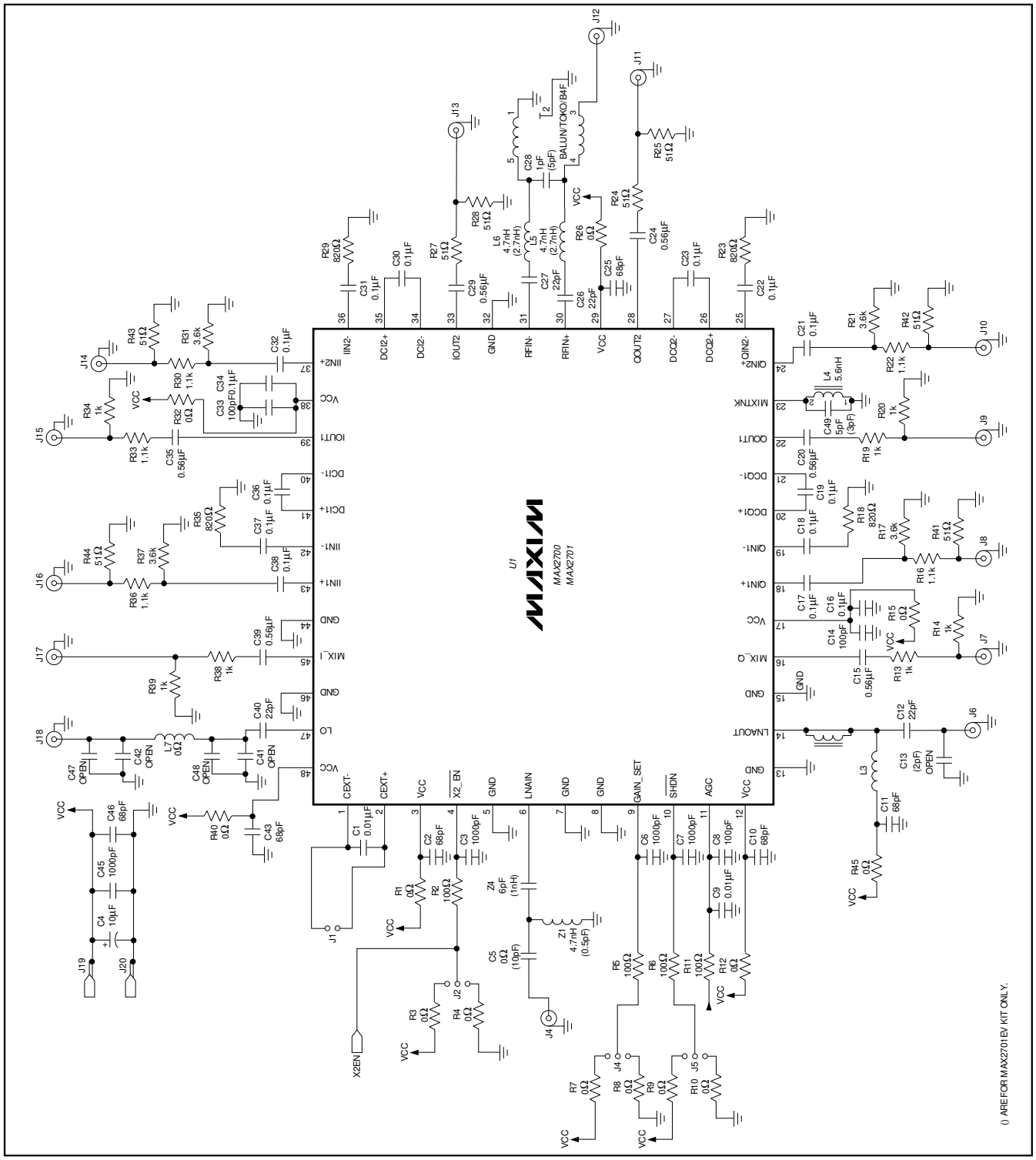

Figure 3. MAX2700/MAX2701 EV kit Schematic

to operate without degrading its performance over the LO power range of -10dBm to -16dBm. The quadrature generator consists of a wideband polyphase network. Each output of the polyphase filter is buffered, amplified, and then fed to the mixer's differential LO port.

Variable Gain Amplifier (VGA)

The AGC in each baseband channel I/Q is implemented by two variable gain amplifiers with equal gains. Each amplifier provides about 40dB voltage gain at the maximum setting and 30dB of gain control. The first baseband VGA (VGA1) is a cascaded wideband amplifier with differential input and single-ended output. It is optimized for low noise in the high-gain state and has low-power dissipation and sufficient linearity in all gain settings to ensure desired compression performance. The second baseband VGA (VGA2) is a multistage wideband amplifier with differential inputs and a single-ended output. In each channel, connect a baseband lowpass filter between VGA1 and VGA2 to provide additional channel selectivity at the adjacent channel. If the VGA amplifiers are driven single ended, the complementary input of VGA should be AC-coupled to ground through a matched source impedance.

VGA Offset Correction

An internal offset correction feedback amplifier associated with each VGA removes the DC offsets present in the VGAs. Offset correction preserves maximum output compression performance during maximum gain conditions. Each offset correction loop effectively AC-couples the associated VGA signal path. Each VGA1 network yields a highpass corner frequency according to the following:

$$f_{-3dB}\,(Hz) = 5300 / C_{DC}\,(nF)\ (V_{AGC} = 2.0V)$$

$$f_{-3dB}\,(Hz) = 700 / C_{DC}\,(nF)\ (V_{AGC} = 0.5V)$$

where C_{DC} is the value of the capacitors, in nanofarads, across DCI1+, DCI1- and DCQ1+, DCQ1-. Note that the corner frequency is a function of the gain setting, increasing with increasing gain. Each VGA2 network provides a highpass corner frequency predicted by the following:

$$f_{-3dB}\,(Hz) = 145 / C_{DC}\,(\mu F)$$

where C_{DC} is the value of the capacitors, in microfarads, across DCI2+, DCI2- and DCQ2+, DCQ2-.

The time constants associated with the offset correction networks limit turn-on time. For applications where the turn-on time is critical, the offset correction networks can be disabled by shorting the corresponding pins together (DCI1+ to DCI1-, DCQ1+ to DCQ1-, DCI2+ to DCI2-, and DCQ2+ to DCQ2-).

VGA2 I/Q Gain Mismatch Correction

The signal amplitudes at the outputs of the I- and Q-channel VGA2 amplifiers are compared, and any difference is corrected by a differential feedback network associated with the gain control circuitry. Differential amplitude information is extracted by use of a single external capacitor across pins 1 and 2 (CEXT- and CEXT+). The residual difference signal is amplified and fed back to the gain control network, increasing the gain of the channel with the smaller signal while decreasing the gain of the larger signal's channel. This network will correct amplitude mismatches generated by gain mismatches in the previous stages of the receiver (the mixer and VGA1), as well as insertion-loss mismatch. The correction network is capable of decreasing up to 2dB of amplitude mismatch at the inputs of the I/Q VGA2 amplifiers to <0.5dB amplitude mismatch. The gain correction network can be disabled by shorting CEXT- to CEXT+.

Bias Circuit

Operate the MAX2700/MAX2701 in shutdown mode by connecting $\overline{SHDN}$ to GND, reducing current consumption to 20µA. In shutdown mode, bias current to all the blocks is turned off through a master shutdown circuit. In applications where the LNA is not used, turn off the LNA by connecting the LNAIN to ground.

Applications Information

LNA Matching

The MAX2700/MAX2701 are designed to operate from 1.8GHz to 2.1GHz and 2.1GHz to 2.5GHz, respectively. The LNAs in Figures 1 and 2 are optimized for noise figure and gain centered around 1960MHz and 2400MHz, respectively. Operation at other frequencies in the band requires reoptimization of the input and output matching circuits. The noise figure is sensitive to input matching and losses in the input traces. LNA input matching should be optimized for desired noise figure, gain, and VSWR performance. High Q matching elements should be used at the LNA input. Proper board layout is essential to increase the isolation between LO and the LNA input. This minimizes LO leakage and thus DC offset.

I/Q Demodulator Input Matching

The RF input match of the I/Q demodulator in Figure 1 and 2 are optimized for 1960MHz and 2400MHz operation, respectively. For operation at a different frequency, the matching circuit should be reoptimized. Single-ended operation at the demodulator is achieved through the use of an off-chip balun transformer. In Figure 1, the balun, inductors, and capacitors constitute the matching circuit of the differential I/Q demodulator input.

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I/Q Mixer and VGA1 Output Load Requirements

To retain acceptable linearity performance, the mixer and VGA1 output loads should be >600Ω.

Layout Issues

A properly designed PC board is an essential part of any RF/microwave circuit. Use controlled impedance lines on all frequency inputs and outputs. Use low-inductance connections to ground on all ground pins and wherever the components are connected to ground. Place decoupling capacitors close to all V_{CC} connections. For proper chip operation, the metal paddle at the back of the chips must be grounded through via holes in the board.

Table 1. MAX2700 LNA S-Parameters High-Gain Mode (V_{CC} = 3.0V)

FREQUENCY (GHz)	|S11|	∠S11	|S21|	∠S21	|S12|	∠S12	|S22|	∠S22
1.70	0.542	-84.1	7.09	53.97	0.023	65.36	0.367	37.3
1.75	0.485	-82.9	7.412	41.4	0.025	46.6	0.286	11.4
1.80	0.471	-80.1	7.268	29.5	0.024	34.3	0.216	-23.1
1.85	0.466	-78.8	7.07	19.9	0.0243	29.6	0.185	-68.4
1.90	0.443	-79.2	6.977	10.1	0.025	22.5	0.217	-99.5
1.95	0.441	-79.3	6.635	0.2	0.025	13.8	0.306	-127
2.00	0.436	-84.8	6.115	-7.96	0.024	16.4	0.387	-152.8
2.05	0.324	-88.3	6.119	-13.47	0.0338	15.23	0.408	-165
2.10	0.288	-74.9	5.947	-22.7	0.0383	-4.813	0.476	-176.7
2.15	0.300	-66.7	5.687	-31.1	0.0387	-20.7	0.529	172
2.20	0.320	-63.1	5.31	-40.5	0.0384	-32.8	0.587	162.4

Table 2. MAX2700 LNA S-Parameters Low-Gain Mode (V_{CC} = 3.0V)

FREQUENCY (GHz)	|S11|	∠S11	|S21|	∠S21	|S12|	∠S12	|S22|	∠S22
1.70	0.637	-65.6	0.731	52.5	0.018	77	0.398	41.5
1.75	0.625	-66.3	0.763	42.9	0.018	52	0.328	21.8
1.80	0.622	-67.1	0.772	31.3	0.016	40	0.258	-7
1.85	0.618	-67.3	0.76	21.2	0.014	39	0.191	-45
1.90	0.617	-67	0.758	10.3	0.014	38	0.203	-79
1.95	0.617	-69.2	0.717	-1.1	0.015	34	0.238	-114
2.00	0.616	-70.1	0.678	-10.7	0.014	24	0.332	-141
2.05	0.611	-71.8	0.603	-13	0.022	37.6	0.323	-105
2.10	0.611	-74.5	0.634	-19.5	0.028	13.4	0.36	-170
2.15	0.61	-76.8	0.634	0.27	0.03	-5	0.402	-178
2.20	0.6	-80	0.621	-37	0.033	-14	0.484	174

Table 3. MAX2701 LNA S-Parameters High-Gain Mode (V_{CC} = 3.0V)

FREQUENCY (GHz)	|S11|	∠S11	|S21|	∠S21	|S12|	∠S12	|S22|	∠S22
2.10	0.303	-110	6.71	-32.9	0.036	-28.1	0.563	-162.5
2.15	0.283	-108	6.35	-42.7	0.04	-42.6	0.61	-178
2.20	0.269	-108	5.98	-49.8	0.042	-55	0.63	168.4
2.25	0.260	-109	5.7	-56.6	0.042	-67.4	0.64	155.4
2.30	0.254	-111	5.37	-63.4	0.043	-80	0.64	144
2.35	0.250	-114.6	5.08	-69.7	0.043	-92	0.632	134.4
2.40	0.241	-120	4.82	-75.7	0.04	-104	0.626	127
2.45	0.230	-129	4.55	-81.5	0.037	-114	0.625	121
2.50	0.218	-139	4.37	-87	0.035	-122	0.635	116

Table 4. MAX2701 LNA S-Parameters Low-Gain Mode (V_{CC} = 3.0V)

FREQUENCY (GHz)	|S11|	∠S11	|S21|	∠S21	|S12|	∠S12	|S22|	∠S22
2.10	0.589	-102.2	0.684	-36.2	0.025	-10.36	0.46	-157
2.15	0.59	-106.12	0.662	-45.2	0.029	-21.6	0.49	-172
2.20	0.591	-111.15	0.644	-52.8	0.032	-35.3	0.51	176.7
2.25	0.596	-117.3	0.63	-60.4	0.033	-50.4	0.54	165
2.30	0.594	-125.2	0.621	-69	0.036	-62.2	0.56	154.5
2.35	0.58	-134	0.608	-77.8	0.037	-76.5	0.58	145.2
2.40	0.548	-144	0.589	-87.8	0.038	-96	0.6	136.5
2.45	0.506	-154.4	0.556	-98	0.035	-109	0.62	129
2.50	0.469	-164	0.519	-107	0.029	-120	0.63	122

Table 5. MAX2700 Mixer RFIN+ Input S-Parameters (V_{CC} = 3.0V)

FREQUENCY (GHz)	|S11|	∠S11
1.70	0.612	-101.2
1.75	0.637	-105
1.80	0.624	-111.5
1.85	0.615	-116
1.90	0.607	-121
1.95	0.603	-128
2.00	0.598	-135

Table 6. MAX2701 Mixer RFIN+ Input S-Parameters (V_{CC} = 3.0V)

FREQUENCY (GHz)	|S11|	∠S11
2.10	0.590	-152
2.15	0.600	-161
2.20	0.604	-171
2.25	0.619	180
2.30	0.634	171
2.35	0.651	162.7
2.40	0.663	154
2.45	0.675	147
2.50	0.690	142

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Table 7. MAX2700 LO Input S-Parameters ($\overline{X2\_EN}$ = 1, $\overline{X2\_EN}$ = 0)

DOUBLER DISABLED $\overline{X2\_EN}$ = V_{CC}			DOUBLER ENABLED $\overline{X2\_EN}$ = 0		
FREQUENCY (GHz)	|S11|	∠S11	FREQUENCY (GHz)	|S11|	∠S11
1.70	0.03	92	850	0.479	-50.6
1.75	0.053	116	875	0.474	-50.1
1.80	0.086	123	900	0.466	-51.6
1.85	0.108	127	925	0.456	-52
1.90	0.135	128	950	0.442	-52
1.95	0.161	132	975	0.424	-53
2.00	0.186	136	1000	0.403	-53.6
—	—	—	1025	0.384	-54
—	—	—	1050	0.365	-54

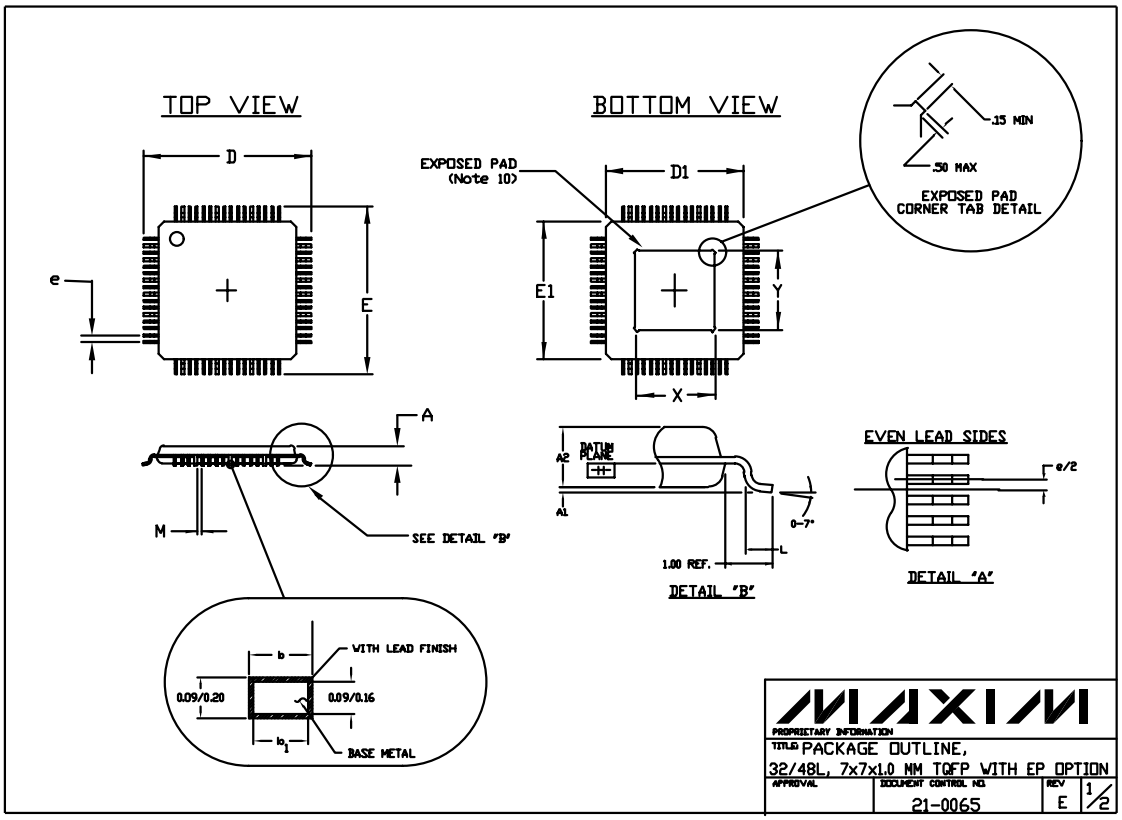
Table 8. MAX2701 LO Input S-Parameters ($\overline{X2\_EN}$ = 1, $\overline{X2\_EN}$ = 0)

DOUBLER DISABLED $\overline{X2\_EN}$ = V_{CC}			DOUBLER ENABLED $\overline{X2\_EN}$ = 0		
FREQUENCY (GHz)	|S11|	∠S11	FREQUENCY (GHz)	|S11|	∠S11
2.10	0.257	160	1.05	0.358	-53.4
2.15	0.279	164	1.10	0.341	-53
2.20	0.299	167	1.15	0.32	-52
2.25	0.314	171	1.20	0.299	-52
2.30	0.33	174	1.25	0.268	-51
2.35	0.347	178	—	—	—
2.40	0.357	-179	—	—	—
2.45	0.366	-175	—	—	—
2.50	0.373	-171	—	—	—

Chip Information

TRANSISTOR COUNT: 3307

Package Information



1.8GHz to 2.5GHz Direct Downconversion Receivers

Package Information (continued)

NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS AC AND AE.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS					
	AC			AE		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	~~~	~~~	1.20	~~~	~~~	1.20
A_1	0.05	0.10	0.15	0.05	0.10	0.15
A_2	0.95	1.00	1.05	0.95	1.00	1.05
D	9.00 BSC.			9.00 BSC.		
D_1	7.00 BSC.			7.00 BSC.		
E	9.00 BSC.			9.00 BSC.		
E_1	7.00 BSC.			7.00 BSC.		
L	0.45	0.60	0.75	0.45	0.60	0.75
N	0.15	~~~	~~~	0.14	~~~	~~~
N	32			48		
e	0.80 BSC.			0.50 BSC.		
b	0.30	0.37	0.45	0.17	0.22	0.27
b1	0.30	0.35	0.40	0.17	0.20	0.23
*X	3.20	3.50	3.80	3.70	4.00	4.30
*Y	3.20	3.50	3.80	3.70	4.00	4.30

* EXPOSED PAD (Note 10)

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.0 MM TQFP WITH EP OPTION
APPROVAL | DOCUMENT CONTROL NO. 21-0065 | REV E | 2/2