ALT80802

Wide Input Voltage, Adjustable Frequency, Buck-Boost or Buck 2 Amp LED Driver

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Supports buck-boost or buck mode operation
- Supply voltage from 3.8 to 50 V in buck mode
  - Handles automotive load dump and cold crank
  - Also supports buck mode from a pre-boost supply
- Supports up to 16 V output in buck-boost mode for 4 WLEDs
- 150 mΩ integrated MOSFET switch
- Programmable switching frequency up to 2.5 MHz for small solution size and operation above AM band
- Designed for low EMC with frequency dithering
- Integrated level shifting allows ground-referenced enable and fault flag in buck-boost mode
- PWM dimming via direct logic input or power supply voltage
- Robust protection against:
  - Adjacent pin-to-pin short
  - Pin-to-VSS (IC ground) short
  - Component open/short faults

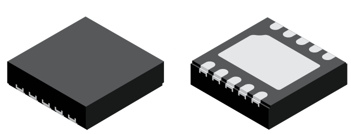
APPLICATIONS

Automotive lighting

- Daytime running lights
- Front and rear fog lights
- Turn/stop lights
- Map light
- Dimmable interior lights

PACKAGE:

10-Pin DFN with Exposed Thermal Pad and Wettable Flank (suffix EJ)



Not to scale

DESCRIPTION

The ALT80802 is a high-frequency switching regulator that provides constant output current to drive high-power LEDs. It integrates a power MOSFET for step-down or inverting buck-boost conversion. With current-mode control and simple external compensation, the ALT80802 can achieve fast transient response.

The wide input range of 3.8 to 50 V makes the ALT80802 suitable for a wide range of lighting applications, including those in an automotive input environment. The device rating also enables a simple solution for driving 3 to 4 WLEDs in buck-boost configuration—a very common application requirement for automotive lighting applications.

The ALT80802 is designed to aid in EMC/EMI design by frequency dithering, soft freewheel diode turn-off, and well-controlled switch node slew rates. A programmable oscillator allows the ALT80802 to switch outside EMI-sensitive frequency bands such as the AM band.

With current-mode control and simple external compensation, the ALT80802 can achieve fast transient response. The control loop of the ALT80802 is designed for PWM dimming operation to achieve low dimming on-time and low turn-on overshoot. In buck-boost operation, the ALT80802 reduces the current overshoot normally caused by right half plane zero effect during a PWM dimming turn-off transient.

Extensive protection features of the ALT80802 include pulse-by-pulse current limit, hiccup mode short-circuit protection, open/short freewheeling diode protection, BOOT open/short voltage protection, VIN undervoltage lockout, and thermal shutdown. Also, it includes internal clamp to prevent output voltage runaway if output LED string is opened in buck-boost operation.

The ALT80802 is available in industry-standard 10 pin DFN-package with thermal pad and wettable flank.

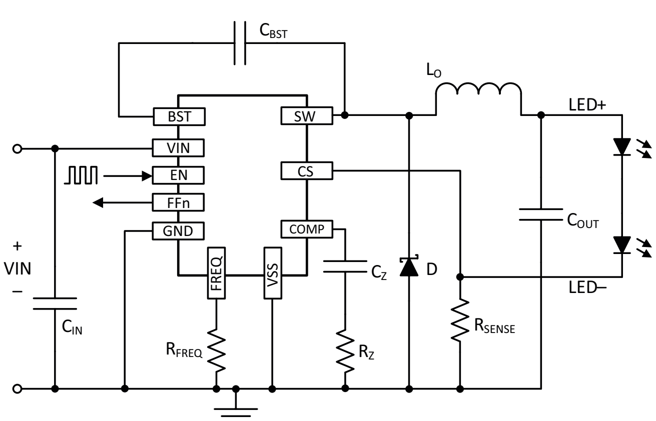


Figure 1: ALT80802 Buck Simplified Schematic

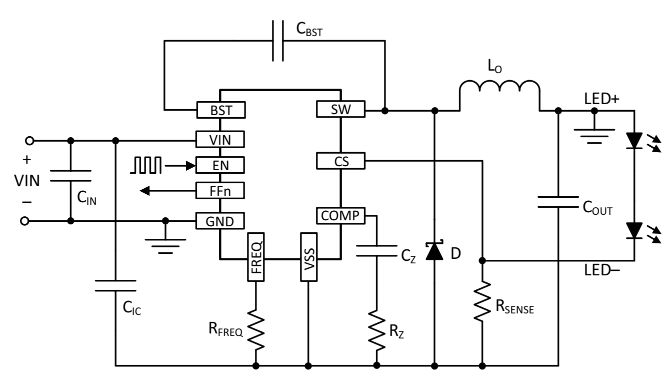


Figure 2: ALT80802 Buck-Boost Simplified Schematic

SPECIFICATIONS

SELECTION GUIDE

Part Number	Package	Packing [1]
ALT80802KEJJTR	10-pin DFN with thermal pad and wettable flank	1500 pieces per 7-inch reel

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
Input Voltage	V_{IN}	In Buck mode (VSS = GND)	−0.3 to 55	V
Switch Node Voltage	V_{SW}		−0.3 to V_{IN} + 0.3	V
		t < 250 ns	−1.5	V
		t < 50 ns	V_{IN} + 3	V
Bootstrap Pin to Switch Node	V_{BST-SW}		−0.3 to 6	V
VSS to GND	$V_{VSS-GND}$	Limits output to –20 V	–20 to 3	V
EN, FREQ, CS, FFn		With respect to VSS pin	−0.3 to V_{IN} + 0.3	V
All other pins		With respect to VSS pin	−0.3 to 6	V
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Test Conditions	Value	Unit
DC Input Voltage	V_{IN}	In Buck-Boost Mode (VSS below GND)	6 to 36	V
		In Buck Mode (VSS = GND)	6 to 50	V
Junction Temperature	T_J		−40 to 150	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	DFN-10 (EJ) package on 4-layer PCB based on JEDEC standard	45	°C/W

[3] Additional thermal information available on the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table of Contents

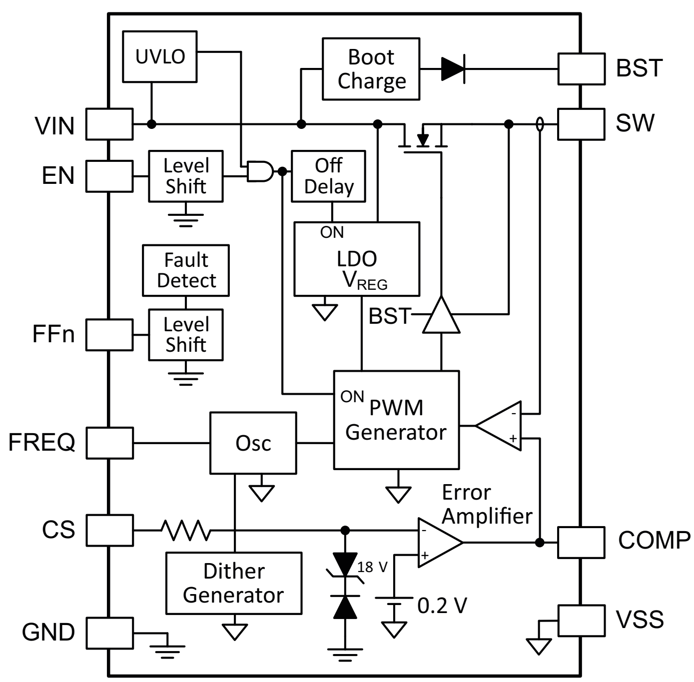
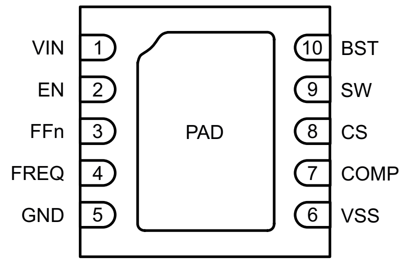


Figure 3: Functional Block Diagram

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PINOUT DIAGRAM AND TERMINAL LIST



Package EJ Pinouts

Terminal List Table

Pin Name	Pin Number	Description
VIN	1	Power input for the control circuits and the drain of the internal high-side N-channel MOSFET. Connect this pin to a power source. A high quality ceramic capacitor should be placed very close to this pin and GND.
EN	2	Input for Enable and PWM dimming; rated up to V_{IN} and logic-level compatible.
FFn	3	Open-drain fault flag output which is pulled low in case of fault. Connect through an external pull-up resistor to the desired level. This pin should be left open if not used.
FREQ	4	Frequency setting pin. A resistor, R_{FREQ}, from this pin to VSS sets the PWM switching frequency. See Table 2 to determine the value of R_{FREQ}.
GND	5	Enable and fault flag ground reference. Connect to input supply ground.
VSS	6	ALT80802 return. Connect to lowest circuit potential. This is input ground when configured as a buck converter and should be connected to the GND pin. It is the negative output when configured as a buck-boost converter. See typical application schematics for more detail.
COMP	7	Output of the error amplifier and compensation node for the current-mode control loop. Connect a series RC network from this pin to VSS for loop compensation. See the Applications section of this datasheet for further details.
CS	8	Feedback (negative) input to the error amplifier. Connect a resistor from this pin to VSS to program the output load current.
SW	9	The source of the internal MOSFET. The output inductor (L_O) and cathode of the free-wheeling diode (D) should be connected to this pin. L_O and D should be placed as close as possible to this pin and connected with relatively wide traces.
BST	10	Bootstrap capacitor connection. A 0.22 µF or higher capacitor is recommended between this pin and SW pin. The voltage on this capacitor drives the internal MOSFET via the high side gate driver.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS [1]: Valid for V_{IN} = 12 V, V_{EN} = 2.5 V, V_{COMP} = 1.4 V, VSS = GND, –40°C ≤ T_J ≤ 125°C, typical values at T_J = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage	V_{IN}	V_{EN} ≥ 2.5 V, V_{IN} with respect to VSS	3.8	12	50	V
VIN UVLO Start	$V_{IN(START)}$	V_{IN} rising, with respect to VSS	3.0	3.3	3.6	V
VIN UVLO Stop	$V_{IN(STOP)}$	V_{IN} falling, with respect to VSS	2.7	3.0	3.3	V
Supply Quiescent Current [1]	$I_{Q(SLEEP)}$	V_{EN} = 0 V	–	11	20	μA
PWM SWITCHING FREQUENCY						
Switching Frequency	f_{SW}	R_{FSET} = 8.06 kΩ	1.8	2.0	2.2	MHz
		R_{FSET} = 41.2 kΩ	360	400	440	kHz
Dither Frequency Sweep	Δf_{SW}		–	±5	–	%
Dither Modulation Frequency	f_{MOD}		–	12	–	kHz
THERMAL PROTECTION						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	–	170	–	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	20	–	°C
PULSE-WIDTH MODULATION (PWM)						
Minimum On-Time	$t_{ON(MIN)}$		–	80	100	ns
Minimum Off-Time	$t_{OFF(MIN)}$		–	100	–	ns
INTERNAL MOSFET						
MOSFET On Resistance	$R_{DS(on)}$	$V_{BOOT-SW}$ = 5 V, T_J = 25°C [2]	–	150	–	mΩ
ERROR AMPLIFIER						
Current Sense Voltage	V_{CS}	3.8 V ≤ V_{IN} ≤ 50 V, –40°C ≤ T_J ≤ 150°C	0.192	0.200	0.208	V
Current Sense Pin Bias Current	I_{CS}		–	–	100	nA
Error Amplifier Voltage Gain	A_{VOL}		–	1000	–	V/V
Error Amplifier Transconductance	g_m	I_{COMP} = ±3 μA	–	120	–	μA/V
Error Amplifier Min. Source Current [3]	$I_{EA(SOURCE)}$	V_{CS} = 0.1 V	–	–13.6	–	μA
Error Amplifier Min. Sink Current [3]	$I_{EA(SINK)}$	V_{CS} = 0.3 V	–	13.6	–	μA

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization; not production tested.
[3] Minimum source and sink current is the minimum current ensured to be provided when COMP demands maximum sink/source current.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS [1] (continued): Valid for V_{IN} = 12 V, V_{EN} = 2.5 V, V_{COMP} = 1.4 V, VSS = GND, –40°C ≤ T_J ≤ 125°C, typical values at T_J = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT PROTECTION						
Pulse-by-Pulse Switch Current Limit	I_{LIM}	Duty cycle 0 to 85%	3.5	5.5	6.5	A
Secondary Current Limit	$I_{LIM(SEC)}$	Hiccup after 2 counts	–	7.1	–	A
COMP to Current Sense Transconductance [2]	G_{CS}		–	9	–	A/V
Slope Compensation	$S_{E(2MHz)}$	Measured at f_{SW} = 2 MHz	–	3.1	–	A/µs
Output Overcurrent	V_{OCP}	With respect to nominal V_{CS} voltage	–	400	–	%
OVERVOLTAGE PROTECTION						
Maximum Output Voltage	V_{OVP}	GND – VSS, when in buck-boost topology	16	18	20	V
LOGIC ENABLE						
EN Logic High Voltage	$V_{EN(H)}$	V_{EN} with respect to GND	1.8	–	–	V
EN Logic Low Voltage	$V_{EN(L)}$	V_{EN} with respect to GND	–	–	0.4	V
EN Hysteresis	$V_{EN(HYS)}$		–	100	–	mV
EN Pin Pull-Down Resistance	R_{ENPN}	V_{EN} = 5 V	–	80	–	kΩ
Maximum PWM Dimming Off Time	t_{PWML}	Measured while EN = low, during dimming control, and internal references are powered-on (exceeding t_{PWML} results in shutdown)	12	20	–	ms
FAULT PIN (FFn)						
Fault Pull-Down Voltage	$V_{FFn(PD)}$	Fault condition asserted, pull-up current = 1 mA	–	–	0.4	V
Fault Pin Leakage Current	$I_{FFn(LKG)}$	Fault condition cleared, pull-up to 12 V	–	–	1	µA
Cooldown Timer for Fault Retry	t_{RETRY}		–	6	–	ms
Delay Timer for Reporting Open LED Fault	t_{OPEN}		–	50	–	µs

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 1: Fault Table

Failure Mode	Symptom Observed	Fault Flag Asserted?	Protection Mode	ALT80802 Response
Inductor shorted	Dim light from LED	Yes	Hiccup	Internal MOSFET switch is shorted. Current spike trips secondary current limit after 2 counts. IC enters hiccup mode with 6 ms retry timer.
LED string open	No light from LED	Depends*	Clamp	In buck topology, IC continues to switch at maximum t_{ON} (since this fault cannot be distinguished from V_{IN} too low for LED forward drop). Output voltage, V_{OUT}, increases until it reaches input voltage, V_{IN}. Fault flag will be asserted if current sense pin voltage, V_{CS}, drops below 150 mV for more than 50 µs. In buck-boost topology, IC continues to switch at maximum t_{ON}. Output voltage V_{OUT} keeps increasing until it is clamped to V_{OVP}. Fault flag will be asserted if current sense pin voltage, V_{CS}, drops below 150 mV for more than 50 µs.
LED string shorted	No light from LED	No	No	V_{OUT} will be regulated to current sense voltage V_{CS} (200 mV typical), no fault is detected.
LED string partially shorted	Some LEDs are not on	No	No	Normal operation, no fault is detected.
Diode open	Dim light from LED	Yes	Hiccup	Detects missing diode fault and shuts off switching. IC enters hiccup mode with 6 ms retry timer.
Diode shorted	No light from LED	Yes	Hiccup	Current spike trips SW secondary current limit. IC enters hiccup mode. IC enters hiccup mode with 6 ms retry timer.
Output capacitor shorted	No light from LED	Yes	Hiccup	IC unable to regulate LED current at V_{OUT} = 0 V. Switch current increases until it trips current limit protection. IC enters hiccup mode with 6 ms retry timer.
Output capacitor open	LED may flicker	Depends	Depends	LED current ripple increases.
Sense resistor open	No light from LED	Yes	Hiccup	Output overcurrent protection is triggered. IC enters hiccup mode with 6 ms retry timer.
Sense resistor shorted	Dim light from LED	Yes*	Hiccup	SW current increases, which eventually trips pulse-by-pulse SW current limit. IC enters hiccup mode with 6 ms retry timer.
FSET resistor open	Dim light from LED	Yes	No	Operates at 772 kHz switching frequency. May hit thermal limit.
FSET resistor shorted	Dim light from LED	Yes	No	Operates at 772 kHz switching frequency. May hit thermal limit.
Boot capacitor open	Dim light from LED	Yes	Hiccup	IC triggers missing Boot protection. IC enters hiccup mode with 6 ms retry timer.
Boot capacitor shorted	No light from LED	Yes	Hiccup	IC triggers Boot shorted protection. IC enters hiccup mode with 6 ms retry timer.

Note (*)

- In case of LED current not in regulation, fault flag is asserted after approximately 50 µs timeout delay. In buck-boost topology, if binning resistors are used, fault flag may not be asserted during an open LED fault.
- If sense resistor is shorted with high resistance wire, protection may not be triggered.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

Overview

The ALT80802 is a buck or buck-boost regulator that incorporates all the control and protection circuitry necessary to satisfy a wide range of LED driver applications. The device employs current-mode control to provide fast transient response, simple compensation, and excellent stability.

The ALT80802 is designed to satisfy the most demanding automotive applications. Extensive protection features prevent the device and the external components from most of the common fault conditions. Care was taken when defining the device pinout to optimize protection against adjacent pin-to-pin short circuits and pin-to-ground (V_{SS}) short circuits.

Switch Mode PWM Operation

A high-speed PWM comparator, with minimum on-time less than 100 ns, is included in the ALT80802. The inverting input of the comparator is connected to the output of the error amplifier. The non-inverting input is connected to the current sense signal.

At the beginning of each switching cycle, the clock signal sets the PWM flip-flop and the internal power MOSFET is turned on. When the current sense signal rises above the error amplifier voltage (proportional to COMP pin voltage), the comparator resets the PWM flip-flop and the high-side MOSFET is turned off. This defines the on-time (t_{ON}) of the switching cycle.

If current sense signal is still higher than the error amplifier voltage before the next clock on signal, the PWM flip-flop will not be set and the next PWM cycle is skipped to prevent output overcharged. This pulse-skipping mode of operation usually happens at high input voltage and low output voltage, when extremely small duty cycle is required. Note that in pulse-skipping mode, average output current is regulated but output ripple will be much higher.

By definition, the duty cycle of a switch mode converter is:

$$D = t_{ON} / \text{Period} = t_{ON} \times f_{SW}$$

where f_{SW} is the switching frequency.

The lowest duty cycle of a converter is limited by the minimum on-time of the high-side MOSFET:

$$D_{MIN} = t_{ON(MIN)} \times f_{SW}$$

For an ideal Buck converter, its duty cycle is given as:

$$D = V_{OUT} / V_{IN}$$

Therefore pulse-skipping will happen in Buck mode when:

Equation 1:

$$V_{OUT} / V_{IN} < t_{ON(MIN)} \times f_{SW}$$

For an ideal Buck-Boost converter, its duty cycle is given as:

$$D = V_{OUT} / (V_{IN} + V_{OUT})$$

In this case, pulse-skipping will happen when:

Equation 2:

$$V_{OUT} / (V_{IN} + V_{OUT}) < t_{ON(MIN)} \times f_{SW}$$

If the current sense signal stays lower than the error amplifier voltage throughout this switching cycle, the PWM flip-flop needs to be reset for a short duration before the next switching cycle can start. This duration is know as the minimum off-time of the high-side MOSFET.

The highest duty cycle of a converter is therefore limited by:

$$D_{MAX} = 1 - t_{OFF(MIN)} \times f_{SW}$$

For a Buck converter (where $D = V_{OUT} / V_{IN}$), the highest output voltage it can generate is:

$$V_{OUT(MAX)} = V_{IN} \times D_{MAX}$$

If V_{IN} continues to decrease, the converter will operate in dropout region. That means both output voltage and LED current will fall below regulation targets.

In Buck mode, the converter operates in dropout region when:

Equation 3:

$$V_{OUT} / V_{IN} > 1 - t_{OFF(MIN)} \times f_{SW}$$

In Buck-Boost mode, the converter operates in dropout mode when:

Equation 4:

$$V_{OUT} / (V_{IN} + V_{OUT}) > 1 - t_{OFF(MIN)} \times f_{SW}$$

It is recommended to keep V_{IN} above dropout region to avoid LED brightness change. ALT80802 does not support dropout region operation with PWM dimming.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Error Amplifier

The primary function of the transconductance error amplifier is to regulate the voltage at the CS pin. By connecting a CS resistor in series with the LED, output current is regulated. The negative input of the error amplifier is connected to the CS pin, and the positive input is connected to the internal reference voltage of 200 mV. The voltage difference between the two inputs is amplified to charge or discharge the compensation network connected to the COMP pin.

To stabilize the regulator, a series RC compensation network (R_Z-C_Z) must be connected from the error amplifier output (COMP pin) to VSS as shown in the typical application schematic. In most applications, an additional low-value capacitor (C_P) should be connected in parallel with the R_Z-C_Z compensation network to roll-off the loop gain at higher frequencies. However, if the C_P capacitor is too large, the phase margin of the regulator may be reduced. In most cases, a C_P value of 39 pF or less is recommended.

The minimum COMP voltage is clamped to 750 mV and its maximum is clamped to 1.5 V. COMP is internally pulled down to V_{SS} during hiccup mode.

Slope Compensation

The ALT80802 incorporates internal slope compensation (S_E) to allow PWM duty cycles above 50% for a wide range of input/output voltages and inductor values. The slope compensation signal is added to the sum of the current sense amplifier output and the PWM ramp offset. The amount of slope compensation scales with the maximum on-time ($1/f_{SW} – t_{OFF(MIN)}$) centered around 3.1 A/µs at 2 MHz. The value of the output inductor should be chosen such that S_E is between 0.5× and 2× the down slope of the inductor current (S_{LD}).

Internal Regulator

An internal series-pass regulator (LDO) generates around 2.9 V for most of the internal circuits of the ALT80802. The power for this LDO is derived from V_{IN}. The LDO is in full regulation once V_{IN} is greater than 3.0 V.

Enable and PWM Dimming

The enable (EN) input allows the system to selectively turn on/off the ALT80802 control loop. The EN pin is rated to 55 V, so the EN pin can be connected directly to VIN if there is no suitable logic signal available to wake up the regulator.

An external logic signal can be applied to the EN pin to control the on/off of LED current. Average brightness of the LED is directly proportional to the duty cycle of the control signal. This technique is commonly known as PWM dimming.

When the EN pin is forced from high to low, the power MOSFET and the error amplifier are turned off, but the IC remains in standby mode for t_{PWML} (20 ms typical) before it completely shuts down. This delay allows PWM dimming frequency down to 100 Hz. In standby mode, the COMP pin is disconnected from the error amplifier and the COMP pin voltage stays at the level before EN turns low. In this way, the steady-state control signal is stored. When the IC receives another EN turn-on signal within t_{PWML}, the system immediately recovers to steady-state operation. As a result, ALT80802 allows down to 15 µs PWM dimming on-time.

In buck-boost topology, the average inductor current is the sum of the average input current and output current. When EN is forced off during PWM dimming operation, the power MOSFET is turned off, cutting the connection from inductor to input capacitor. The inductor current will dump all its energy in terms of current to the output capacitor. This current is much higher than the output current as it also contains the input current portion in buck-boost topology. As a result, the output capacitor will be overcharged and an LED current spike will be seen. To reduce this current spike, the ALT80802 incorporates an internal bleeding circuit that will divert the extra current away from the LED during the PWM dimming turn-off period.

If EN is low for more than t_{PWML}, the IC enters shutdown mode to reduce power consumption. The next high signal on EN will initialize a full startup sequence before LED current starts to build. Note that this startup sequence is not present during PWM dimming operation.

The EN signal is referenced to the GND pin of the ALT80802. This allows the user to use system-referenced signals to this pin even when the output is configured as an inverting buck-boost regulator.

Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) comparator monitors the voltage at the VIN pin (with reference to VSS) and keeps the regulator disabled if the voltage is below the lockout threshold ($V_{IN(START)}$). The UVLO comparator incorporates enough hysteresis ($V_{IN(HYS)}$) to prevent on/off cycling of the regulator due to I_R drops in the V_{IN} path during heavy loading or during startup.

Startup and Shutdown

If both V_{IN} and V_{EN} are higher than their thresholds, the IC starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuits.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Three events can shut down the IC: EN low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the power MOSFET is turned off first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down.

MOSFET Driver and Bootstrap Capacitor

The position of the internal N-channel power MOSFET requires special consideration when driving it. The source of this MOSFET is connected to the SW node and its voltage can be either close to V_{IN} or V_{SS}. For this reason, a floating gate charge driver is required. This driver requires a voltage greater than V_{IN} to ensure the MOSFET can be turned on.

A simple charge pump—consisting of an internal charge circuit, an external capacitor (BST capacitor), and the freewheeling diode —is required to power the high-side gate driver. The internal charge circuit is power by V_{IN}. When the SW node is sufficiently below V_{IN}, the charge circuit will charge the BST capacitor to around 5 V with respect to the SW node. This BST voltage is used to turn the high-side MOSFET on. As the SW node rises, the BST capacitor will maintain the BST pin at 5 V above SW, ensuring sufficient voltage to keep the MOSFET on.

Also, the BST charge circuit incorporates its own UVLO of 1.8 V rising and 0.4 V hysteresis. When BST voltage (with respect to SW pin) is less than UVLO, the power MOSFET is turned off.

Frequency Dithering

The ALT80802 includes a dithering function, which changes the switching frequency within a certain frequency range. By shifting the switching frequency of the regulator in a triangle fashion around the programmed switching frequency, the overall system noise magnitude can be greatly reduced.

The dithering sweep is internally set at ±5%. The switching frequency will ramp from a low of 0.95 times the programmed frequency to a high of 1.05 times the programmed frequency. The rate or modulation at which the frequency sweeps is governed by an internal 12 kHz triangle pattern.

Pulse-by-Pulse Current Limit

A high-bandwidth current sense amplifier monitors the current in the power MOSFET. The current signal is supplied to the PWM comparator and overcurrent comparator. If the MOSFET current exceeds I_{LIM}, the MOSFET will be turned off. This protects the MOSFET from excessive current and possible damage.

Switch Overcurrent Protection and Hiccup Mode

A switch overcurrent (OC) counter and hiccup mode circuit protect the regulator when the output of the regulator is shorted to VSS (shorting output capacitor) or when the load current is too high (shorting CS resistor).

The OC counter is enabled and begin counting every clock cycle when COMP pin voltage, V_{COMP}, is clamped at its maximum voltage. If V_{COMP} remains at its maximum voltage, the counter keeps counting pulses from the overcurrent comparator. If V_{COMP} decreases, the OC counter is cleared. If the OC counter reaches 120 counts, a hiccup latch is set, and the part enters hiccup mode.

In hiccup mode, the COMP pin is quickly pulled down by a relatively low resistance (4 kΩ). Switching is halted for 6 ms to provide time for the device to cool down. The FFn pin is pulled low to indicate a fault condition. After the hiccup off time expires, the device begins a startup sequence. If the fault condition remains, another hiccup cycle occurs. If the fault has been removed, the device starts up normally and the output automatically recovers to target value.

Secondary Switch Overcurrent Protection

If the switch current continues to rise during the OC counting period, a secondary switch current limit of 7.1 A can be reached and the power MOSFET is turned off. If this secondary overcurrent is detected for more than 1 clock cycle, the hiccup latch is set immediately, and the part enters hiccup mode. This usually happens when SW is shorted to VSS.

BOOT Capacitor Protection

The ALT80802 monitors the voltage across the BOOT capacitor to detect if the capacitor is missing or short-circuited. If the BOOT capacitor is missing, the device enters hiccup mode after 7 clock cycles. If the BOOT capacitor is shorted, the device enters hiccup mode after 120 clock cycles. If BOOT capacitor voltage is overcharged to more than 6.3 V, BOOT overvoltage protection is triggered, and the IC enters hiccup mode after 7 PWM cycles.

Freewheeling Diode Protection

If the freewheeling diode is missing or damaged (open), the SW pin is subjected to unusually high negative voltages. This negative voltage may cause the device to malfunction and could lead to damage. The ALT80802 includes protection circuitry to detect when the freewheeling diode is missing. If the SW pin is below −1.25 V for more than 50 ns, the device enters hiccup mode after detecting one missing diode fault. Also, if the freewheeling

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

diode is shorted, the device experiences extremely high currents through the high-side MOSFET. If this occurs, the device triggers a secondary switch current limit and enters hiccup mode.

During a diode short-circuit fault in buck-boost topology, VIN is directly connected to VSS pin when the power MOSFET turns on. This might cause a voltage spike from VSS to GND. If the V_{SS} voltage spike is more than one diode drop higher than GND, it may damage the internal ESD diode at VSS pin. As a result, for buck-boost topology, a Schottky diode must be connected between VSS to GND to clamp the voltage spike during this fault.

Note that the reverse breakdown voltage of the diode must be higher than the maximum output voltage (18 V) and the current rating should be higher than 500 mA.

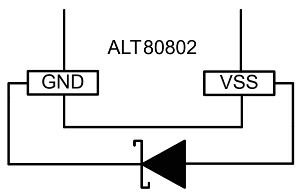


Figure 4: VSS to GND Positive Clamp in Buck-Boost Applications

Output Overcurrent Protection

The ALT80802 provides an always-on output overcurrent protection that monitors CS pin voltage to protect against extremely high LED current. If CS pin voltage, V_{CS}, rises to 800 mV, the device enters hiccup mode immediately.

Output Overvoltage Protection in Buck-Boost

In buck-boost topology, during an open LED fault, output current drops to zero and the control loop will try to compensate the loss of current by demanding higher inductor current. Output voltage across the capacitor is charged up immediately. In the ALT80802, an internal 18 V Zener diode is placed between the positive output (GND) to the negative input of the error amplifier. When output voltage rises to over 18 V (which means CS pin is more than 18 V below GND), the negative input of the error amplifier is charged up, forcing the inductor current to drop. In this way, output voltage can be clamped to 18 V.

However, if the part starts up with an open LED fault, it may take much longer time for the error amplifier to discharge the COMP pin voltage. This delay time may cause the output voltage to rise beyond 20 V, which is higher than the maximum rating for the IC. If inductor current happens to be at a high level, a large current may flow into the IC via the GND pin and the IC may be damaged. To prevent any damage to the IC, it is suggested to use an external circuit, as shown in Figure 5, to stop the switching event before high current flows into the GND pin.

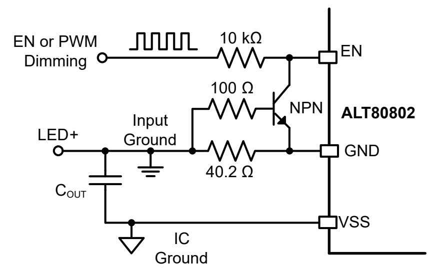


Figure 5: VSS to GND Positive Clamp in Buck-Boost Applications

During an open LED fault, the CS pin voltage drops to zero and the FFn pin will be pulled low if the CS pin voltage stays below 150 mV for more than 50 µs. Note that this undervoltage timer is halted during the PWM dimming off period and will resume when the next dimming cycle starts.

Thermal Shutdown

The ALT80802 protects itself from overheating by means of an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold (T_{TSD}, 170°C typical), the COMP pin will be pulled to VSS and the power MOSFET will be turned off. The ALT80802 will automatically restart when the junction temperature decreases more than the thermal shutdown hysteresis (T_{HYS}, 20°C typical).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATIONS INFORMATION

Setting the Switching Frequency

The switching frequency (f_{SW}) of a regulator using the ALT80802 can be set by connecting a resistor from the FREQ pin (R_{FREQ}) to VSS. The recommended R_{FREQ} value for various switching frequencies can be obtained from Table 2:

Table 2: R_{FREQ} vs. f_{SW}

f_{SW} (MHz)	R_{FREQ} (kΩ)
2.5	6.34
2.0	8.06
1.8	8.87
1.5	10.7
1.0	16.2
0.8	20.5
0.5	33.2
0.4	41.2
0.3	56.2
0.2	84.5
0.2	619

R_{FREQ} resistor can also be calculated with following equation:

Equation 5:

$$R_{FREQ} = \frac{16.95}{f_{SW}} - 0.375$$

where R_{FREQ} is in kΩ and f_{SW} is in MHz.

While the ALT80802 can switch at frequencies up to 2.5 MHz, care must be taken when operating at higher frequencies. The minimum controllable on-time for the ALT80802 is around 80 ns. This means that at higher frequencies, high input voltages, and low output voltages, pulse skipping may be seen.

Setting the Output Voltage

A resistor (R_{SENSE}) from the CS pin to VSS sets the output current. The output current can be calculated with following equation:

Equation 6:

$$I_{OUT} = \frac{V_{CS}}{R_{SENSE}}$$

The bias current of the CS is sufficiently low that is allows for a series resistor between R_{SENSE} and CS pin. This resistor allows the user to perform analog dimming. This can be useful for thermal foldback of the LED current or changing current based on binning resistors.

Figure 6 shows the application schematic for adjusting LED current based on binning resistors. In this schematic, R1 is in parallel with R3 and R_{BIN}. These 3 resistors combining with R2 form a resistor divider that raises the voltage across the sense resistor.

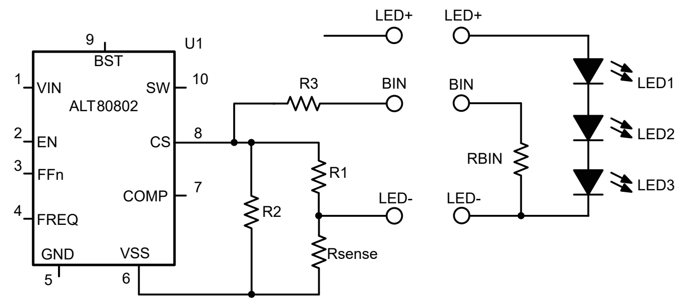


Figure 6: Application Circuit Example for Binning Resistors

The regulated voltage across R_{SENSE} can be calculated with the following equation:

Equation 7:

$$V_{RSENSE} = V_{CS} \times \frac{R_2 + R_1 \parallel (R_3 + R_{BIN})}{R_2}$$

Output current can be calculated with the following equation:

Equation 8:

$$I_{OUT} = \frac{V_{RSENSE}}{R_{SENSE}}$$

In this way, the regulated output current can be tuned by changing R_{BIN}. Note that the purpose of R3 is to filter potential high frequency noise coming from the long LED string cable.

Inductor

To ensure that the inductor operates in continuous mode, the value of the inductor should be set such that half of the peak-to-peak inductor current is not greater than the average inductor current. In buck topology, the average inductor current is the average output current. In buck-boost topology, the average inductor current is the sum of average input current and output current.

As a result, for buck regulators, the following must be guaranteed:

Equation 9:

$$L > \frac{V_{OUT} \times (1 - D_{min})}{2 \times I_{OUT} \times f_{SW}}$$

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

For buck-boost regulators, the following must be guaranteed:

Equation 10:

$$L > \frac{V_{OUT} \times (1 - D_{min})^2}{2 \times I_{OUT} \times f_{SW}}$$

where D_{min} is the minimum duty cycle at maximum input voltage.

To avoid subharmonic oscillation in the current-mode controlled regulators when duty cycle is greater than 50%, the inductor value should be set to match the slope compensation value at the designed frequency.

Slope compensation (S_E) will vary with switching frequency. S_E can be calculated with the following equation:

Equation 11:

$$S_E = S_{E(2MHz)} \times \left(\frac{\frac{1}{2\ MHz} - 100\ ns}{\frac{1}{f_{SW}} - 100\ ns} \right)$$

where S_E is in A/µs and f_{SW} is in MHz. The typical value of $S_{E(2MHz)}$ is 3.1 A/µs.

For a stable system, the following is recommended:

Equation 12:

$$2 \times S_{LD} > S_E > 0.5 \times S_{LD}$$

where S_{LD} is the down slope of the inductor. For buck or buck-boost regulators:

Equation 13:

$$S_{LD} = \frac{V_{OUT}}{L}$$

where L is the inductor value in µH.

As a result, the following must be guaranteed:

Equation 14:

$$\frac{2 \times V_{OUT}}{S_E} > L > \frac{V_{OUT}}{2 \times S_E}$$

The recommended inductor value based on S_E can be calculated using the following equation:

Equation 15:

$$L = \frac{V_{OUT}}{S_E} \times \left(1 - \frac{0.18}{D_{max}}\right)$$

where D_{max} is the maximum duty cycle at minimum input voltage.

The current rating of the inductor should be higher than the peak current during operation.

For buck regulators, the peak inductor current can be calculated by:

Equation 16:

$$I_{LPK} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L}\left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right)$$

For buck-boost regulators, the peak inductor current can be calculated by:

Equation 17:

$$I_{LPK} = I_{OUT} \times \left(1 + \frac{V_{OUT}}{V_{IN(min)}}\right) + \frac{V_{OUT} \times V_{IN(min)}}{2 \times f_{SW} \times L \times (V_{IN(min)} + V_{OUT})}$$

The saturation current of the inductor should be higher than the pulse-by-pulse current limit of the IC (5.5 A typical).

Freewheeling Diode

The freewheeling diode allows the current in the inductor to flow to the load when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky diode.

In buck topology, the voltage rating of the diode must be higher than the maximum input voltage. The average current rating of the diode must be higher than maximum output current. In buck-boost topology, the voltage rating of the diode must be higher than the maximum sum of input voltage and output voltage. The average current rating of the diode must be higher than maximum sum of output current and input current. Note that the peak current of the diode is the peak inductor current.

If the application requires PWM dimming, it is recommended to choose a diode with low reverse current I_R. During PWM dimming off period, output capacitor voltage is discharged mostly by the reverse current of the diode, especially at high temperature. A smaller I_R helps to reduce voltage drop of the output capacitor.

Input Capacitor

Three factors should be considered when choosing the input capacitors. First, they must be chosen to support the maximum expected input voltage with adequate design margin.

Second, their RMS current rating must be higher than the expected RMS input current to the regulator. For simplification, choose the input capacitor with an RMS current rating greater than half of the load current. Generally, a MLCC capacitor can provide enough RMS current with low heat generation.

Third, they must have enough capacitance and a low enough ESR to limit the input voltage dv/dt to much less than the hysteresis of the VIN pin UVLO circuitry (350 mV (typ)) at maximum loading and minimum input voltage.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The input capacitor(s) must limit the voltage deviations at the VIN pin to something significantly less than the ALT80802 VIN pin UVLO hysteresis during maximum load and minimum input voltage.

For buck regulators, the minimum input capacitance can be calculated as:

Equation 18:

$$C_{IN} > \frac{I_{OUT}}{4 \times \eta \times f_{SW} \times \Delta V_{IN}}$$

For buck-boost regulators, the minimum input capacitance can be calculated as:

Equation 19:

$$C_{IN} > \frac{I_{OUT} \times D_{max}}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where ΔV_{IN} is the output capacitor voltage deviation, η is the estimated efficiency of the regulator. ΔV_{IN} should be chosen to be much less than the hysteresis of the VIN pin, UVLO comparator ($\Delta V_{IN} \leq 100$ mV is recommended).

Note that the DC bias on the capacitor can derate the capacitance value. For example, a 50 V, 4.7 µF rated ceramic capacitor can be less than 3 µF when 30 V DC bias is applied. Capacitance value can also change due to temperature. X7R capacitors are recommended for low capacitance variation over temperature.

In general, for 2 MHz applications, a 4.7 µF ceramic capacitor with X7R dielectric is sufficient.

Output Capacitor

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage, and they store energy to help maintain voltage regulation during a transient event. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitor parameters: C_{OUT}, ESR, and ESL.

For buck regulators, the output voltage ripple can be calculated by:

Equation 20:

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L} \times ESL + \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}}$$

For buck-boost regulators, the output voltage ripple can be calculated by:

Equation 21:

$$\Delta V_{OUT} = I_{LPK} \times ESR + \frac{V_{OUT}}{L} \times ESL + \frac{I_{OUT} \times V_{OUT}}{f_{SW} \times (V_{IN} + V_{OUT}) \times C_{OUT}}$$

where ΔI_L is the peak-to-peak inductor current, I_{LPK} is the peak inductor current.

To reduce the overall output ripple, it is recommended to use ceramic output capacitors, especially for buck-boost regulators. The ESR and ESL of the ceramic capacitors are virtually zero.

If ceramic output capacitors are used, for buck regulators, calculate:

Equation 22:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}}$$

For buck-boost regulators, calculate:

Equation 23:

$$\Delta V_{OUT} = \frac{I_{OUT} \times V_{OUT}}{f_{SW} \times (V_{IN} + V_{OUT}) \times C_{OUT}}$$

In general, for 2 MHz applications, a 1 µF ceramic output capacitor with X7R dielectric is sufficient.

Compensation Components

The ALT80802 employs current-mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero pair to control the characteristics of the control system.

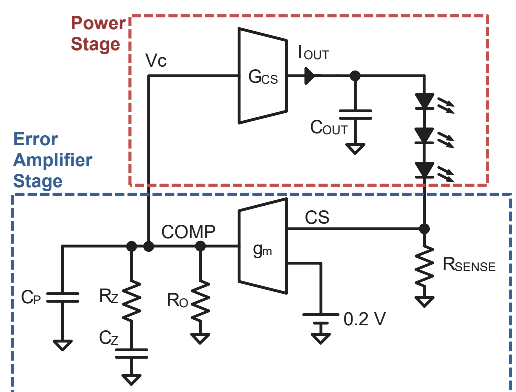


Figure 7: Basic Current-Mode Control Schematic

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The objective of the selection of compensation components is to ensure a high DC gain and wide bandwidth for optimal small-signal transient response, and adequate margin to avoid instability. As an LED driver or current regulator, output current is the controlled target.

The small-signal loop can be modeled as shown in Figure 7, where the loop is broken into two blocks: power stage and error amplifier stage.

The power stage includes an inner current loop of the current-mode controller, C_{OUT} and LED load. Although the peak inductor current is being controlled, to a first approximation for simplifying the equations, it is acceptable to use the output current I_{OUT}.

The error amplifier stage includes a current sense resistor R_{SENSE}, an error amplifier, and compensation components.

Compensation Design for Buck Regulators

The power stage DC gain can be calculated as:

Equation 24:

$$G_{PS} = \frac{\Delta I_{OUT}}{\Delta V_C} = G_{CS}$$

where G_{CS} is the current sense gain of the current amplifier. The typical value of G_{CS} is 9 A/V.

The output capacitor integrates the ripple current through the inductor, effectively forming a single pole with the output load. The pole $f_{P(ps)}$ can be found at:

Equation 25:

$$f_{P(ps)} = \frac{1}{2\pi \times R_{LED} \times C_{OUT}}$$

where R_{LED} is the effective resistance for the LED when conducting target output current I_{OUT}. The small signal LED resistance can be calculated as:

Equation 26:

$$R_{LED} = \frac{d_v}{d_i}$$

Note that this dv and di can be found by the I-V curve of the LED. For example, if the target output current is 700 mA, dV and dI are set around that level as shown in Figure 8.

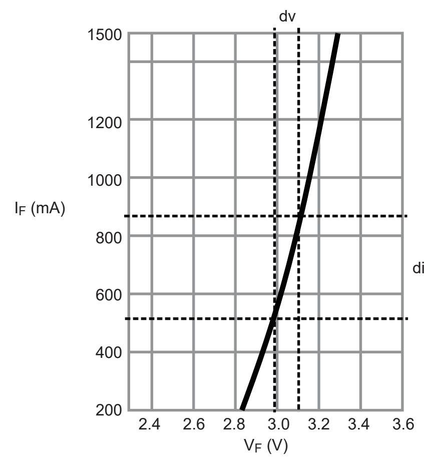


Figure 8: Typical I-V Curve of a White LED

There is also a zero in the power stage formed by the ESR of the output capacitor. However, if ceramic capacitors are used, this zero can be ignored.

For the error amplifier stage, the DC gain of the amplifier is 1000 V/V, and the transconductance g_m value is 120 µA/V. The effective output impedance of the error amplifier R_O can be given as:

Equation 27:

$$R_O = \frac{1000}{120 \times 10^{-6}} = 8.33 \text{ M}\Omega$$

The DC gain of the error amplifier is high enough to ensure good output current regulation. The gain is rolled off with a single pole formed by the output impedance of the amplifier R_O and the capacitor C_Z connected to the COMP pin. The position of this pole is:

Equation 28:

$$f_{P1(ea)} = \frac{1}{2\pi \times R_O \times C_Z}$$

A zero is positioned at a higher frequency to cancel the effects of the power stage pole. This zero can be found at:

Equation 29:

$$f_{Z(ea)} = \frac{1}{2\pi \times R_Z \times C_Z}$$

A second pole is needed to suppressed high-frequency noise. It should be placed far away from the crossover frequency to have minimal effect on the control. This pole can be found at:

Equation 30:

$$f_{P2(ea)} = \frac{1}{2\pi \times R_Z \times C_P}$$

The current sense resistor introduces a DC gain for the control loop, which can be calculated as:

Equation 31:

$$G_{FB} = \frac{V_{CS}}{I_{OUT}} = R_{SENSE}$$

Overall loop response is the combination of the power stage and error amplifier stage. This feedback loop should be designed to have a suitable crossover frequency and phase margin.

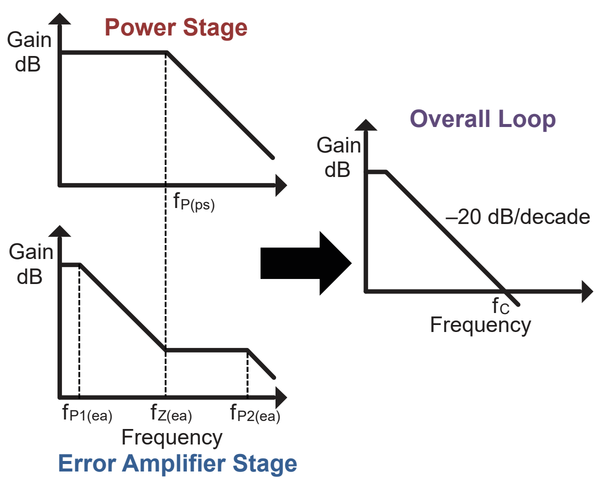


Figure 9: Basic Current-Mode Control Schematic

It is recommended to achieve a –20 dB/decade roll-off for the overall loop, which means that the error amplifier zero should be placed at the same frequency of the power stage pole. Figure 9 shows recommended gain plot of the power stage, the error amplifier stage, and the combined overall loop response.

Compensation Design for Buck-Boost Regulators

The compensation design for buck-boost regulators follows the same idea as the buck. The error amplifier stage of the buck-boost regulators is the same as the buck. The only difference is the power stage response.

The power stage DC gain of buck-boost regulators can be calculated as:

Equation 32:

$$\frac{I_{OUT}}{V_C} = \frac{1-D}{1+D} \times G_{CS}$$

where D is the duty cycle, and G_{CS} is 9 A/V.

The power stage pole can be calculated as:

Equation 33:

$$f_{P(ps)} = \frac{1+D}{2\pi \times R_{LED} \times C_{OUT}}$$

where R_{LED} is the effective resistance for the LED.

The power stage also includes a right half plane zero, which frequency can be calculated as:

Equation 34:

$$f_{RHPZ(ps)} = \frac{R_{LED} \times (1-D)^2}{L \times D}$$

where L is the inductor in the power stage.

Recommended Control Loop Design Strategy

1. Choose a crossover frequency f_C to be 1/10 of the switching frequency f_{SW}. However, the maximum f_C should be set below 75 kHz to have good noise suppression. For buck-boost regulators, cross-over frequency should be less than 1/5 of the right half plane zero frequency.
2. Calculate DC gain of the overall loop in dB, which is:
$$G_{LOOP(dB)} = G_{PS(dB)} + g_{m(dB)} + G_{FB(dB)}$$
3. The estimated –20 dB/decade roll-off slew rate from the first amplifier pole to the crossover frequency will set the position of the pole $f_{P1(ea)}$. Calculate the C_Z value.
4. Calculate the position of the power stage pole $f_{P(ps)}$.
5. Set the error amplifier zero $f_{Z(ea)}$ to be at the same frequency of the power stage pole. Calculate the R_Z value. If the power stage pole $f_{P(ps)}$ is significantly higher than the crossover frequency (more than 5×), R_Z can be removed. However, R_Z is helpful in instant transient response.
6. Set the high frequency error amplifier pole to be higher than the error amplifier zero and calculate the C_P value. Typically, choose a C_P value between 22 pF and 39 pF.
7. If possible, test the overall loop bode plot of the system. Adjust the R_Z and C_Z to fine-tune the control loop crossover frequency and phase margin. Typically, phase margin should be more than 45 degrees to guarantee stability.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Design Example

Buck LED Driver

This example application is a buck LED driver using the ALT80802. The operating voltage range is 9 to 18 V, nominal input voltage is 12 V, and the target switching frequency is 2 MHz; the output load is 2 white LEDs (LUW CQAR) with 3 V forward voltage; target output current is 700 mA.

To set the output current to 700 mA, current sense resistor R_{SENSE} is:

Equation 35:

$$R_{SENSE} = \frac{V_{CS}}{I_{OUT}} = \frac{200\ mV}{700\ mA} = 285\ m\Omega$$

Note that 280 mΩ is the common resistor value with 1% accuracy. As a result, 280 mΩ is chosen.

The nominal duty cycle can be calculated as:

Equation 36:

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{6}{12} = 0.5$$

To guarantee CCM operation over all input range, inductor L must satisfy:

Equation 37:

$$L > \frac{V_{OUT} \times (1 - D_{min})}{2 \times I_{OUT} \times f_{SW}} = \frac{12 \times (1 - 0.33)}{2 \times 0.7 \times 2 \times 10^6} = 2.87\ \mu H$$

A 3.3 µH inductor can be selected. The down slope of the inductor can be calculated as:

Equation 38:

$$S_{LD} = \frac{V_{OUT}}{L} = \frac{6\ V}{3.3\ \mu H} = 1.82\ (A/\mu s)$$

$$\frac{S_E}{S_{LD}} = \frac{3.1}{1.82} = 1.70$$

The slope compensation to inductor down slope ratio is within the range of 0.5 to 2. As a result, the slope compensation should have little influence on the overall loop response.

Input capacitors and output capacitors are selected to the standard values of 4.7 µF and 1 µF.

For a 2 MHz design, the maximum crossover frequency should be set below 75 kHz. The crossover frequency can be set to 40 kHz in this application.

From LUW CQAR datasheet, the small signal LED resistance can be calculated as:

Equation 39:

$$R_{LED} = \frac{d_V}{d_I} \approx 0.5\ \Omega$$

The power stage DC gain can be calculated as:

Equation 40:

$$\frac{\Delta I_{OUT}}{\Delta V_C} = G_{CS} = 9$$

The current sense DC gain is:

Equation 41:

$$G_{FB} = \frac{V_{CS}}{I_{OUT}} = R_{SENSE} = 0.28$$

The DC gain of the error amplifier is 1000 V/V.

The overall loop gain can be calculated as:

Equation 42:

$$G_{LOOP(dB)} = 20\log_{10} 9 + 20\log_{10} 0.28 + 20\log_{10} 1000 = 68.02\ dB$$

with estimated –20 dB/decade roll-off slew, the position of the first amplifier pole can be calculated as:

Equation 43:

$$f_{P1(ea)} = \frac{40\text{ kHz}}{10^{\frac{68.02}{20}}} = 15.88 Hz$$

The C_Z value can be calculated as:

Equation 44:

$$C_Z = \frac{1}{2\pi \times R_O \times f_{P1(ea)}} = \frac{1}{2\pi \times 8.33 \times 10^6 \times 11.90} = 1.3\ nF$$

To match the standard capacitor value, a 1.5 nF C_Z can be selected.

The power stage pole can be calculated as:

Equation 45:

$$f_{P(ps)} = \frac{1}{2\pi \times R_{LED} \times C_{OUT}} = \frac{1}{2\pi \times 0.7 \times 1 \times 10^{-6}} = 227\ kHz$$

This power stage pole is at much higher frequency than the designed crossover frequency. As a result, R_Z is not needed. However, to improve the instant response, a 2.49 kΩ resistor is selected.

For C_P, a typical value of 22 pF can be chosen to suppress high frequency noise.

If PWM binning applications, the binning circuit resistors and binning resistor selected by the design tools.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Buck-Boost LED Driver

This example application is a buck-boost LED driver using the ALT80802. The operating voltage range is 6 to 18 V, nominal input voltage is 12 V, and the target switching frequency is 2 MHz; the output load is 4 white LEDs (LUW CQAR) with 3 V forward voltage; target output current is 350 mA.

To set the output current to 700 mA, current sense resistor R_{SENSE} is:

Equation 46:

$$R_{SENSE} = \frac{V_{CS}}{I_{OUT}} = \frac{200\ mV}{350\ mA} = 571\ m\Omega$$

Note that 560 mΩ is the common resistor value with 1% accuracy. As a result, 560 mΩ is chosen. The nominal output current with 560 mΩ is 357 mA.

The nominal duty cycle can be calculated as:

Equation 47:

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}} = \frac{3 \times 4}{12 + 3 \times 4} = 0.5$$

To guarantee CCM operation over all input range, inductor L must satisfy:

Equation 48:

$$L > \frac{V_{OUT} \times (1 - D_{min})^2}{2 \times I_{OUT} \times f_{SW}} = \frac{12 \times (1 - 0.4)^2}{2 \times 0.35 \times 2 \times 10^6} = 3.08\ \mu H$$

To reduce the output ripple, a 4.7 µH inductor can be selected. The down slope of the inductor can be calculated as:

Equation 49:

$$S_{LD} = \frac{V_{OUT}}{L} = \frac{12\ V}{4.7\ \mu H} = 2.55\ (A/\mu s)$$

$$\frac{S_E}{S_{LD}} = \frac{3.1}{2.55} = 1.22$$

The slope compensation to inductor down slope ratio is within the range of 0.5 to 2. As a result, the slope compensation should have little influence on the overall loop response.

Input capacitors and output capacitors are selected to be the standard values of 4.7 µF and 1 µF.

As a buck-boost regulator, crossover frequency should be less than 1/5 of the right half plane zero.

From the LUW CQAR datasheet, the small signal LED resistance can be calculated as:

Equation 50:

$$R_{LED} = \frac{d_V}{d_I} \approx 0.9\ \Omega$$

The right half plane zero of buck-boost regulators can be calculated as:

Equation 51:

$$f_{RHPZ(ps)} = \frac{R_{LED} \times (1 - D)^2}{L \times D} = \frac{0.9 \times 0.5^2}{4.7 \times 10^{-6} \times 0.5} = 95.74\ kHz$$

As a result, the crossover frequency can be set at 20 kHz.

The power stage DC gain can be calculated as:

Equation 52:

$$\frac{\Delta I_{OUT}}{\Delta V_C} = \frac{1 - D}{1 + D} \times G_{CS} = \frac{0.5}{1.5} \times 9 = 3$$

The current sense DC gain is:

Equation 53:

$$G_{FB} = \frac{V_{CS}}{I_{OUT}} = R_{SENSE} = 0.56$$

The DC gain of the error amplifier is 1000 V/V.

The overall loop gain can be calculated as:

Equation 54:

$$G_{LOOP(dB)} = 20 \log_{10} 3 + 20 \log_{10} 0.56 + 20 \log_{10} 1000 = 64.51\ dB$$

With estimated –20 dB/decade roll-off slew, the position of the first amplifier pole can be calculated as:

Equation 55:

$$f_{P1(ea)} = \frac{20\ \text{kHz}}{10^{\frac{64.51}{20}}} = 11.89\ Hz$$

The C_Z value can be calculated as:

Equation 56:

$$C_Z = \frac{1}{2\pi \times R_O \times f_{P1(ea)}} = \frac{1}{2\pi \times 8.33 \times 10^6 \times 11.89} = 1.61\ nF$$

To match the standard capacitor value, a 1.5 nF C_Z can be selected.

The power stage pole can be calculated as:

Equation 57:

$$f_{P(ps)} = \frac{1 + D}{2\pi \times R_{LED} \times C_{OUT}} = \frac{1 + 0.5}{2\pi \times 0.9 \times 1 \times 10^{-6}} = 265\ kHz$$

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

This power stage pole is at much higher frequency than the designed crossover frequency. As a result, R_Z is not needed. However, to improve the instant response, a 2.49 kΩ resistor is selected.

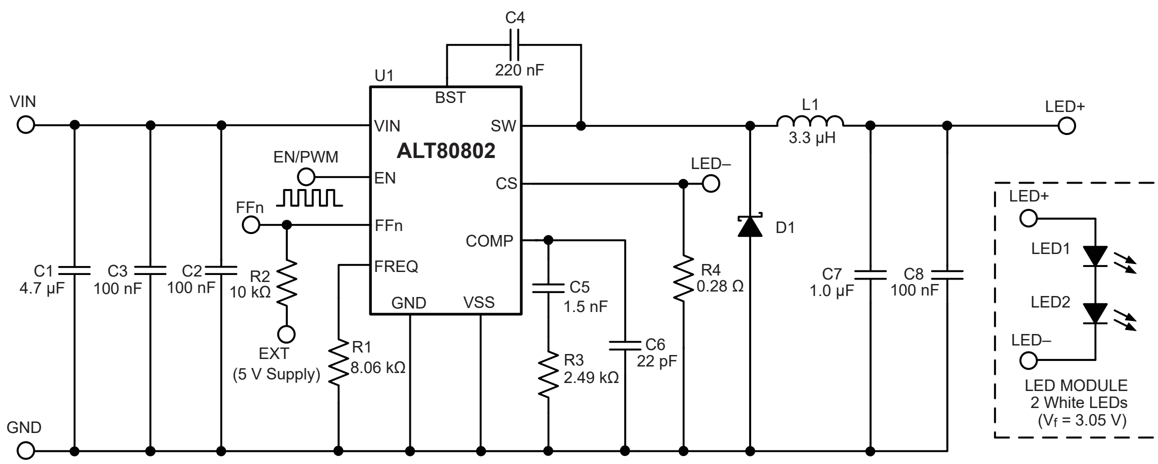
For C_P, a typical value of 22 pF can be chosen to suppress high frequency noise.

For PWM binning applications, the binning circuit resistors and binning resistor can be selected by the design tools.

To improve the EMI/EMC performance, a 100 nF capacitor should be placed between VIN and VSS to supply the Boot capacitor during boot charging transients. Note that this capacitor cannot be too large, or it will affect the output stability during V_{IN} transients.

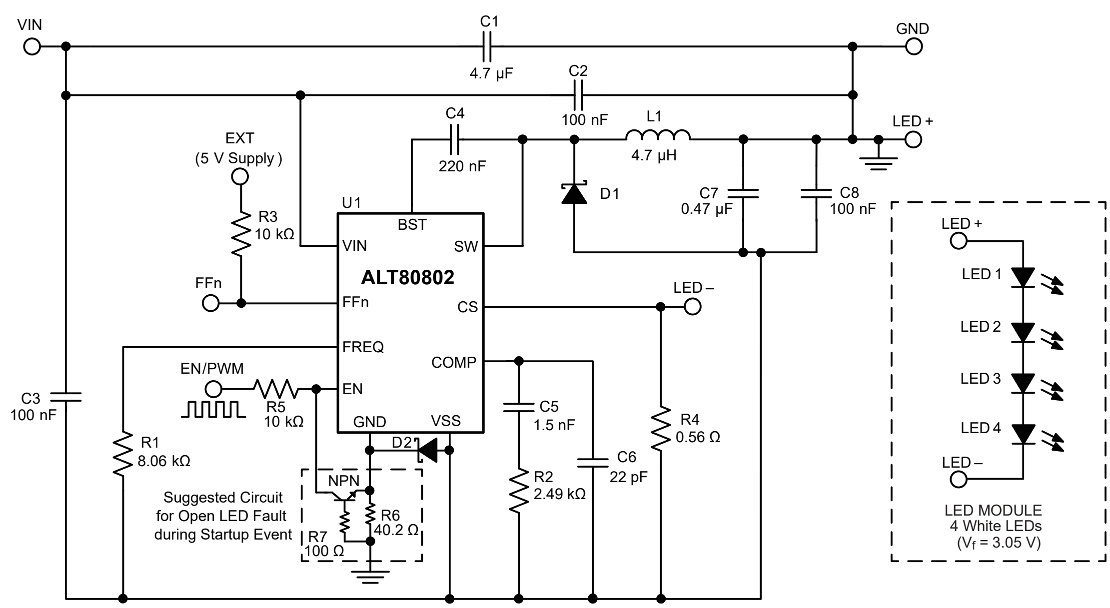
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

TYPICAL APPLICATION SCHEMATICS



DC Input Voltage Range	9-18 V
PWM Dimming Range (200 Hz)	1%-100%

Figure 10: 2 MHz, 700 mA, 2 LEDs Buck LED Driver with Fault Flag and PWM Dimming



DC Input Voltage Range	6-18 V
PWM Dimming Range (200 Hz)	1%-100%

Figure 11: 2 MHz, 350 mA, 4 LEDs Inverting Buck-Boost LED Driver with Fault Flag and PWM Dimming

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PCB COMPONENT PLACEMENT AND ROUTING

Buck LED Driver

A good PCB layout is critical for the ALT80802 to provide clean, stable output voltages. Figure 12 shows a typical ALT80802-based buck LED driver schematic with the critical power paths/loops. Figure 13 shows an example PCB component placement and routing with the same critical power paths/loops as shown in the schematic. Follow these guidelines to ensure a good PCB layout.

1. The high di/dt pulsating current loop for a buck regulator is formed by the ceramic input capacitor (C1 and C2), power MOSFET inside of the IC, and freewheeling diode (D1). These components must be closely placed with wide traces and the loop area must be minimized. Ideally, these components are all connected using only the top metal layer.
2. Another pulsating current loop is the boot charging path which includes the input capacitor (C1 and C2), boot charge capacitor (C4), and freewheeling diode. The current of this loop should be less than 300 mA, and the trace width should be set accordingly.
3. A 100 nF capacitor, C3, from VIN to GND provides a solid ground reference for the input of the internal LDO. This capacitor should be placed close to VIN pin and VSS pin of the IC.
4. VSS and GND pins should be tied together with a single solid ground plane. Note that to ensure the lowest junction temperature, multiple vias are recommended to connect the thermal pad to the bottom layer ground plane.
5. Compensation components, FSET resistor, and current sense resistors should be connected close to the IC with clean ground reference.
6. SW node is a high dv/dt node. This high dv/dt copper area should be minimized to reduce any voltage coupling to the other layers.

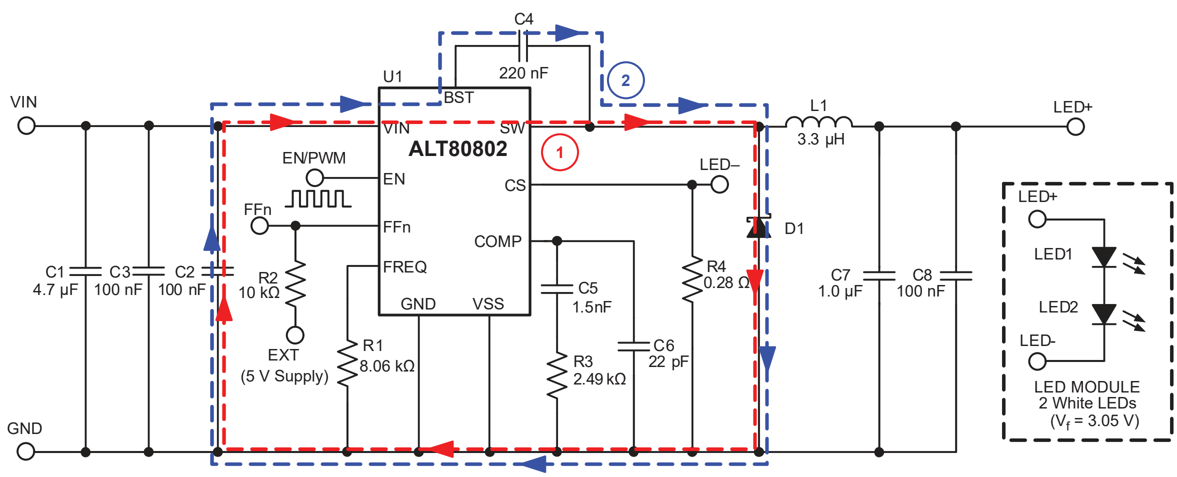


Figure 12: Typical Buck LED Driver Application with Critical Loops Shown

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

LOOP 1 (RED)

This loop contains the main switching frequency pulsating current during operation. The loop area should be minimized to reduce the loop inductance and noise antenna size.

The turn-on and turn-off of the power MOSFET will generate high di/dt transients. Parasitic inductance within this loop will cause oscillation during these transients. Also, the peak current in this loop can be as high as 5.5 A. It is recommended to use short and wide traces to reduce the parasitic inductance and resistance.

LOOP 2 (BLUE)

This loop contains pulsating current when the Boot capacitor is charged. The frequency of this pulsating current can also be as high as the switching frequency. The loop area should be minimized.

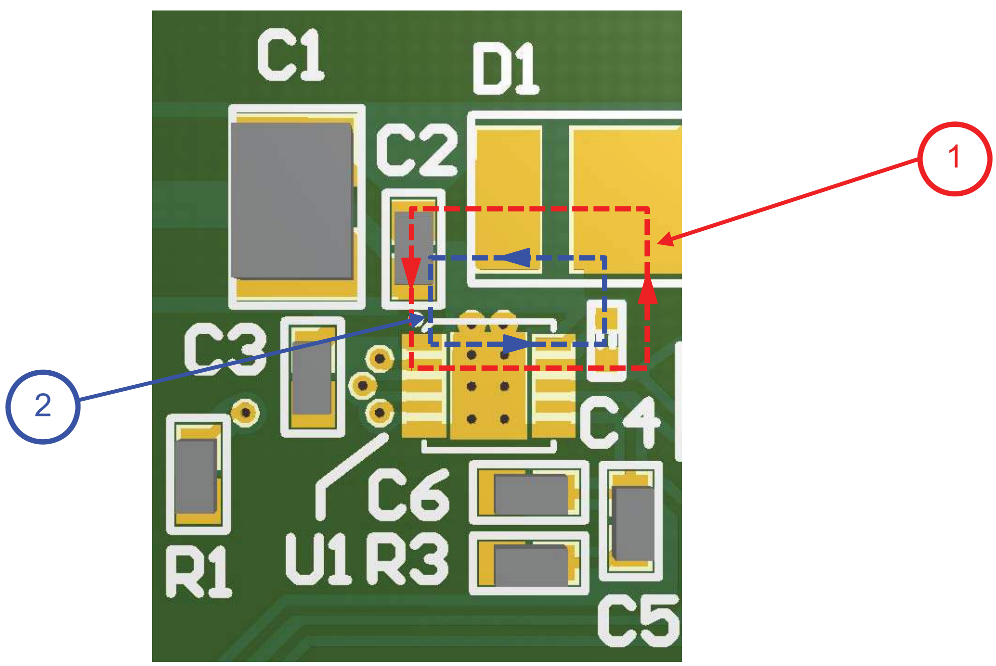


Figure 13: Example PCB Layout for Buck LED Driver Application

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Buck-Boost LED Driver

Figure 14 shows a typical ALT80802-based buck-boost LED driver schematic with the critical power paths/loops. Figure 15 shows an example PCB component placement and routing with the same critical power paths/loops as shown in the schematic. Follow the following guidelines to ensure a good PCB layout.

1. The high di/dt pulsating current loop for a buck-boost regulator is formed by the ceramic input capacitor (C1 and C2), power MOSFET inside of the IC, freewheeling diode (D1), and the ceramic output capacitor (C7 and C8). These components need to be placed closely with wide traces and the loop area needs to be minimized. Ideally, these components are all connected using only the top metal layer.
2. Another pulsating current loop is the boot charging path which includes the VIN to VSS ceramic capacitor (C3), boot charge capacitor, and freewheeling diode. The current of this loop should be less than 300 mA, and the trace width should be set accordingly. The boot capacitor and the VIN to VSS ceramic capacitor should be connected as close as possible to the IC.
3. The solid ground reference for the IC is VSS instead of GND. In buck topology, these two pins should be tied together with a single solid ground plane. In buck-boost topology, these two pins are completely separated. The ground plane on the PCB should be tied to VSS pin and thermal pad of the IC. Note that to ensure the lowest junction temperature, multiple vias are recommended to connect the thermal pad to the bottom layer ground plane.
4. Compensation components, FSET resistor, and current sense resistors should be connected close to the IC with clean ground reference.
5. The clamping diode from VSS to GND should be connected close to these two pins.
6. SW node is a high dv/dt node. This high dv/dt copper area should be minimized to reduce any voltage coupling to the other layers.

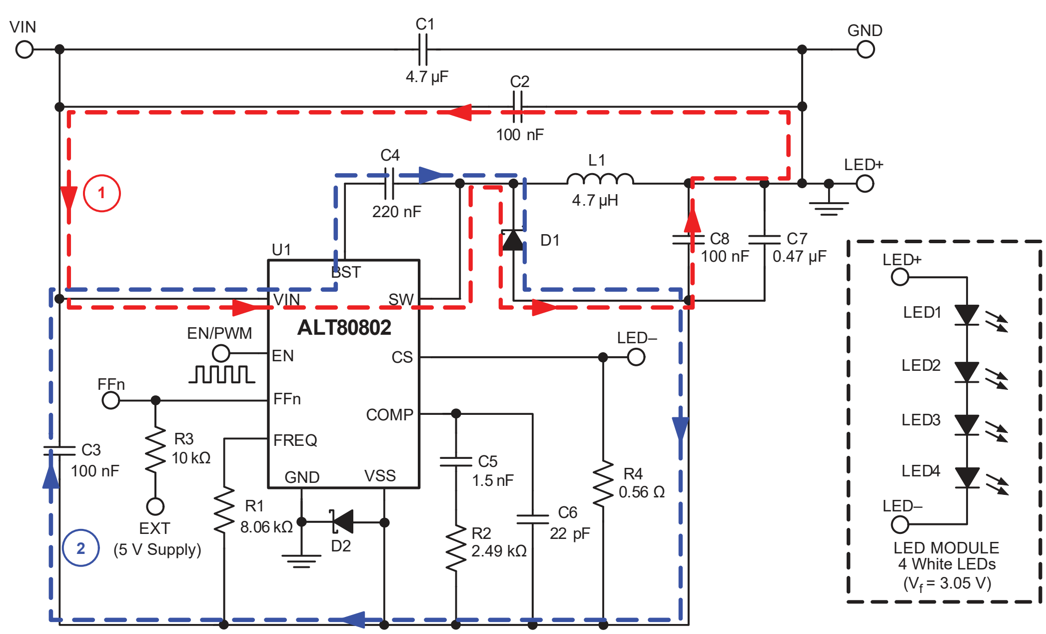


Figure 14: Typical Buck-Boost LED Driver Application with Critical Loops Shown

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

LOOP 1 (RED)

This loop contains the main switching frequency pulsating current during operation. The loop area should be minimized to reduce the loop inductance and noise antenna size.

The turn-on and turn-off of the power MOSFET will generate high di/dt transients. Parasitic inductance within this loop will cause oscillation during these transients. Also, the peak current in this loop can be as high as 5.5 A. It is recommended to use short and wide traces to reduce the parasitic inductance and resistance.

LOOP 2 (BLUE)

This loop contains pulsating current when the Boot capacitor is charged. The frequency of this pulsating current can also be as high as the switching frequency. The loop area should be minimized.

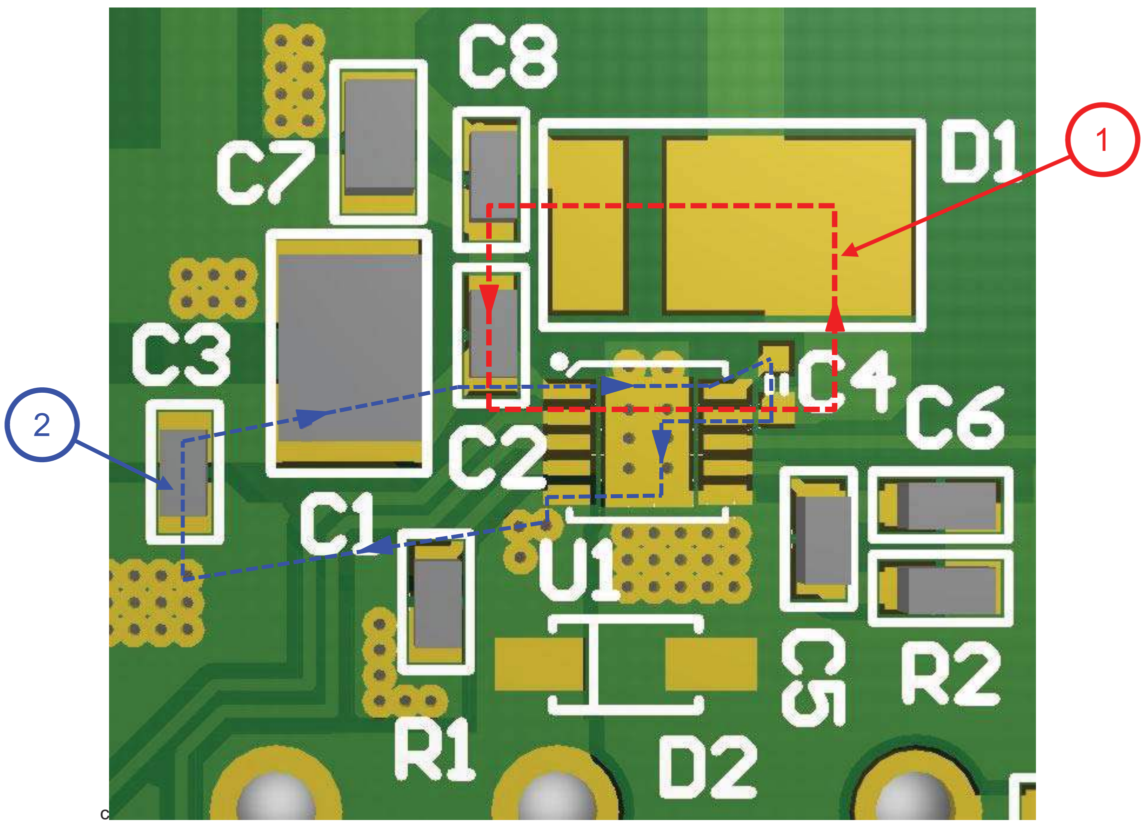
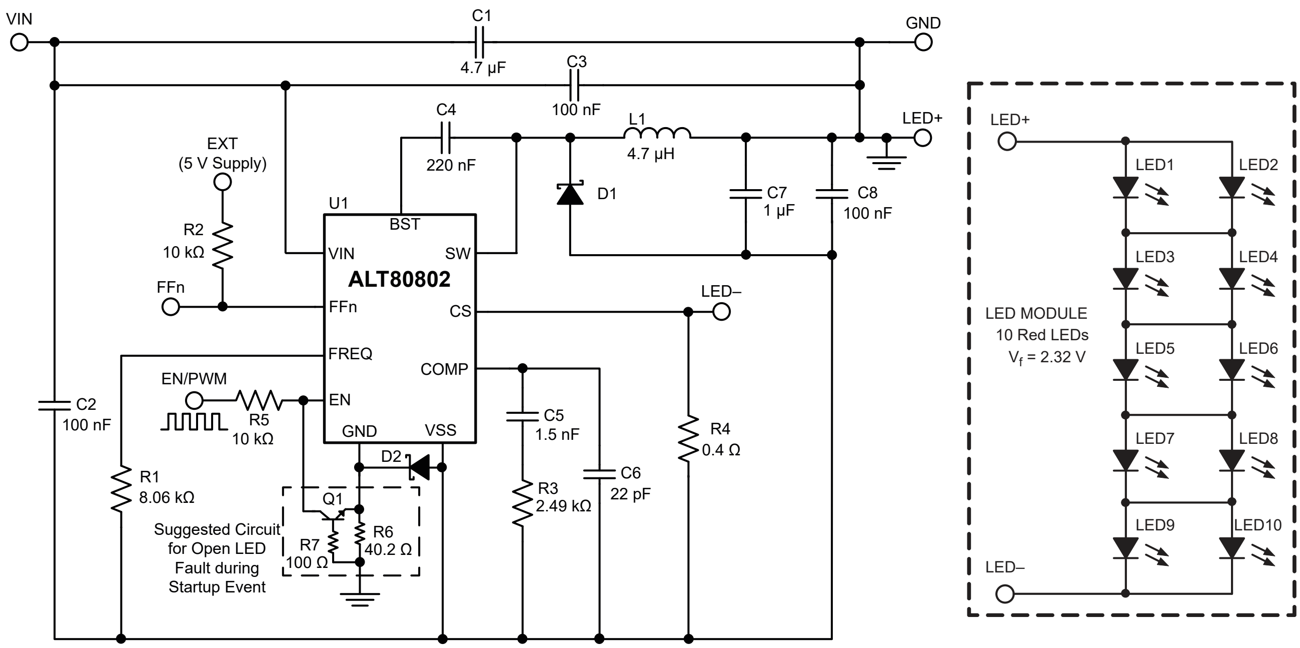


Figure 15: Example PCB Layout for Buck-Boost LED Driver Application

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION CIRCUIT EXAMPLES

Application 1: CHMSL with 10 Red LEDs



DC Input Voltage Range	6-18 V
PWM Dimming Range (200 Hz)	1%-100%

Figure 16: 2 MHz, 250 mA, 10 Red LEDs Inverting Buck-Boost LED Driver with Fault Flag

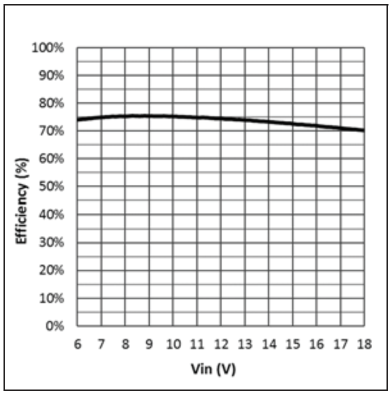
Application 1: Recommended Bill of Materials

Reference	Description	Manufacturer/Part Number
C1	4.7 µF, ceramic capacitor, X7R, 50 V, 1210	
C2, C3, C8	100 nF, ceramic capacitor, X7R, 50 V, 0603	
C4	220 nF, ceramic capacitor, X7R, 16 V, 0402 or 0603	
C5	1.5 nF, ceramic capacitor, X7R, 16 V, 0603	
C6	22 pF, ceramic capacitor, X7R, 16 V, 0603	
C7	1 µF, ceramic capacitor, X7R, 50 V, 0805	
R1	8.06 kΩ resistor, 1/10 W, 1%	
R2	10 kΩ resistor, 1/10 W, 1%	
R3	2.49 kΩ resistor, 1/10 W, 1%	
R4	400 mΩ resistor, 1/2 W, 1%	
R6	40.2 Ω resistor, 1/10 W, 1%	
R7	100 Ω resistor, 1/10 W, 1%	
D1	Diode, Schottky, 60 V, 5 A, 670 mV @ 5 A	Diodes Incorporated, PDS560-13
D2	Diode, Schottky, 40 V, 1 A, 410 mV @ 1 A	Diodes Incorporated, 1N5819HW-7-F
Q1	Transistor, NPN, 65 V, 0.1 A, SOT23	On Semiconductor, BC846ALT1G
L1	Inductor, 4.7 µH, 9.8 A(sat), 15.32 mΩ (max)	Vishay, IHLP4040DZER4R7M8A

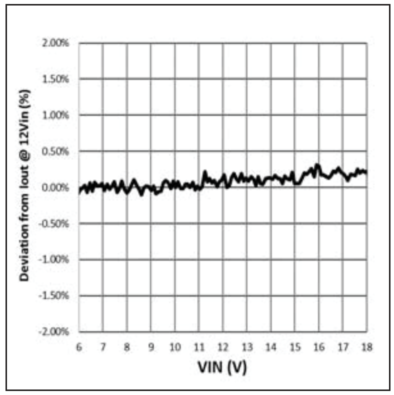
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Application 1: Performance

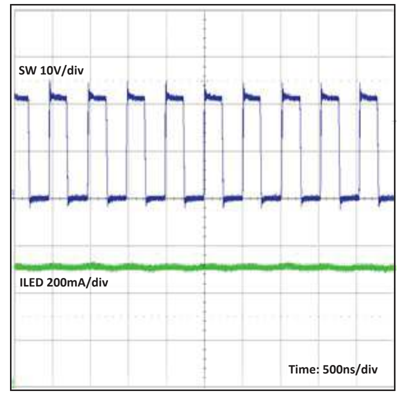
System Efficiency with Full Brightness



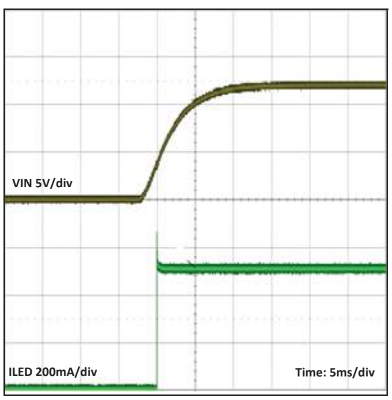
LED Current Line Regulation



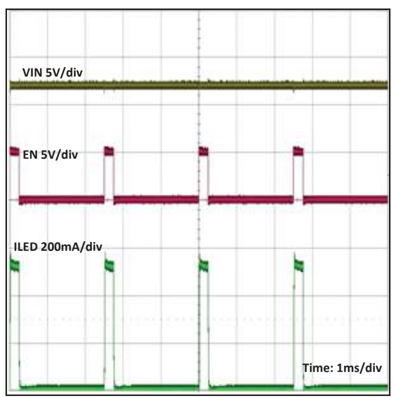
Switching Waveform



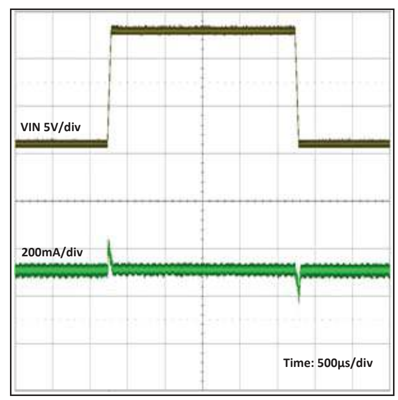
Startup Waveform



10% LED Dimming Waveform

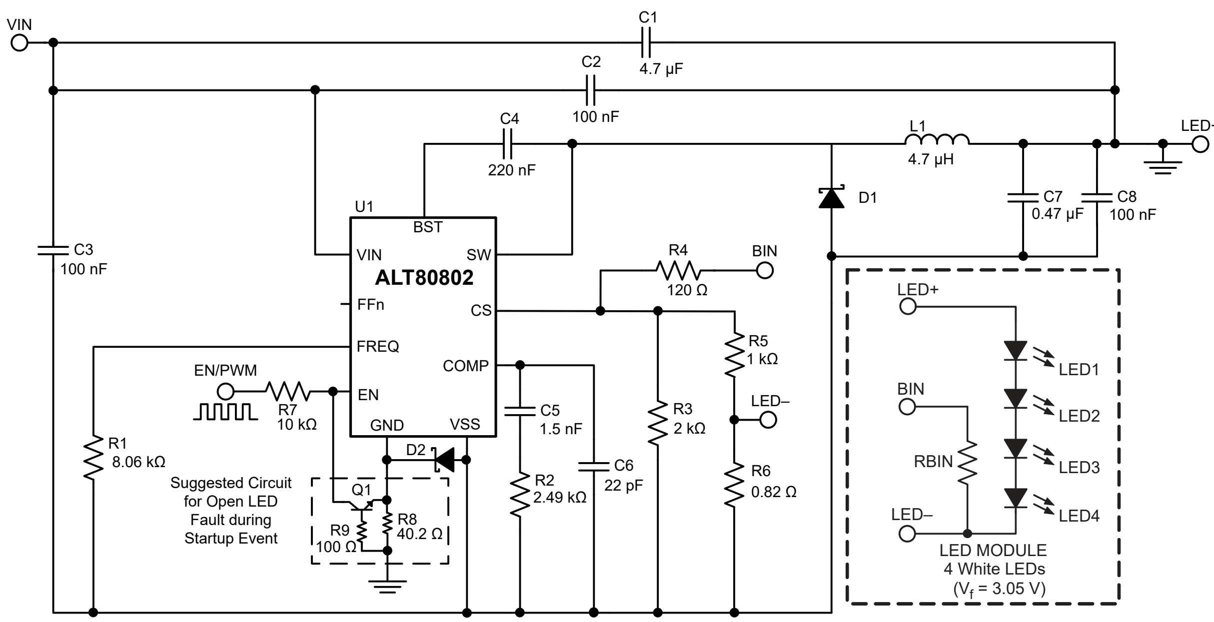


6-18 V Fast VIN Transient



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Application 2: Buck-Boost LED Driver with Binning Resistor



Input Range	6-18 V
PWM Dimming Range (200 Hz)	1%-100%

Binning resistor values for LED current reduction:

LED Current	100%	90%	80%	70%
RBIN	Open	2.21 kΩ	549 Ω	Short

Figure 17: 2 MHz, 350 mA Inverting Buck-Boost LED Driver for 1-4 LEDs with Binning Resistor on LED Module

Application 2: Recommended Bill of Materials

Reference	Description	Manufacturer/Part Number
C1	4.7 µF, ceramic capacitor, X7R, 50 V, 1210	
C2, C3, C8	100 nF, ceramic capacitor, X7R, 50 V, 0603	
C4	220 nF, ceramic capacitor, X7R, 16 V, 0402 or 0603	
C5	1.5 nF, ceramic capacitor, X7R, 16 V, 0603	
C6	22 pF, ceramic capacitor, X7R, 16 V, 0603	
C7	1 µF, ceramic capacitor, X7R, 50 V, 0805	
R1	8.06 kΩ resistor, 1/10 W, 1%	
R2	2.49 kΩ resistor, 1/10 W, 1%	
R3	2 kΩ resistor, 1/10 W, 1%	

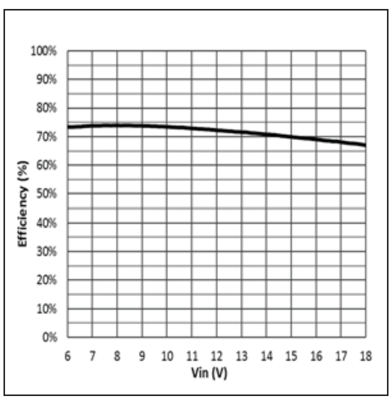
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Application 2: Recommended Bill of Materials (continued)

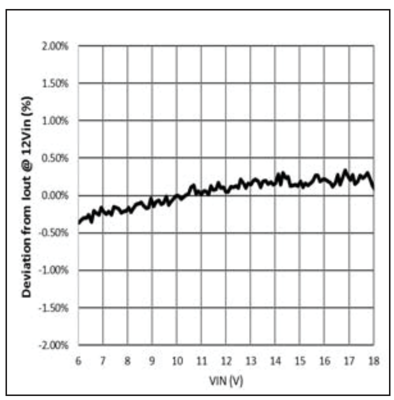
Reference	Description	Manufacturer/Part Number
R4	120 Ω resistor, 1/10 W, 1%	
R5	120 Ω resistor, 1/10 W, 1%	
R6	820 mΩ resistor, 1/2 W, 1%	
R7	10 kΩ resistor, 1/10 W, 1%	
R8	40.2 Ω resistor, 1/10 W, 1%	
D1	Diode, Schottky, 60 V, 5 A, 670 mV @ 5 A	Diodes Incorporated, PDS560-13
D2	Diode, Schottky, 40 V, 1 A, 410 mV @ 1 A	Diodes Incorporated, 1N5819HW-7-F
Q1	Transistor, NPN, 65 V, 0.1 A, SOT23	On Semiconductor, BC846ALT1G
L1	Inductor, 4.7 µH, 9.8 A(sat), 15.32 mΩ (max)	Vishay, IHLP4040DZER4R7M8A

Application 2: Performance

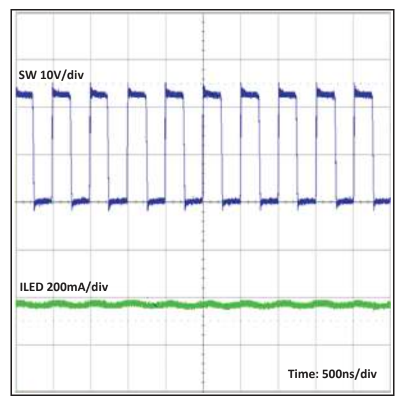
System Efficiency with Full Brightness



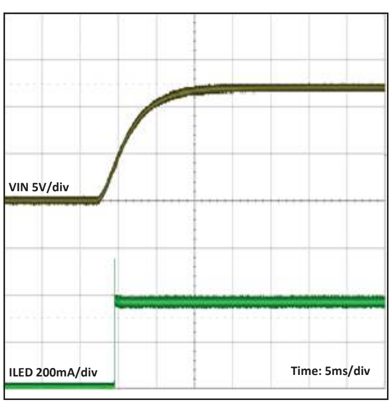
LED Current Line Regulation



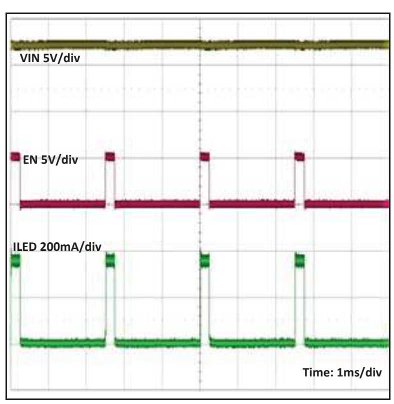
Switching Waveform



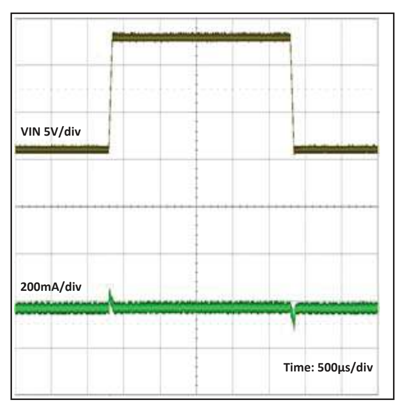
Startup Waveform



10% LED Dimming Waveform

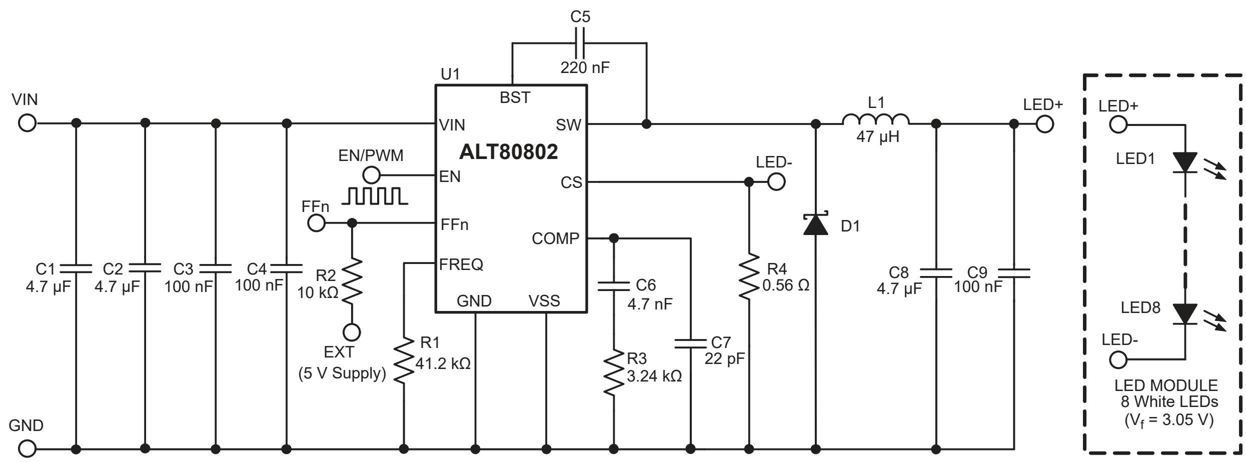


6-18 V Fast VIN Transient



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Application 3: High Input Voltage Buck with 8 White LEDs



Input Range	28-36 V
PWM Dimming Range (200 Hz)	5%-100%

Figure 18: 32 V_{IN}, 400 kHz, 350 mA, 8 White LEDs Buck LED Driver with Fault Flag

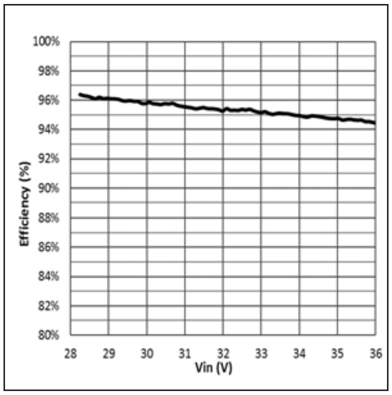
Application 3: Recommended Bill of Materials

Reference	Description	Manufacturer/Part Number
C1, C2, C8	4.7 µF, ceramic capacitor, X7R, 50 V, 1210	
C3, C4, C9	100 nF, ceramic capacitor, X7R, 50 V, 0603	
C5	220 nF, ceramic capacitor, X7R, 16 V, 0402 or 0603	
C6	4.7 nF, ceramic capacitor, X7R, 16 V, 0603	
C7	22 pF, ceramic capacitor, X7R, 16 V, 0603	
R1	41.2 kΩ resistor, 1/10 W, 1%	
R2	10 kΩ resistor, 1/10 W, 1%	
R3	3.24 kΩ resistor, 1/10 W, 1%	
R4	560 mΩ resistor, 1/4 W, 1%	
D1	Diode, Schottky, 60 V, 5 A, 670 mV @ 5 A	Diodes Incorporated, PDS560-13
L1	Inductor, 47 µH, >5 A(sat)	

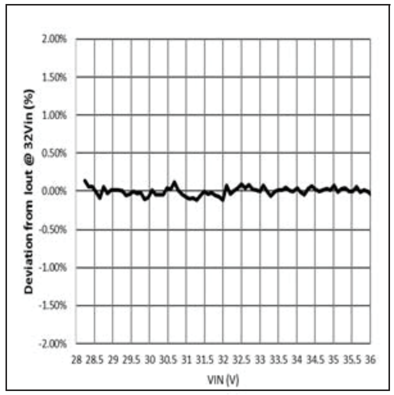
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Application 3: Performance

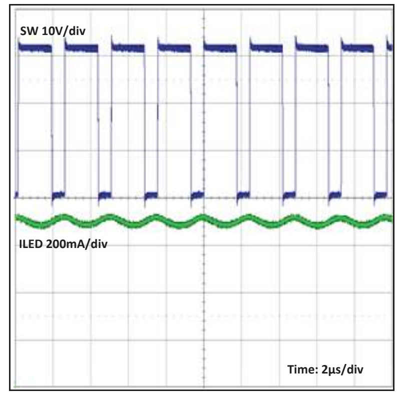
System Efficiency with Full Brightness



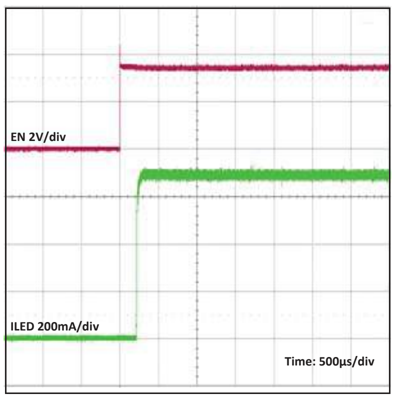
LED Current Line Regulation



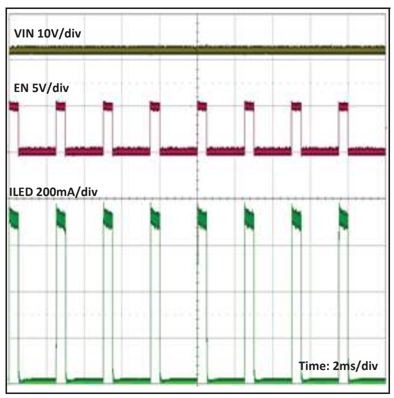
Switching Waveform



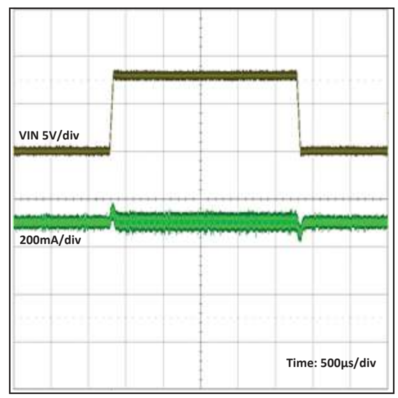
Startup Waveform



20% LED Dimming Waveform

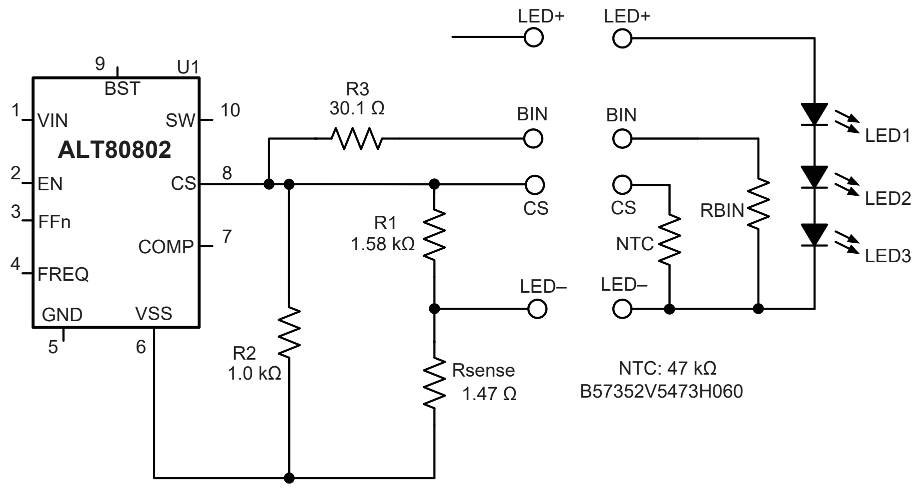


6-18 V Fast VIN Transient



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

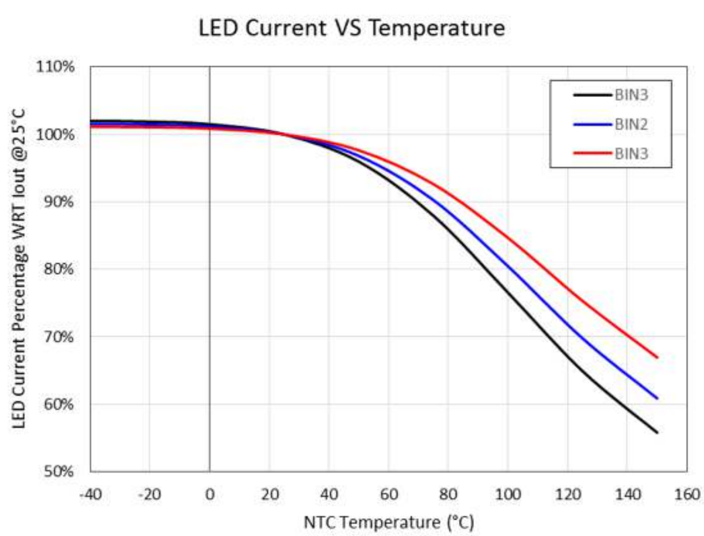
Current Sense Block with NTC and Binning Resistor Example



Binning resistor values for LED current reduction

	BIN1	BIN2	BIN3
LED Current	100%	90%	80%
RBIN	Open	8.06 kΩ	3.24 kΩ

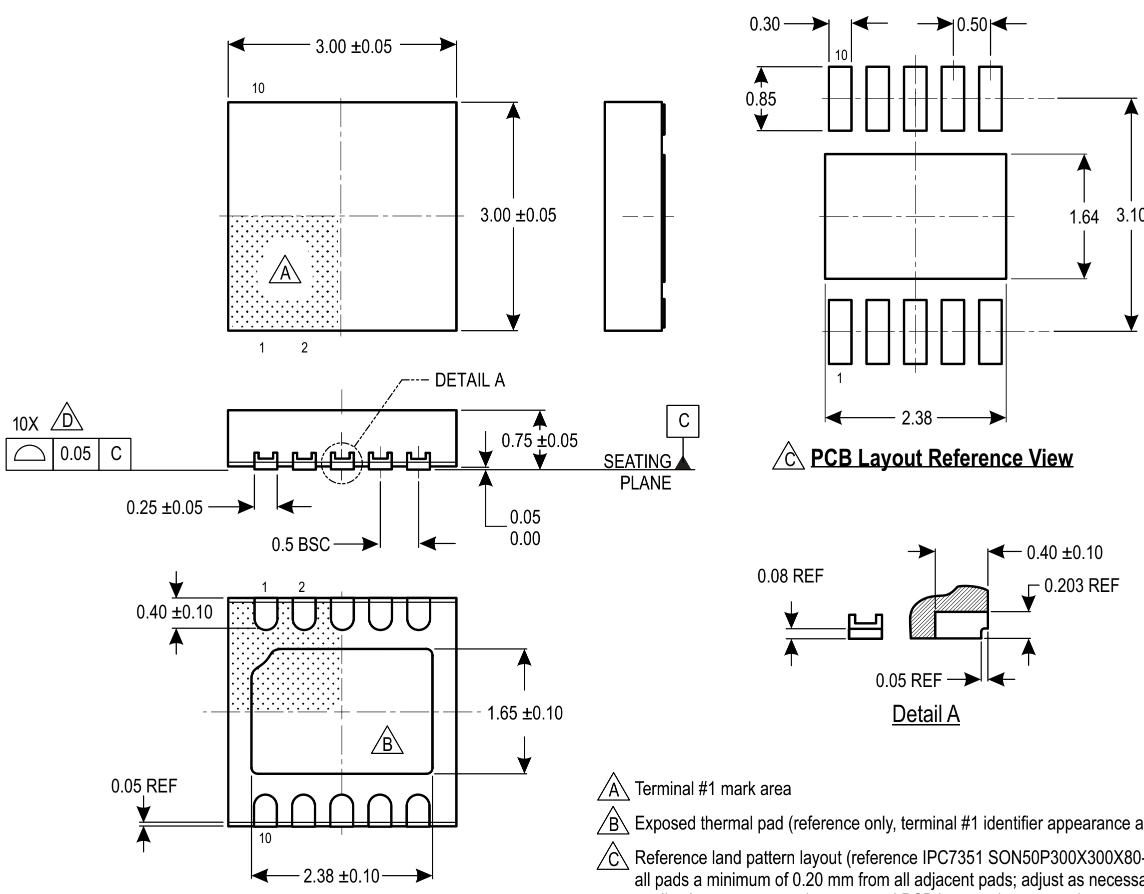
Figure 19: 350 mA Inverting Buck-Boost LED Driver with Binning Resistor on LED Module



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use
(Reference JEDEC MO-229)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Figure 20: Package EJ, 10-Pin DFN with Exposed Thermal Pad and Wettable Flank

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	September 10, 2018	Initial release
1	September 13, 2019	Minor editorial updates
2	September 20, 2022	Updated Features and Benefits (page 1), Input Voltage notes and VSS to GND symbol and rating (page 2), DC Input Voltage (page 2), Figure 3 (page 3), Switch Mode PWM Operation (page 8), Freewheeling Diode Protection (page 11), Output Overvoltage Protection in Buck-Boost (page 11), and Figure 11 (page 20).

For the latest version of this document, visit our website:

www.allegromicro.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com