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June 2015

# FDZ1416NZ

## Common Drain N-Channel 2.5 V PowerTrench® WL-CSP MOSFET

24 V, 7 A, 23 mΩ

### Features

- Max  $r_{S1S2(on)}$  = 23 mΩ at  $V_{GS} = 4.5$  V,  $I_{S1S2} = 1$  A
- Max  $r_{S1S2(on)}$  = 25 mΩ at  $V_{GS} = 4$  V,  $I_{S1S2} = 1$  A
- Max  $r_{S1S2(on)}$  = 28 mΩ at  $V_{GS} = 3.1$  V,  $I_{S1S2} = 1$  A
- Max  $r_{S1S2(on)}$  = 33 mΩ at  $V_{GS} = 2.5$  V,  $I_{S1S2} = 1$  A
- Occupies only 2.2 mm<sup>2</sup> of PCB area
- Ultra-thin package: less than 0.35 mm height when mounted to PCB
- High power and current handling capability
- HBM ESD protection level > 3.2 kV (Note 3)
- RoHS Compliant

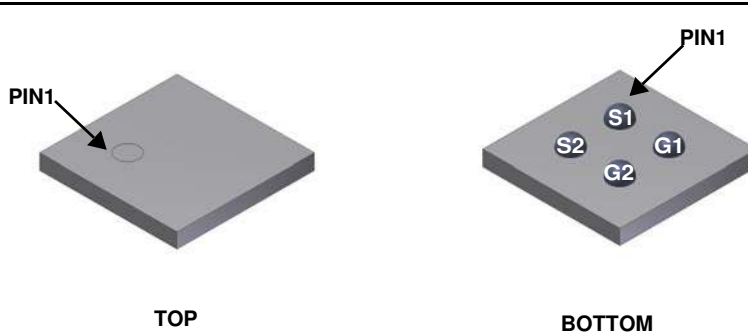


### General Description

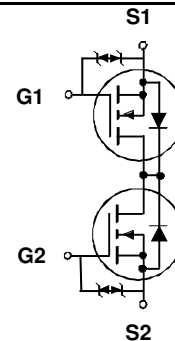
This device is designed specifically as a single package solution for Li-Ion battery pack protection circuit and other ultra-portable applications. It features two common drain N-channel MOSFETs, which enables bidirectional current flow, on Fairchild's advanced PowerTrench® process with state of the art "low pitch" WLCSP packaging process, the FDZ1416NZ minimizes both PCB space and  $r_{S1S2(on)}$ . This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge and low  $r_{S1S2(on)}$ .

### Applications

- Battery management
- Load switch
- Battery protection



WL-CSP 1.4X1.6



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol         | Parameter   | Ratings     | Units            |
|----------------|---|-------------|------------------|
| $V_{S1S2}$     | Source1 to Source2 Voltage  | 24          | V                |
| $V_{GS}$       | Gate to Source Voltage  | $\pm 12$    | V                |
| $I_{S1S2}$     | Source1 to Source2 Current -Continuous $T_A = 25^\circ\text{C}$ (Note 1a) | 7           | A                |
|                | -Pulsed   | 30          |                  |
| $P_D$          | Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)                      | 1.7         | W                |
|                | Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)                      | 0.5         |                  |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range                          | -55 to +150 | $^\circ\text{C}$ |

### Thermal Characteristics

|                 |   |           |     |                    |
|-----------------|---|-----------|-----|--------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 74  | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1b) | 230 |                    |

### Package Marking and Ordering Information

| Device Marking | Device    | Package        | Reel Size | Tape Width | Quantity   |
|----------------|-----------|----------------|-----------|------------|------------|
| EN             | FDZ1416NZ | WL-CSP 1.4X1.6 | 7"        | 8 mm       | 5000 units |

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

### Off Characteristics

|            |  |   |  |  |          |               |
|------------|--|---|--|--|----------|---------------|
| $I_{S1S2}$ | Zero Gate Voltage Source1 to Source2 Current | $V_{S1S2} = 19\text{ V}, V_{GS} = 0\text{ V}$     |  |  | 1        | $\mu\text{A}$ |
| $I_{GSS}$  | Gate to Source Leakage Current               | $V_{GS} = \pm 12\text{ V}, V_{S1S2} = 0\text{ V}$ |  |  | $\pm 10$ | $\mu\text{A}$ |

### On Characteristics

|                |   |   |     |     |     |            |
|----------------|---|---|-----|-----|-----|------------|
| $V_{GS(th)}$   | Gate to Source Threshold Voltage        | $V_{GS} = V_{S1S2}, I_{S1S2} = 250\text{ }\mu\text{A}$                          | 0.4 | 0.9 | 1.3 | V          |
| $r_{S1S2(on)}$ | Static Source1 to Source2 On Resistance | $V_{GS} = 4.5\text{ V}, I_{S1S2} = 1\text{ A}$                                  | 9   | 16  | 23  | m $\Omega$ |
|                |   | $V_{GS} = 4\text{ V}, I_{S1S2} = 1\text{ A}$                                    | 10  | 17  | 25  |            |
|                |   | $V_{GS} = 3.1\text{ V}, I_{S1S2} = 1\text{ A}$                                  | 11  | 19  | 28  |            |
|                |   | $V_{GS} = 2.5\text{ V}, I_{S1S2} = 1\text{ A}$                                  | 12  | 22  | 33  |            |
|                |   | $V_{GS} = 4.5\text{ V}, I_{S1S2} = 1\text{ A}, T_J = 125\text{ }^\circ\text{C}$ |     | 24  | 36  |            |
| $g_{FS}$       | Forward Transconductance                | $V_{S1S2} = 5\text{ V}, I_{S1S2} = 1\text{ A}$                                  |     | 4.5 |     | S          |

### Dynamic Characteristics

|           |                              |  |  |      |      |    |
|-----------|------------------------------|--|--|------|------|----|
| $C_{iss}$ | Input Capacitance            | $V_{S1S2} = 12\text{ V}, V_{GS} = 0\text{ V},$<br>$f = 1\text{ MHz}$ |  | 1140 | 1515 | pF |
| $C_{oss}$ | Output Capacitance           |  |  | 136  | 220  | pF |
| $C_{rss}$ | Reverse Transfer Capacitance |  |  | 129  | 205  | pF |

### Switching Characteristics

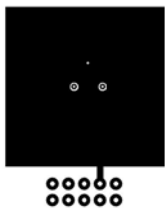
|              |                                 |  |  |     |    |    |
|--------------|---------------------------------|--|--|-----|----|----|
| $t_{d(on)}$  | Turn-On Delay Time              | $V_{S1S2} = 12\text{ V}, I_{S1S2} = 1\text{ A},$<br>$V_{GS} = 4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$ |  | 9.5 | 19 | ns |
| $t_r$        | Rise Time                       |  |  | 12  | 22 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time             |  |  | 37  | 59 | ns |
| $t_f$        | Fall Time                       |  |  | 16  | 33 | ns |
| $Q_g$        | Total Gate Charge               |  |  | 12  | 17 | nC |
| $Q_{gs}$     | Gate to Source1 Gate Charge     | $V_{S1S2} = 12\text{ V}, I_{S1S2} = 1\text{ A},$<br>$V_{G1S1} = 4.5\text{ V}, V_{G2S2} = 0\text{ V}$   |  | 1.6 |    | nC |
| $Q_{gd}$     | Gate to Source2 "Miller" Charge |  |  | 3.7 |    | nC |

### Source1 to Source2 Diode Characteristics

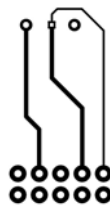
|           |   |  |  |     |     |   |
|-----------|---|--|--|-----|-----|---|
| $I_{fss}$ | Maximum Continuous Source1 to Source2 Diode Forward Current |  |  | 1   | A   |   |
| $V_{fss}$ | Source1 to Source2 Diode Forward Voltage                    | $V_{G1S1} = 0\text{ V}, V_{G2S2} = 4.5\text{ V},$<br>$I_{fss} = 1\text{ A}$ (Note 2) |  | 0.7 | 1.2 | V |

#### Notes:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 74 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper

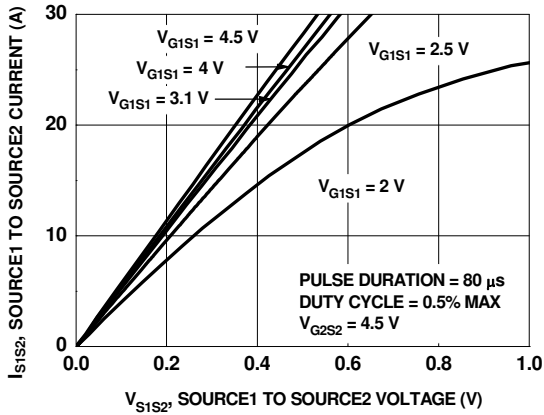


b. 230 °C/W when mounted on a minimum pad of 2 oz copper

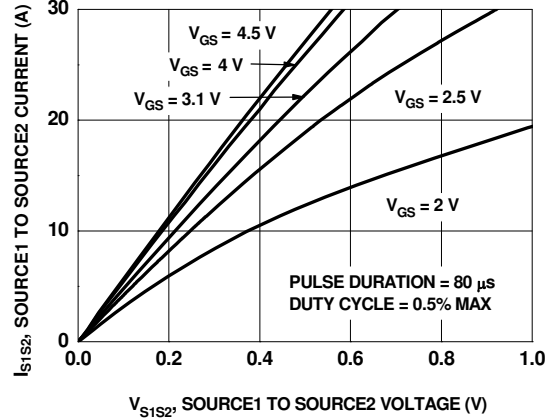
- Pulse Test: Pulse Width < 300 us, Duty cycle < 2.0%.

- The diode connected between the gate and source serves only protection against ESD. No gate overvoltage rating is implied.

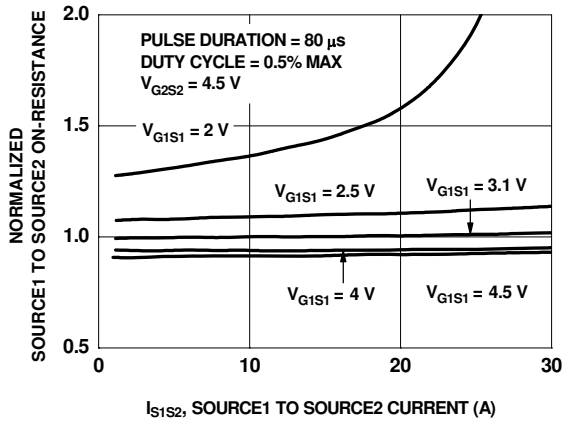
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



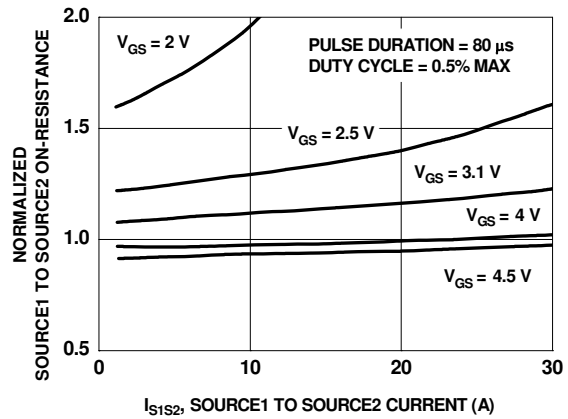
**Figure 1. On-Region Characteristics**



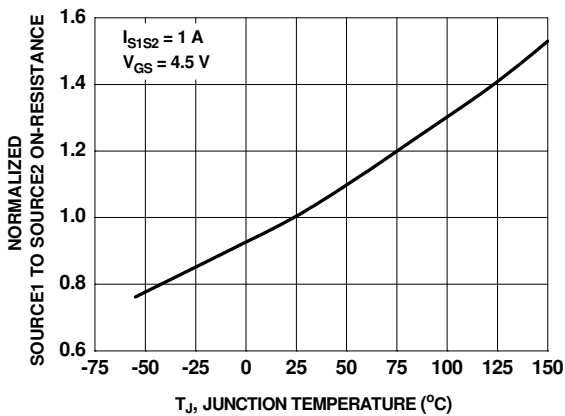
**Figure 2. On-Region Characteristics**



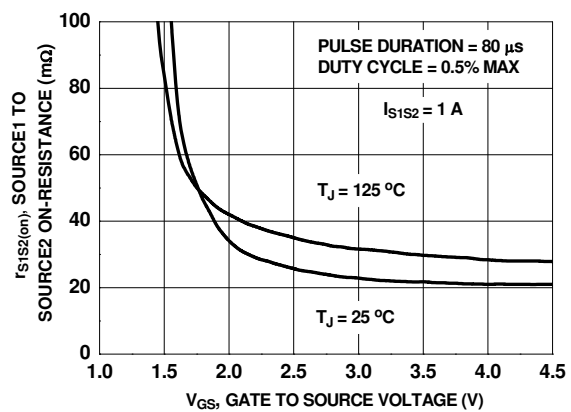
**Figure 3. Normalized On-Resistance vs. Source1 to Source2 Current and Gate Voltage**



**Figure 4. Normalized On-Resistance vs. Source1 to Source2 Current and Gate Voltage**

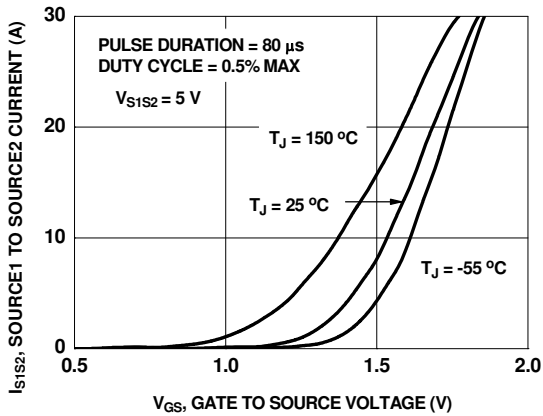


**Figure 5. Normalized On Resistance vs. Junction Temperature**

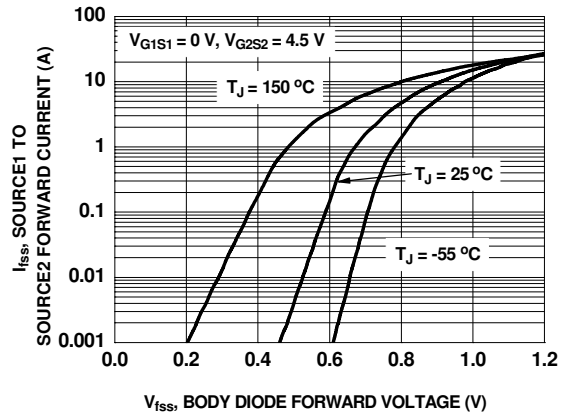


**Figure 6. On Resistance vs. Gate to Source Voltage**

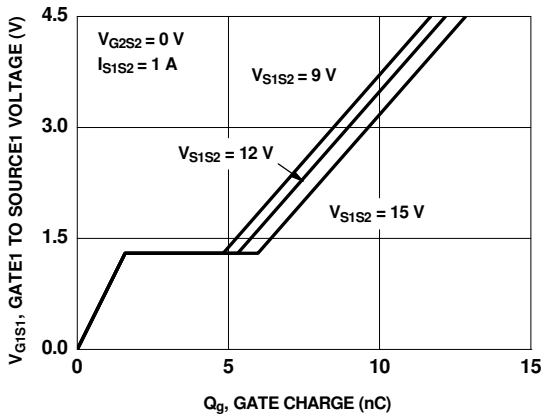
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



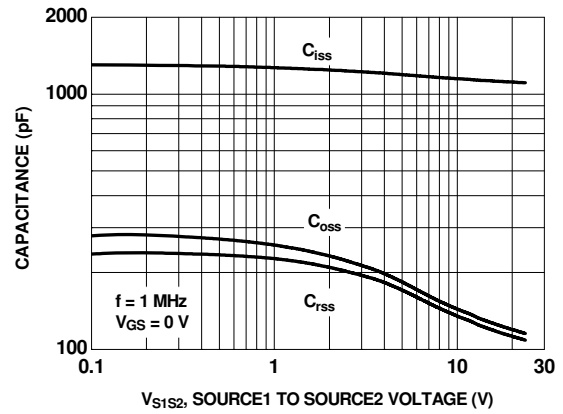
**Figure 7. Transfer Characteristics**



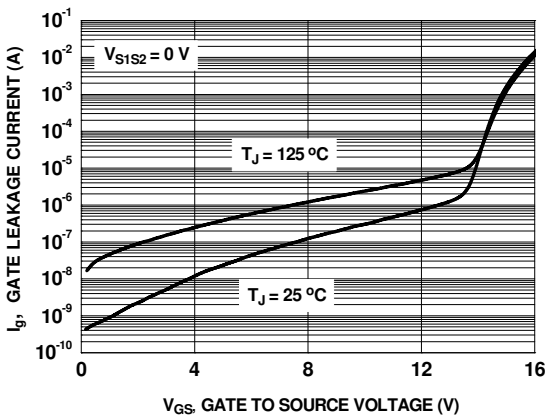
**Figure 8. Source1 to Source2 Diode Forward Voltage vs Source Current**



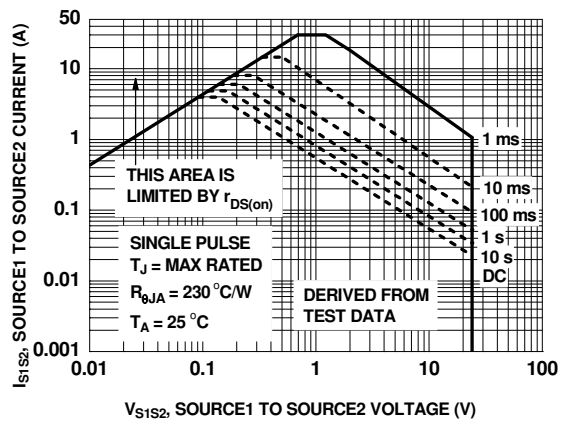
**Figure 9. Gate Charge Characteristics**



**Figure 10. Capacitance vs Source1 to Source2 Voltage**



**Figure 11. Gate Leakage Current vs Gate to Source Voltage**



**Figure 12. Forward Bias Safe Operating Area**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

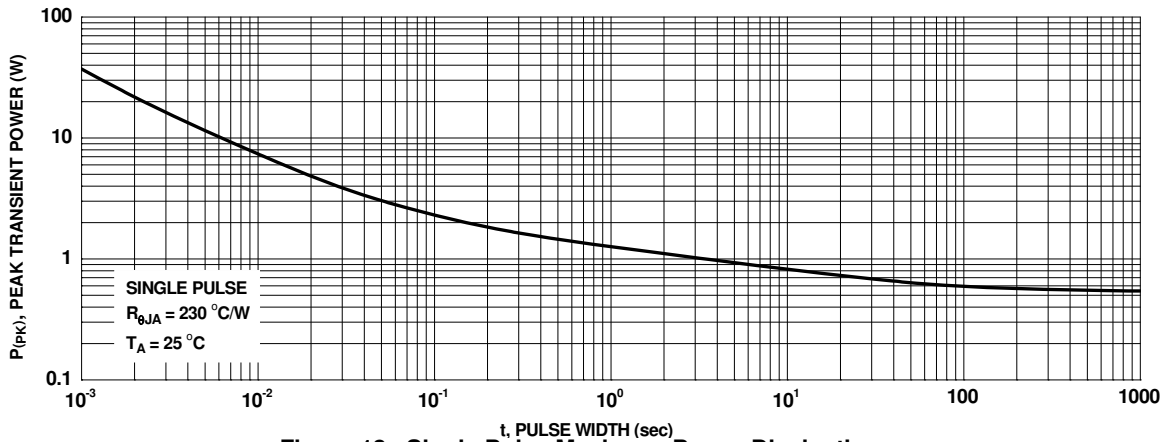


Figure 13. Single Pulse Maximum Power Dissipation

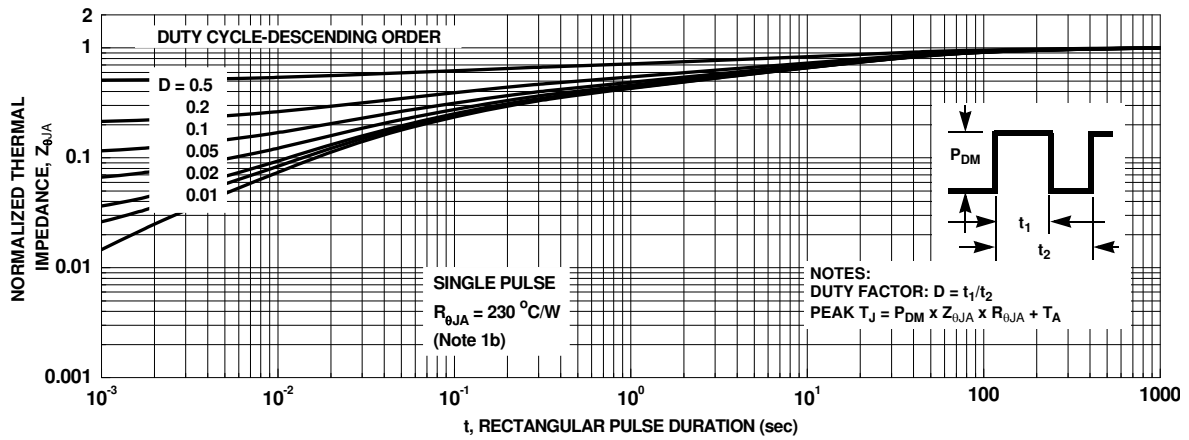


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

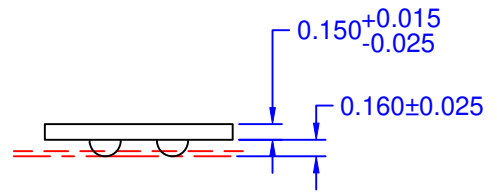
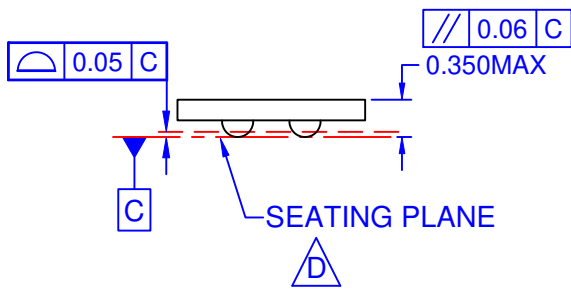
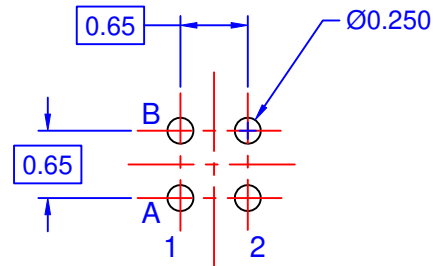
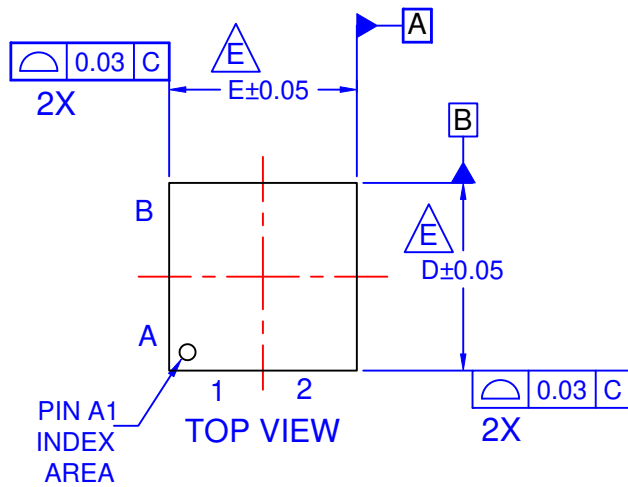
The following information applies to the WL-CSP package dimensions on the next page:

**Pin Definitions:**

|          |    |    |    |    |
|----------|----|----|----|----|
| Pin Name | G1 | G2 | S1 | S2 |
| Position | A2 | B2 | A1 | B1 |

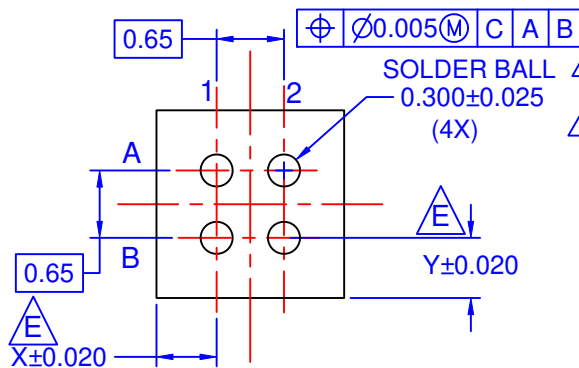
**Product Specific Dimensions:**

|        |        |          |          |
|--------|--------|----------|----------|
| D      | E      | X        | Y        |
| 1.4 mm | 1.6 mm | 0.475 mm | 0.375 mm |



NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. FOR DIMENSIONS D,E,X AND Y SEE PRODUCT DATA SHEET.
- F. FOR PIN-OUT ASSIGNMENT, REFER TO DATA SHEET.
- G. DRAWING NAME: MKT-UC004AJREV2.



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