

P-Channel NexFET™ Power MOSFET

FEATURES

- **Ultralow Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 2-mm × 2-mm Plastic Package**

APPLICATIONS

- **Battery Management**
- **Load Management**
- **Battery Protection**

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile. Low on resistance coupled with the extremely small footprint and low profile make the device ideal for battery operated space constrained applications.

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	-20	V
Q_g	Gate Charge Total (-4.5V)	2.6	nC
Q_{gd}	Gate Charge Gate to Drain	0.5	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -1.8V$	71 mΩ
		$V_{GS} = -2.5V$	56 mΩ
		$V_{GS} = -4.5V$	39 mΩ
$V_{GS(th)}$	Threshold Voltage	-0.65	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD25302Q2	SON 2-mm × 2-mm Plastic Package	13-Inch Reel	3000	Tape and Reel

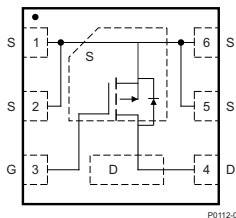
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	-5	A
	Continuous Drain Current ⁽¹⁾	-5	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	-20	A
P_D	Power Dissipation	2.4	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

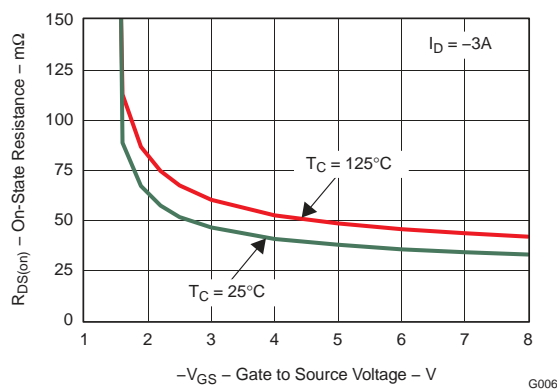
(1) Package Limited

(2) Pulse duration 10 μs , duty cycle $\leq 2\%$

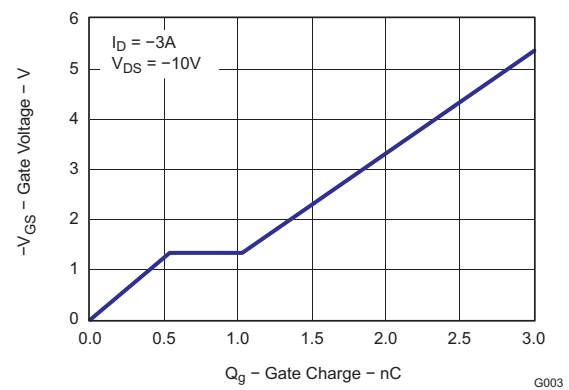
Top View



$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise specified

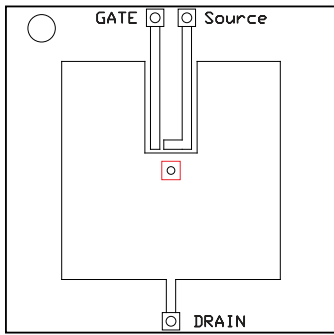
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_{DS} = -250\mu A$	-20			V
I_{DSS}	Drain to Source Leakage	$V_{GS} = 0V, V_{DS} = -16V$			-1	μA
I_{GSS}	Gate to Source Leakage	$V_{DS} = 0V, V_{GS} = \pm 8V$			-100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = -250\mu A$	-0.5	-0.65	-0.9	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -1.8V, I_{DS} = -3.0A$		71	92	m Ω
		$V_{GS} = -2.5V, I_{DS} = -3.0A$		56	70	m Ω
		$V_{GS} = -4.5V, I_{DS} = -3.0A$		39	49	m Ω
g_{fs}	Transconductance	$V_{DS} = -10V, I_{DS} = -3.0A$		12.3		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		270	350	pF
C_{OSS}	Output Capacitance			120	150	pF
C_{RSS}	Reverse Transfer Capacitance			40	55	pF
Q_g	Gate Charge Total (-4.5V)	$V_{DS} = -10V, I_{DS} = -3.0A$		2.6	3.4	nC
Q_{gd}	Gate Charge – Gate to Drain			0.5		nC
Q_{gs}	Gate Charge Gate to Source			0.54		nC
$Qg(th)$	Gate Charge at V_{th}			0.2		nC
Q_{OSS}	Output Charge	$V_{DS} = -13V, V_{GS} = 0V$		2.3		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = -10V, V_{GS} = -4.5V, I_{DS} = -3.0A, R_G = 2\Omega$		3.2		ns
t_r	Rise Time			13.2		ns
$t_{d(off)}$	Turn Off Delay Time			8.6		ns
t_f	Fall Time			1.3		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{DS} = -3.0A, V_{GS} = 0V$	-0.8	-1.0		V
Q_{rr}	Reverse Recovery Charge	$V_{dd} = -13V, I_F = -3.0A, di/dt = 300A/\mu s$		2.5		nC
t_{rr}	Reverse Recovery Time			8.8		ns

THERMAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise specified

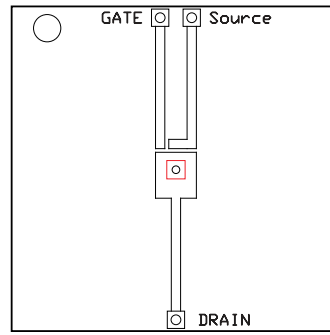
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			8.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			66	$^\circ\text{C/W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 66^\circ\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

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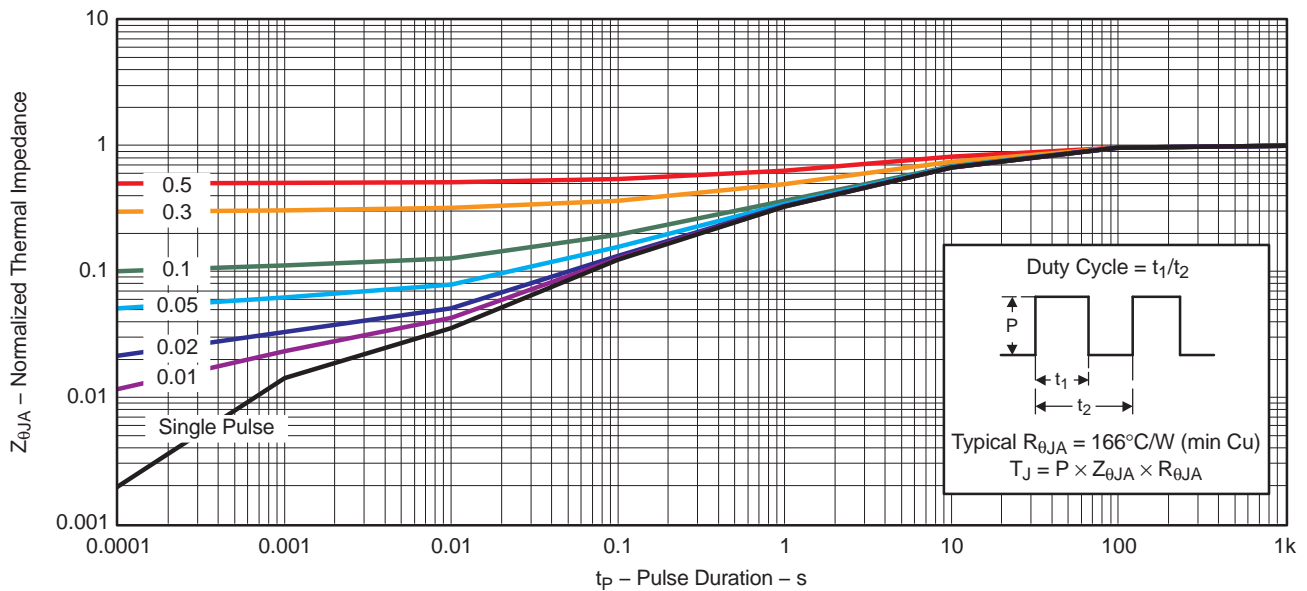


Max $R_{\theta JA} = 207^\circ\text{C/W}$
when mounted on
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

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TYPICAL MOSFET CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise specified



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

T_A = 25°C, unless otherwise specified

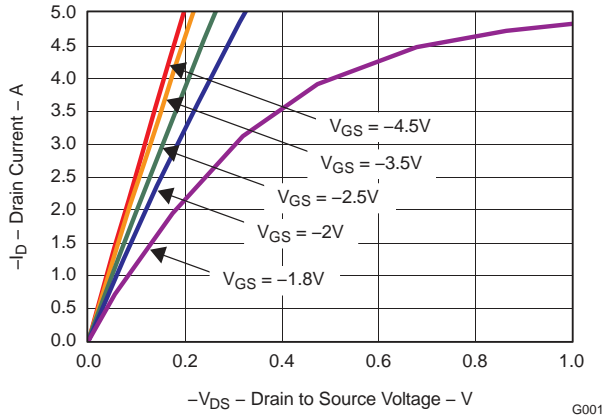


Figure 2. Saturation Characteristics

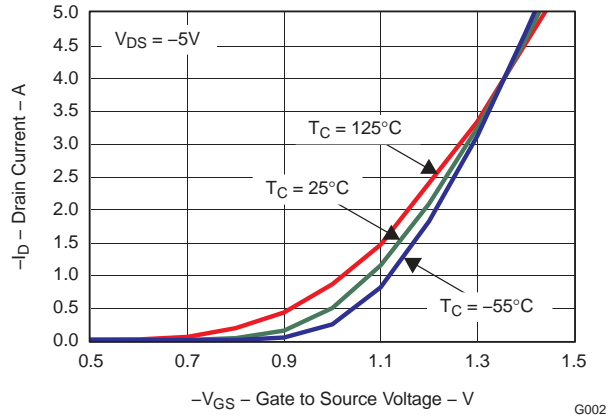


Figure 3. Transfer Characteristics

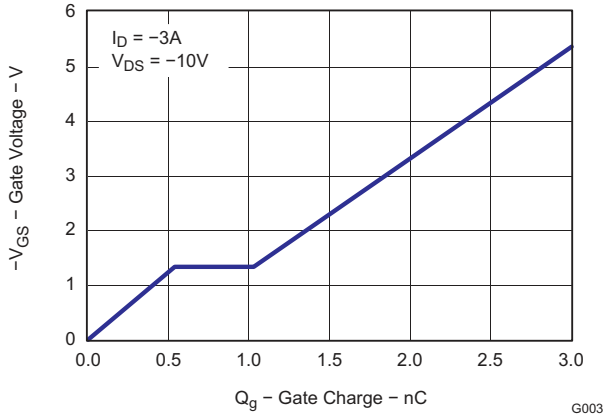


Figure 4. Gate Charge

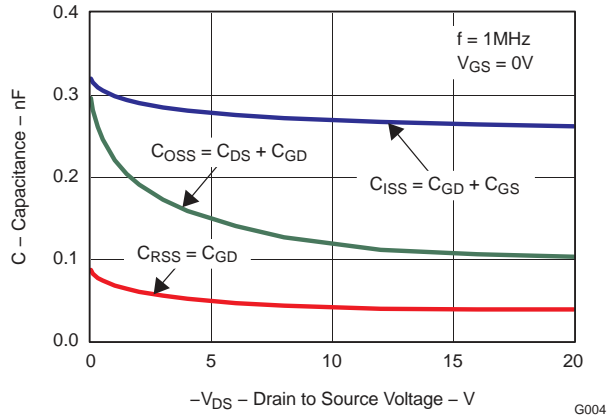


Figure 5. Capacitance

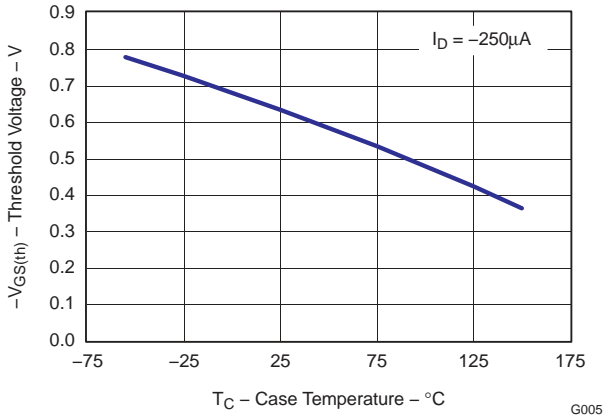


Figure 6. Threshold Voltage vs. Temperature

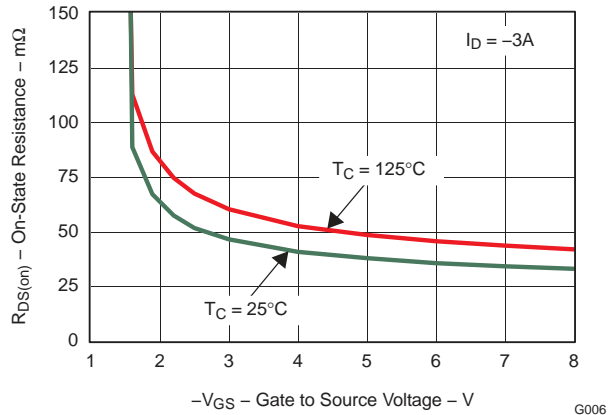


Figure 7. On-State Resistance vs. Gate to Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, unless otherwise specified

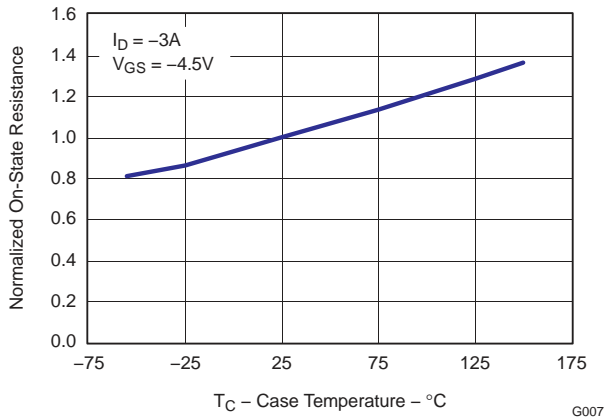


Figure 8. Normalized On-State Resistance vs. Temperature

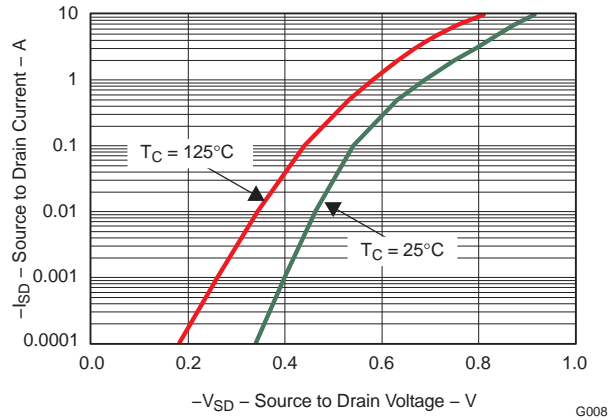


Figure 9. Typical Diode Forward Voltage

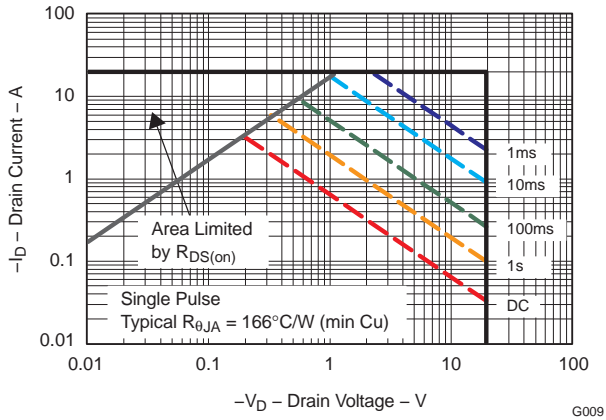


Figure 10. Maximum Safe Operating Area

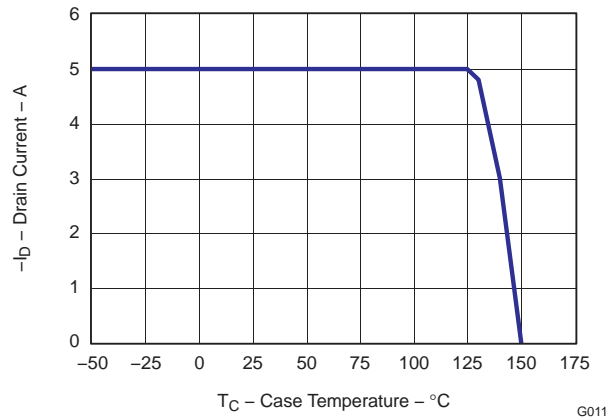
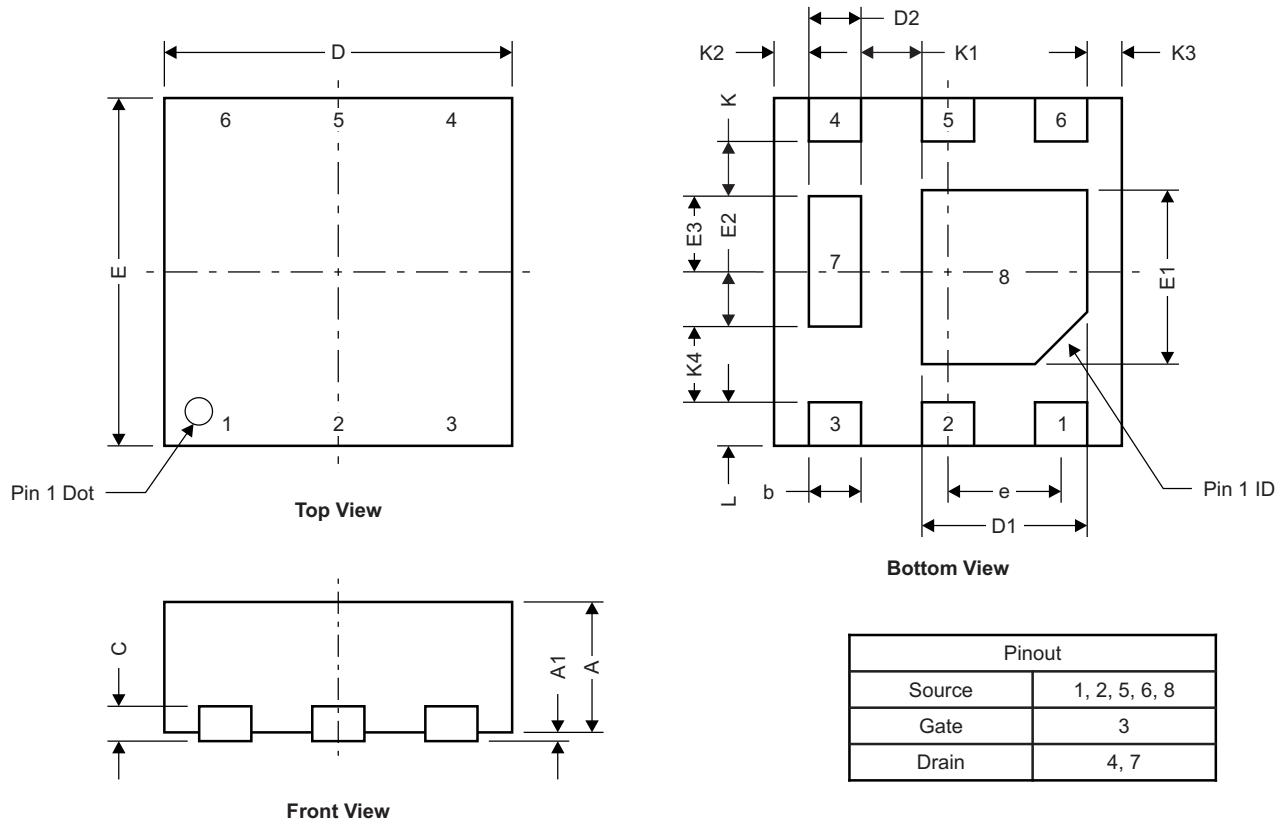


Figure 11. Maximum Drain Current vs. Temperature

MECHANICAL DATA

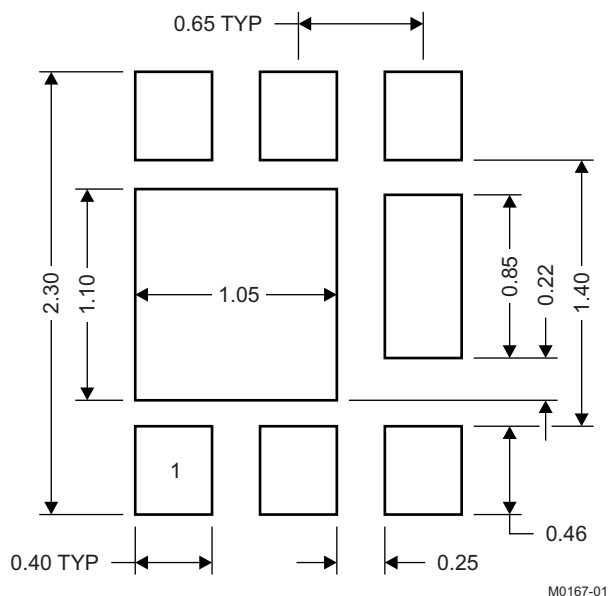
Q2 Package Dimensions



M0175-01

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C	0.203 TYP			0.008 TYP		
D	2.000 TYP			0.080 TYP		
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2	0.300 TYP			0.012 TYP		
E	2.000 TYP			0.080 TYP		
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2	0.280 TYP			0.0112 TYP		
E3	0.470 TYP			0.0188 TYP		
e	0.650 BSC			0.026 TYP		
K	0.280 TYP			0.0112 TYP		
K1	0.350 TYP			0.014 TYP		
K2	0.200 TYP			0.008 TYP		
K3	0.200 TYP			0.008 TYP		
K4	0.470 TYP			0.0188 TYP		
L	0.200	0.25	0.300	0.008	0.010	0.0121

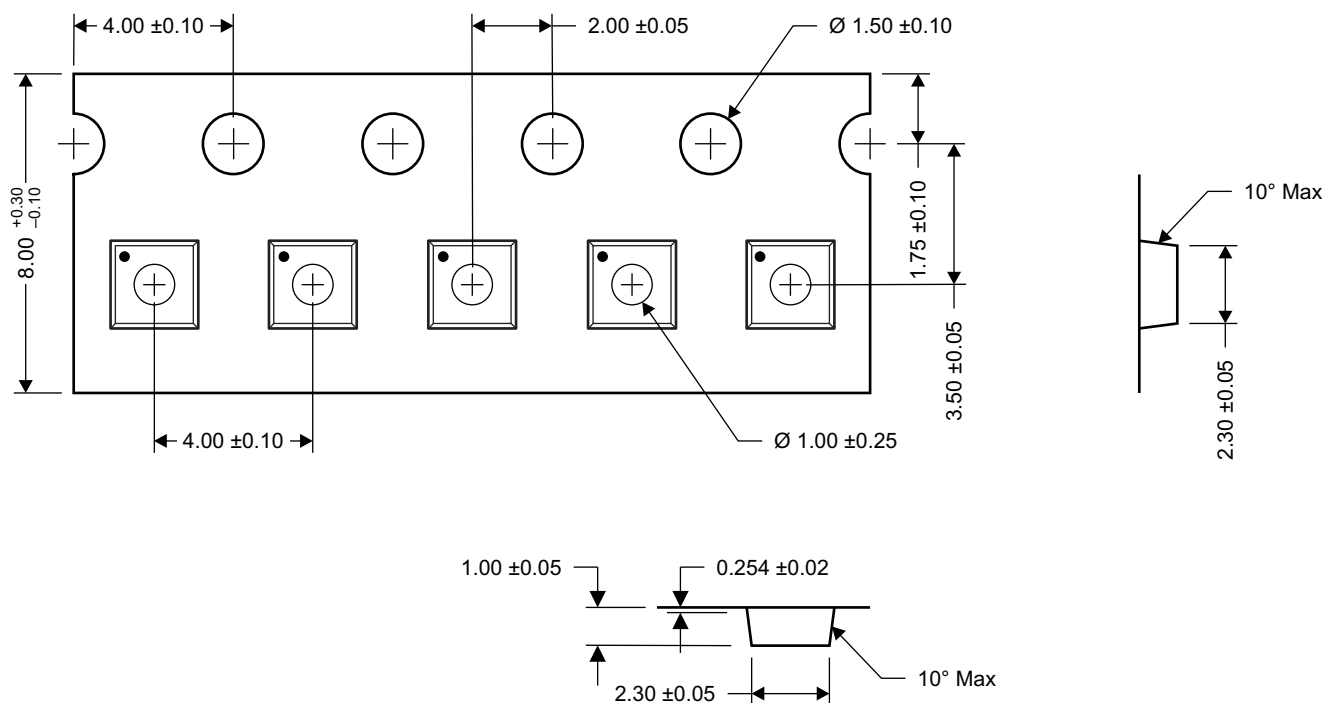
Recommended PCB Pattern



Note: All dimensions are in mm, unless otherwise specified.

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing through PCB Layout Techniques](#).

Q2 Tape and Reel Information



- Notes:
1. Measured from centerline of sprocket hole to centerline of pocket
 2. Cumulative tolerance of 10 sprocket holes is ± 0.20
 3. Other material available
 4. Typical SR of form tape Max 10^8 OHM/SQ
 5. All dimensions are in mm, unless otherwise specified.

REVISION HISTORY

Changes from Original (November 2009) to Revision A **Page**

- Deleted the Package Marking Information section **8**
-

Changes from Revision A (October 2010) to Revision B **Page**

- Added ESDS statement **2**
-

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