



# P-Channel Enhancement-Mode Vertical DMOS FET

## Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{ISS}$  and fast switching speeds
- ▶ High input impedance and high gain
- ▶ Excellent thermal stability
- ▶ Integral source-to-drain diode

## Applications

- ▶ Motor controls
- ▶ Converters, amplifiers, and switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

## General Description

The Supertex VP2206 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Ordering Information

Part Number	Package Option	Packing
VP2206N2-G	TO-39	500/Bag
VP2206N3-G	TO-92	1000/Bag
VP2206N3-G P002	TO-92	2000/Reel
VP2206N3-G P003		
VP2206N3-G P005		
VP2206N3-G P013		
VP2206N3-G P014		

-G denotes a lead (Pb)-free / RoHS compliant package.  
 Contact factory for Wafer / Die availability.  
 Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

## Product Summary

$BV_{DSS}/BV_{DGS}$	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)
-60V	0.9Ω	-4.0A

## Absolute Maximum Ratings

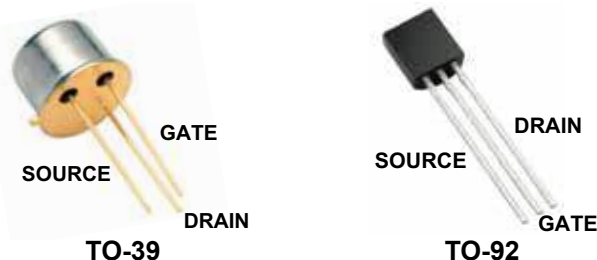
Parameter	Value
Drain-to-source voltage	$BV_{DSS}$
Drain-to-gate voltage	$BV_{DGS}$
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

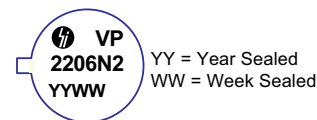
## Typical Thermal Resistance

Package	$\theta_{ja}$
TO-39	N/A
TO-92	132°C/W

## Pin Configuration

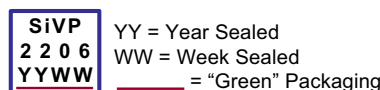


## Product Marking



Package may or may not include the following marks: Si or

TO-39



Package may or may not include the following marks: Si or

TO-92

### Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup>	$I_D$ (pulsed)	Power Dissipation @ $T_c = 25^\circ\text{C}$	$I_{DR}$ <sup>†</sup>	$I_{DRM}$
TO-39	-750mA	-8.0A	0.36W	-750mA	-8.0A
TO-92	-640mA	-4.0	0.74W	-640mA	-4.0

**Notes:**

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .

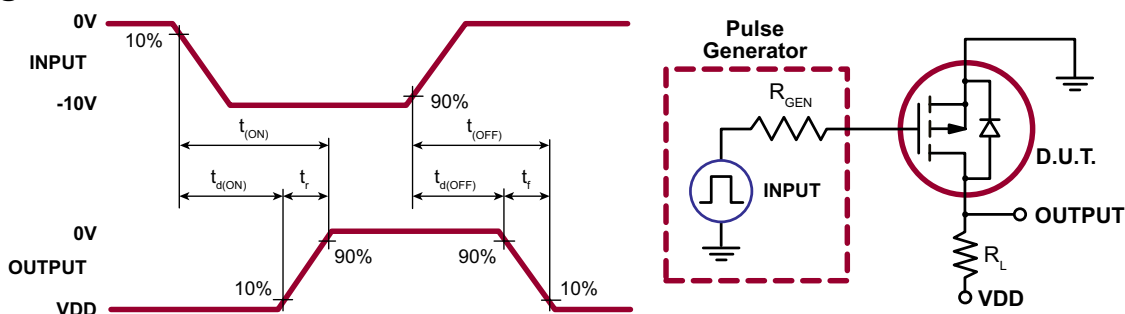
### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	-60	-	-	V	$V_{GS} = 0V, I_D = -10mA$
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-3.5	V	$V_{GS} = V_{DS}, I_D = -10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-4.3	-5.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -10mA$
$I_{GSS}$	Gate body leakage	-	-1.0	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero gate voltage drain current	-	-	-50	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
		-	-	-10	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	-0.85	-2.0	-		$V_{GS} = -5.0V, V_{DS} = -25V$
		-4.0	-9.0	-	A	$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	1.3	1.5	$\Omega$	$V_{GS} = -5.0V, I_D = -1.0A$
		-	0.75	0.9		$V_{GS} = -10V, I_D = -3.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.85	1.2	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -3.5A$
$G_{FS}$	Forward transductance	800	1400	-	mmho	$V_{DS} = -25V, I_D = -2.0A$
$C_{ISS}$	Input capacitance	-	325	450	pF	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz$
$C_{OSS}$	Common source output capacitance	-	125	180		
$C_{RSS}$	Reverse transfer capacitance	-	30	40		
$t_{d(ON)}$	Turn-on delay time	-	4.0	15	ns	$V_{DD} = -25V, I_D = -4.0A, R_{GEN} = 10\Omega$
$t_r$	Rise time	-	16	25		
$t_{d(OFF)}$	Turn-off delay time	-	16	50		
$t_f$	Fall time	-	22	50		
$V_{SD}$	Diode forward voltage drop	-	-1.1	-1.6	V	$V_{GS} = 0V, I_{SD} = -3.5A$
$t_{rr}$	Reverse recovery time	-	500	-	ns	$V_{GS} = 0V, I_{SD} = -1.0A$

**Notes:**

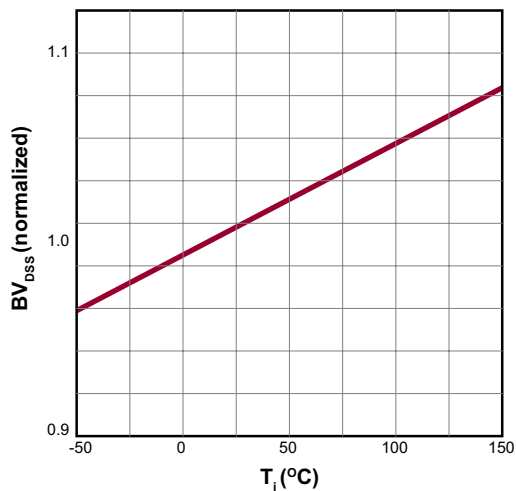
1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

### Switching Waveforms and Test Circuit

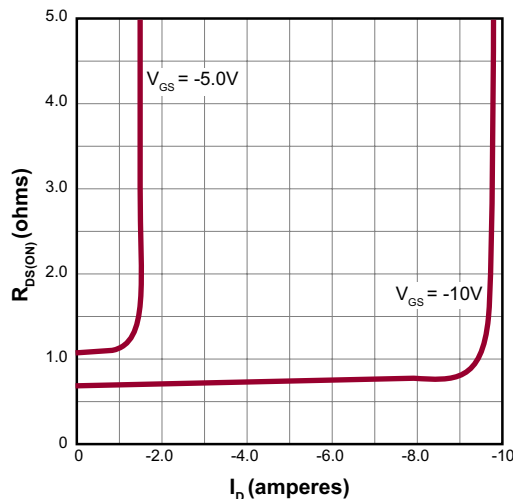


# Typical Performance Curves

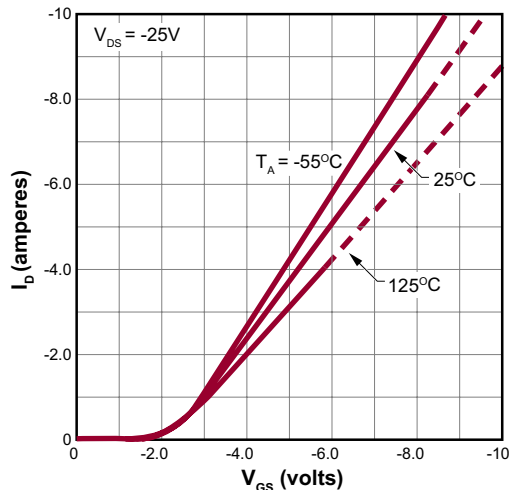
**BV<sub>DSS</sub> Variation with Temperature**



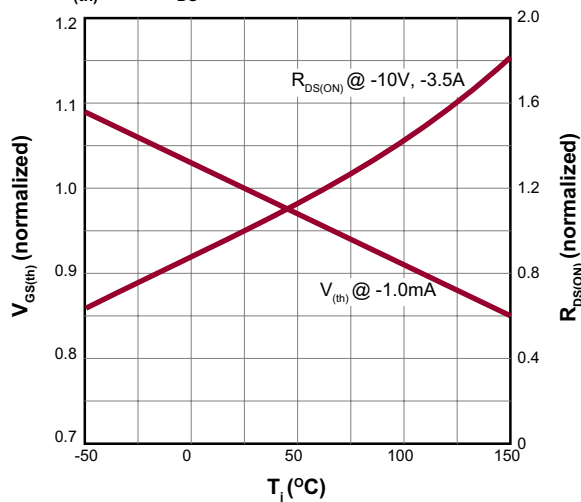
**On-Resistance vs. Drain Current**



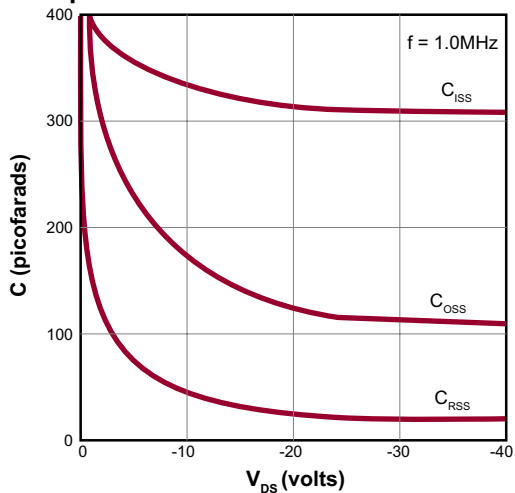
**Transfer Characteristics**



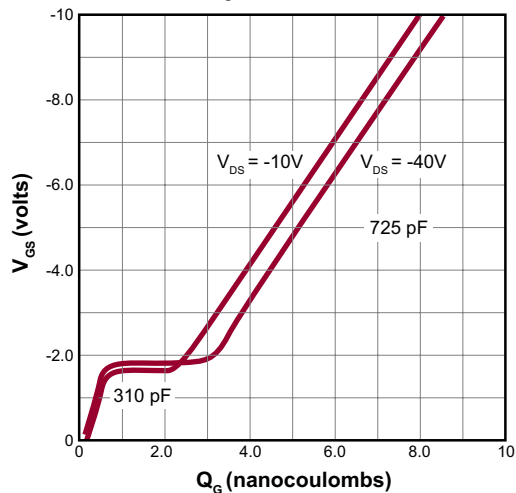
**V<sub>(th)</sub> and R<sub>DS</sub> Variation with Temperature**



**Capacitance vs. Drain-to-Source Voltage**

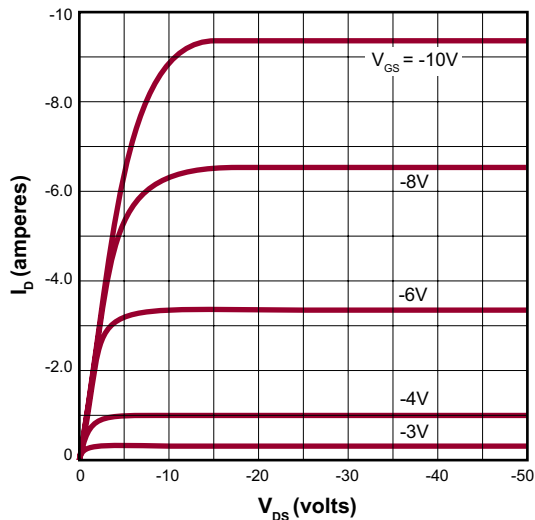


**Gate Drive Dynamic Characteristics**

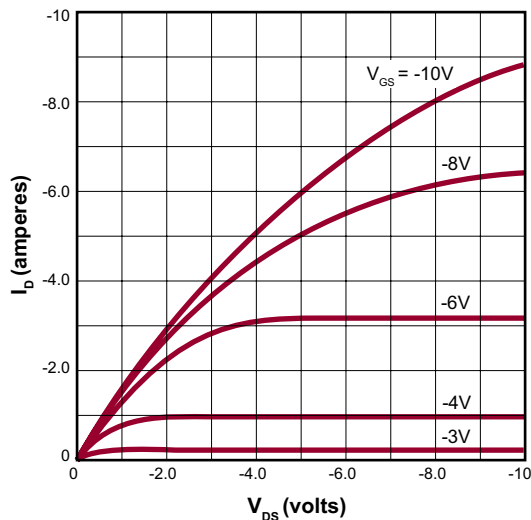


Typical Performance Curves (cont.)

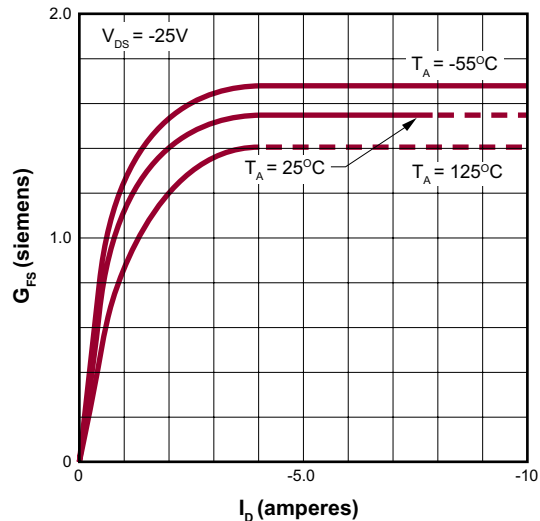
Output Characteristics



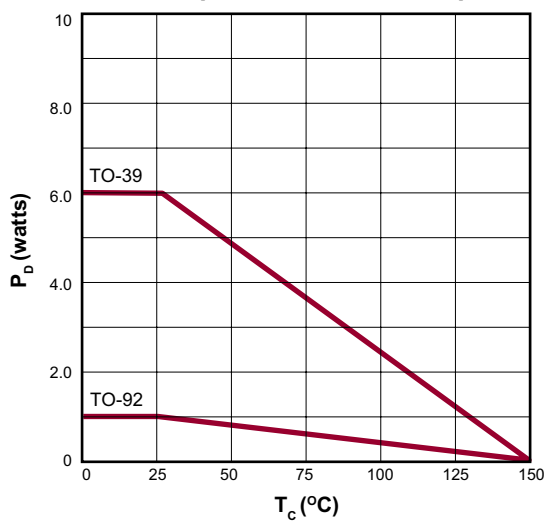
Saturation Characteristics



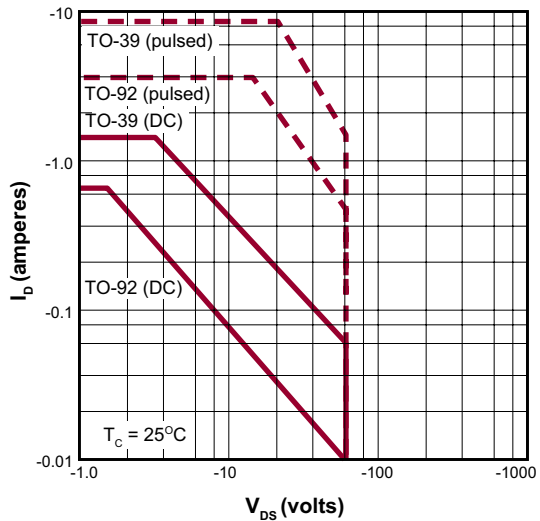
Transconductance vs. Drain Current



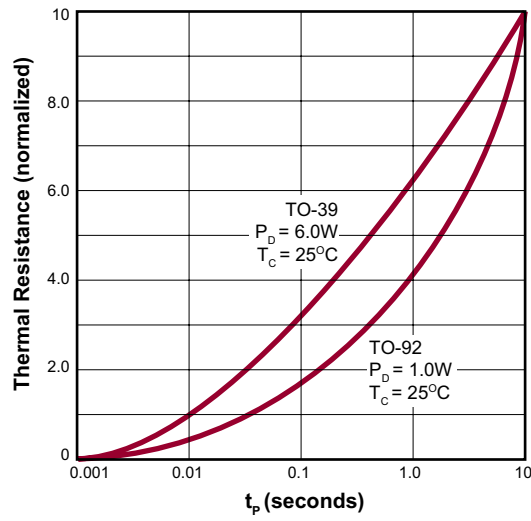
Power Dissipation vs. Case Temperature



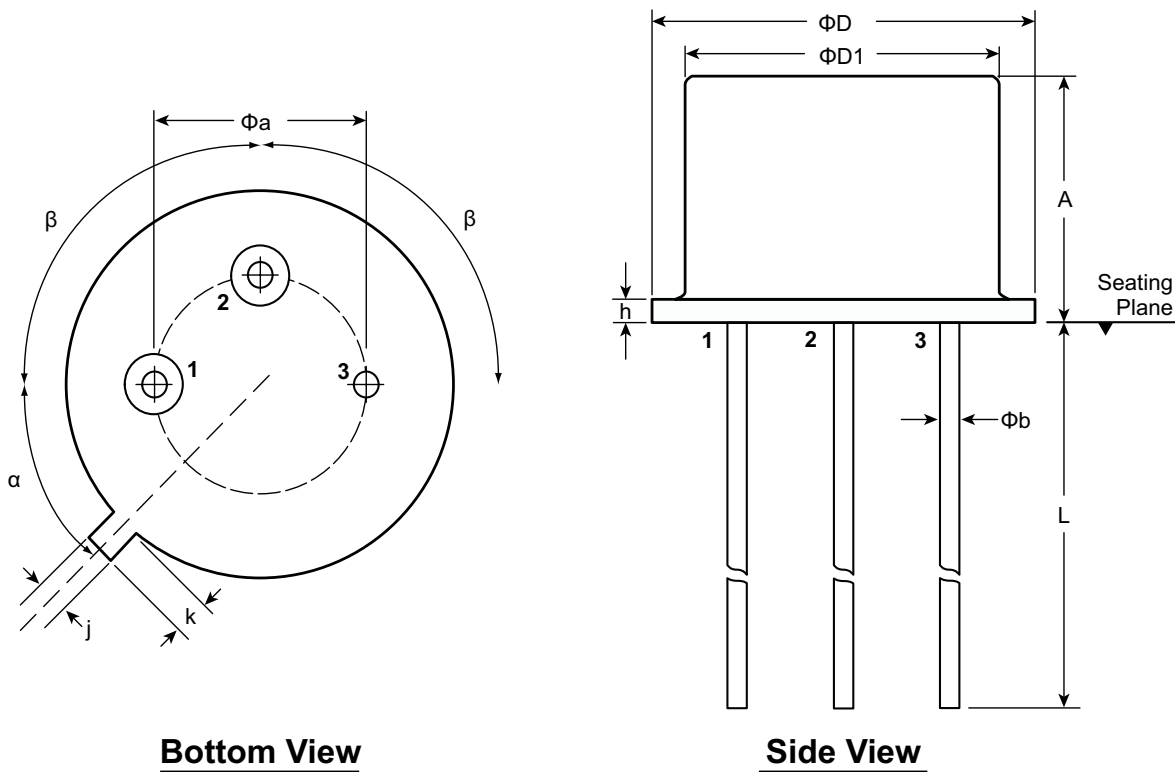
Maximum Rated Safe Operating Area



Thermal Response Characteristics



### 3-Lead TO-39 Package Outline (N2)



**Bottom View**

**Side View**

Symbol	$\alpha$	$\beta$	A	$\phi_a$	$\phi_b$	$\phi_D$	$\phi_{D1}$	h	j	k	L	
Dimension (inches)	MIN	45° NOM	90° NOM	.240	.190	.016	.350	.315	.009	.028	.029	.500
	NOM			-	-	-	-	-	-	-	-	-
	MAX			.260	.210	.021	.370	.335	.125	.034	.040	.560*

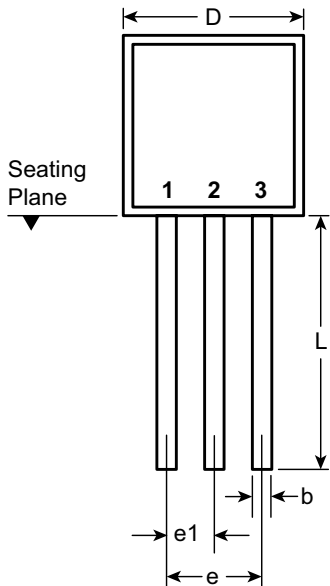
JEDEC Registration TO-39.

\* This dimension is not specified in the JEDEC drawing.

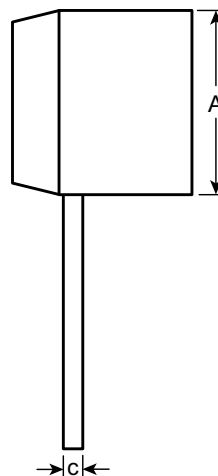
Drawings not to scale.

Supertex Doc. #: DSPD-3TO39N2, Version B052009.

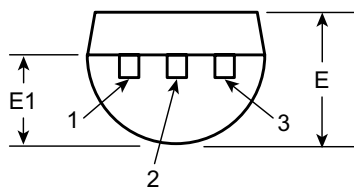
### 3-Lead TO-92 Package Outline (N3)



**Front View**



**Side View**



**Bottom View**

Symbol	A	b	c	D	E	E1	e	e1	L	
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

**Supertex inc.** does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." **Supertex inc.** does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the **Supertex inc.** (website: <http://www.supertex.com>)