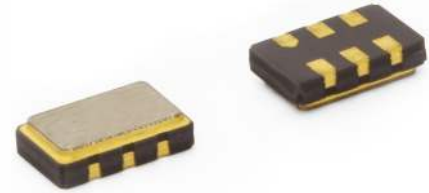


# Model 653

## Very Low Jitter LVPECL or LVDS Clock

### Features

- Ceramic Surface Mount Package
- Very Low Phase Jitter Performance, 500fs Maximum
- Fundamental or 3<sup>rd</sup> Overtone Crystal Design
- Frequency Range 10 – 320MHz \*
- +2.5V or +3.3V Operation [+1.8V LVDS only]
- Output Enable Standard
- Tape and Reel Packaging, EIA-481



Part Dimensions:  
5.0 × 3.2 × 1.2mm • 62.00mg

### Standard Frequencies

\* See Page 10 for common frequencies.  
Check with factory for availability of frequencies not listed.

### Applications

- SerDes
- Storage Area Networking
- Broadband Access
- SONET/SDH/DWDM
- PON
- Ethernet/Gbe/SyncE
- Fiber Channel
- Medical Electronics
- Test and Measurement

### Description

CTS Model 653 is a low cost, high performance clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M653 has excellent stability and very low jitter/phase noise performance.

### Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging
653	P	XXX or XXXX	3	G	3	T
		Code    Frequency Product Frequency Code <sup>1</sup>		Code    Temp. Range A    -10°C to +60°C C    -20°C to +70°C I    -40°C to +85°C G    -40°C to +105°C <sup>3</sup>	Code    Voltage M    +1.8Vdc <sup>4</sup> 2    +2.5Vdc 3    +3.3Vdc	Code    Packing T    1k pcs./reel
	Code    Output P    LVPECL - Pin 1 Enable L    LVDS - Pin 1 Enable E    LVPECL - Pin 2 Enable V    LVDS - Pin 2 Enable	Code    Stability    Code    Stability 6    ±20ppm <sup>2</sup> 4    ±30ppm 5    ±25ppm        3    ±50ppm	Code    Stability    Code    Stability 2    ±100ppm			

#### Notes:

- 1] Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2] Check factory for availability. Temperature codes A and C only.
- 3] Check factory for availability. Stability codes 2 and 3 only.
- 4] LVDS output only. Consult factory for availability.

**Not all performance combinations and frequencies may be available.  
Contact your local CTS Representative or CTS Customer Service for availability.**

This product is specified for use only in standard commercial applications. Supplier disclaims all express and implied warranties and liability in connection with any use of this product in any non-commercial applications or in any application that may expose the product to conditions that are outside of the tolerances provided in its specification.



## Electrical Specifications

### Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	$V_{CC}$	-	-0.5	-	5.0	V
Supply Voltage [Note 1]	$V_{CC}$	±5%	1.710 2.375 3.135	1.8 2.5 3.3	1.890 2.625 3.465	V
<b>Supply Current</b>						
LVPECL	$I_{CC}$	$V_{CC} = +2.5V$ or $+3.3V$ @ Maximum Load	-	55	88	mA
LVDS			-	45	66	
LVDS			-	7	20	
Operating Temperature	$T_A$	-	-20 -40 -40	+25	+70 +85 +105	°C
Storage Temperature	$T_{STG}$	-	-40	-	+125	°C

### Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Frequency Range</b>						
LVPECL	$f_0$	$V_{CC} = +2.5V$ or $+3.3V$		10 - 320		MHz
LVDS				10 - 320		
LVDS			$V_{CC} = +1.8V$	20 - 220		
Frequency Stability [Note 2]	$\Delta f/f_0$	-		20, 25, 30, 50 or 100		±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal $V_{CC}$	-3	-	3	ppm

1.] LVDS output only for +1.8V option.

2.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

### Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	$R_L$	Terminated to $V_{CC} - 2.0V$	-	50	-	Ohms
Output Voltage Levels	$V_{OH}$	PECL Load, -20°C to +70°C	$V_{CC} - 1.025$	-	$V_{CC} - 0.880$	V
	$V_{OL}$		$V_{CC} - 1.810$	-	$V_{CC} - 1.620$	
	$V_{OH}$	PECL Load, -40°C to +85°C	$V_{CC} - 1.085$	-	$V_{CC} - 0.880$	V
	$V_{OL}$		$V_{CC} - 1.830$	-	$V_{CC} - 1.555$	
Output Duty Cycle	SYM	@ $V_{CC} - 1.3V$	45	-	55	%
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels, $R_L = 50$ Ohms	-	0.3	0.7	ns
<b>LVDS</b>						
Output Type	-	-		LVDS		-
Output Load	$R_L$	Between Outputs	-	100	-	Ohms
Output Voltage Levels	$V_{OH}$	LVDS Load	-	1.43	1.60	V
	$V_{OL}$		0.90	1.10	-	
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	$V_{OD}$	$R_L = 100$ Ohms	247	330	454	mV
Offset Voltage	$V_{OS}$	LVDS Load	1.125	1.25	1.375	V
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels, $R_L = 100$ Ohms	-	0.4	0.7	ns

## Electrical Specifications

### Output Parameters

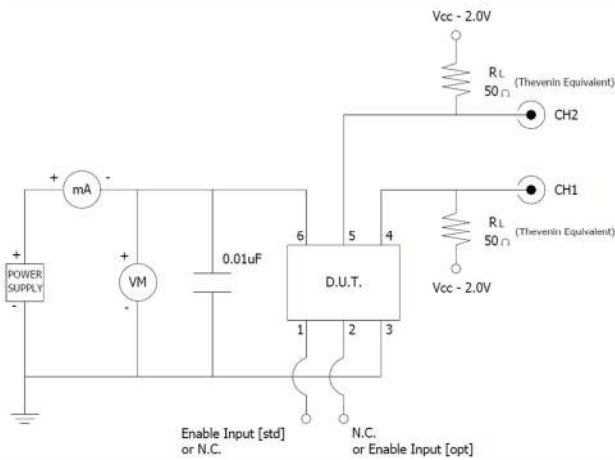
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	$T_S$	Application of $V_{CC}$	-	2	5	ms
<b>Enable Function [Standby]</b>						
Enable Input Voltage	$V_{IH}$	Pin 1 or 2 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	$V_{IL}$	Pin 1 or 2 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V
Disable Time	$T_{PLZ}$	Pin 1 or 2 Logic '0', Output Disabled	-	-	200	ns
Enable Time	$T_{PLZ}$	Pin 1 or 2 Logic '1', Output Enabled	-	-	2	ms
Phase Jitter, RMS	$t_{jrms}$	40MHz - 320MHz, Bandwidth 12kHz to 20MHz	-	300	500	fs
		10MHz - 39.999MHz, Bandwidth 12kHz to 5MHz	-	500	<1	ps

### Enable Truth Table

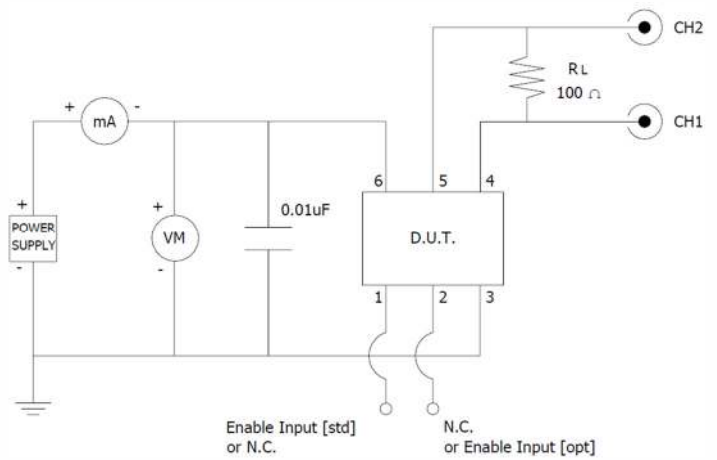
Pin 1 or Pin 2	Pin 4 & Pin 5
Logic '1'	Output Enabled
Open	Output Enabled
Logic '0'	Output Disabled, High Impedance

### Test Circuit

LVPECL

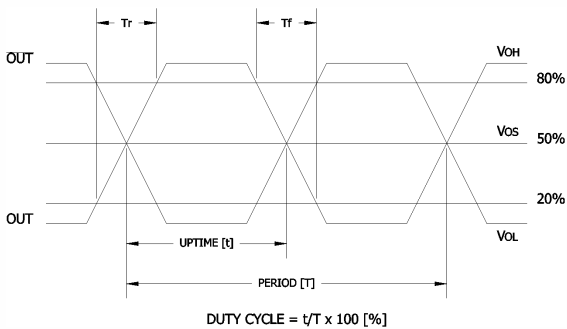


LVDS



### Output Waveform

LVPECL or LVDS

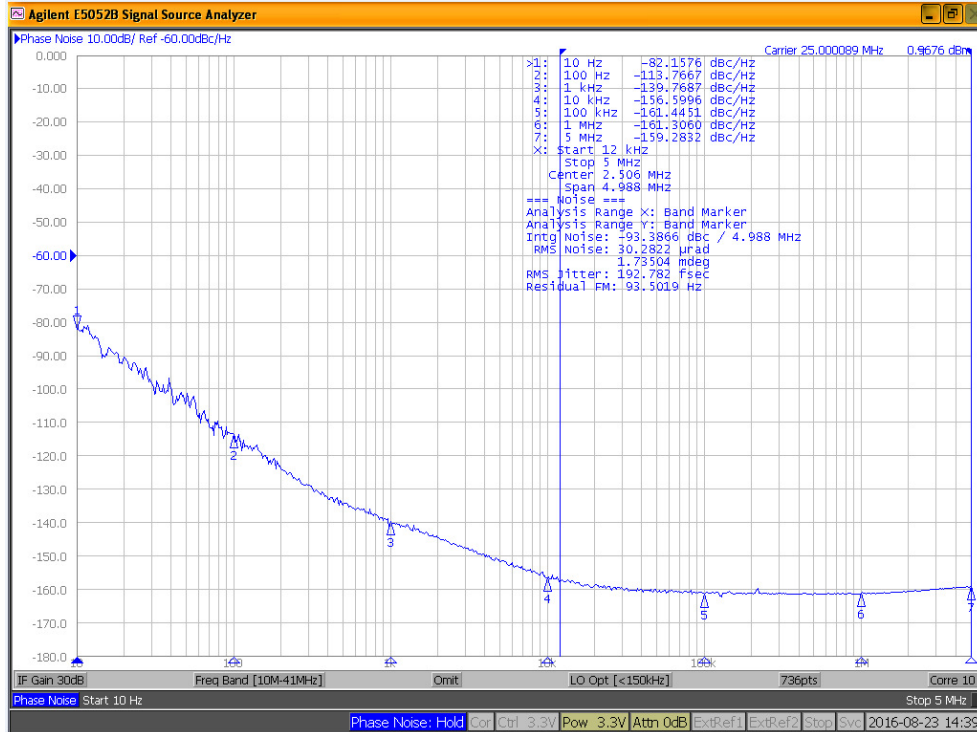


## Electrical Specifications

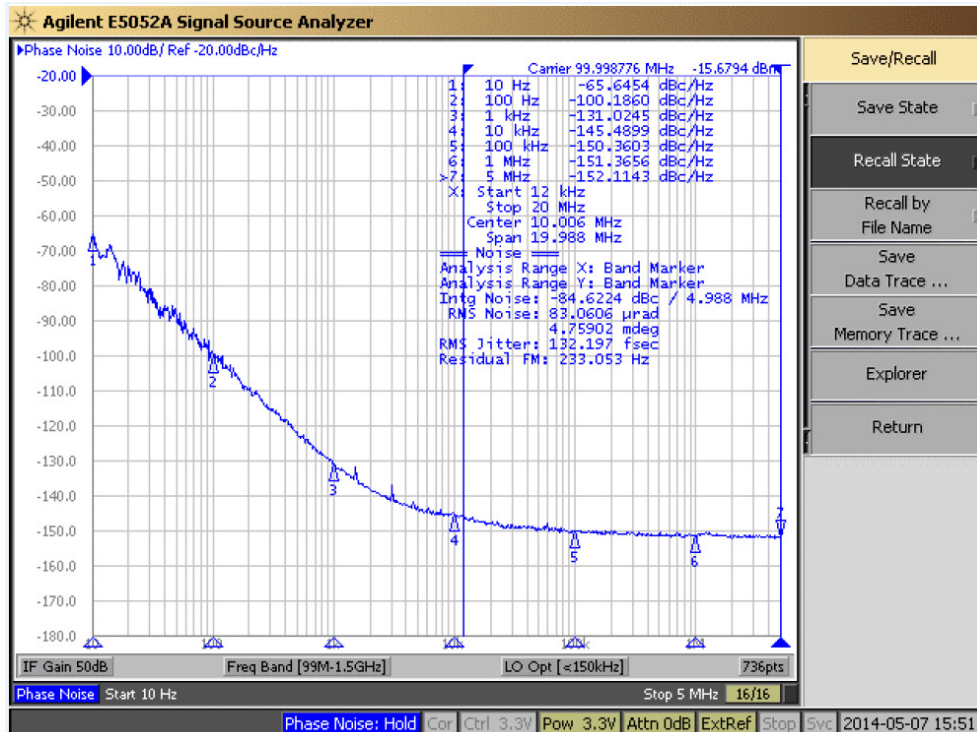
### Performance Data

#### Phase Noise [typical]

25MHz, LVPECL,  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$



100MHz, LVPECL,  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$

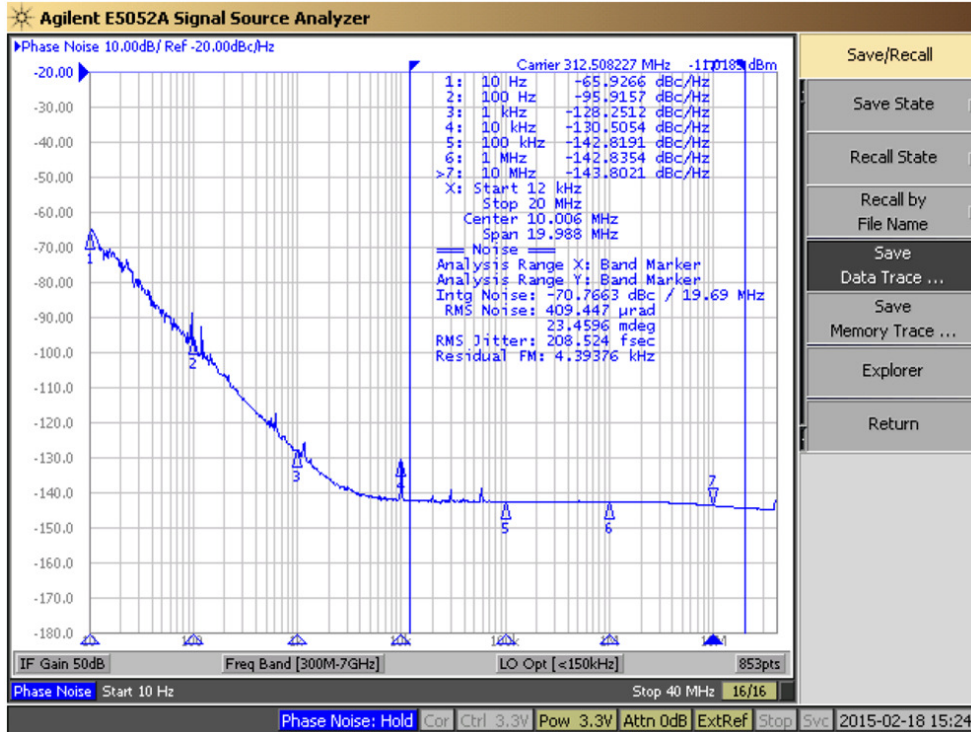


## Electrical Specifications

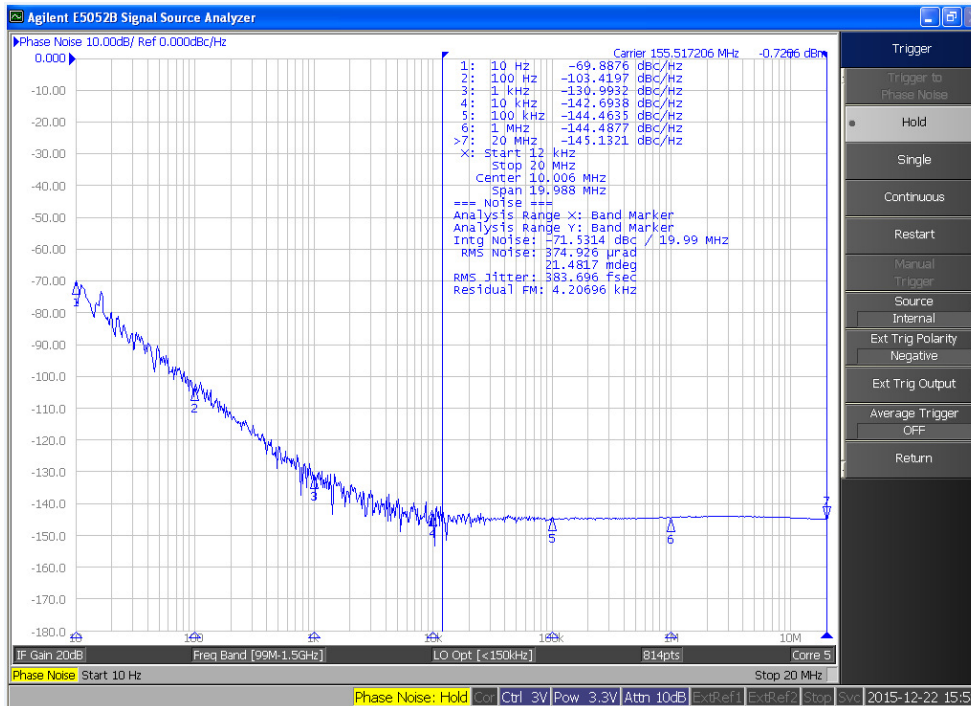
### Performance Data

#### Phase Noise [typical]

312.50MHz, LVPECL,  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$



155.52MHz, LVDS,  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$

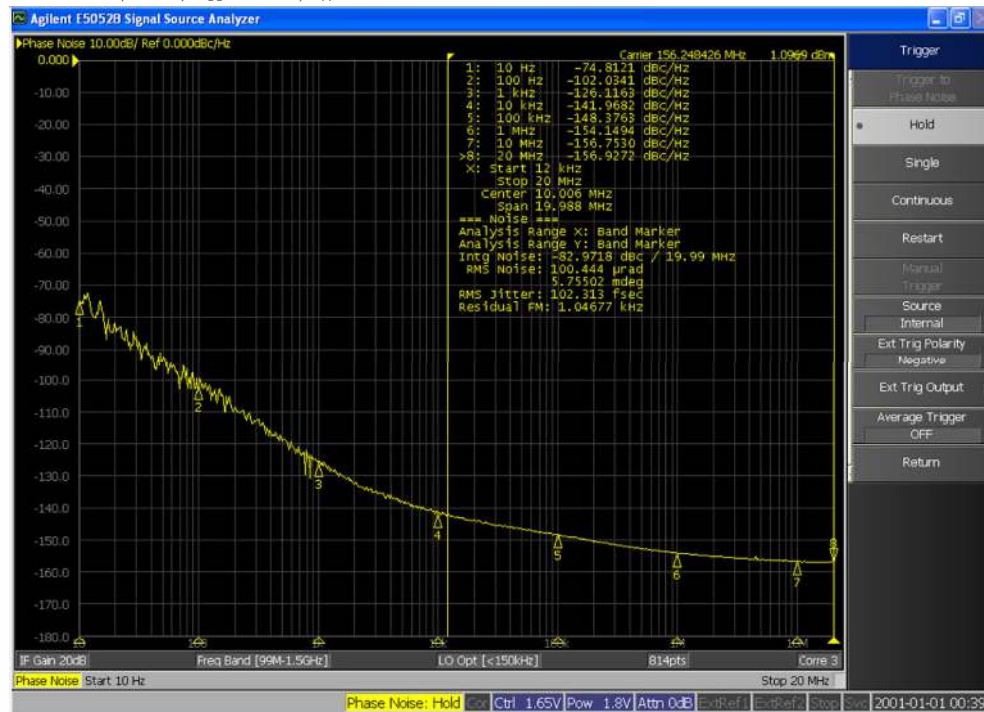


### Electrical Specifications

#### Performance Data

##### Phase Noise [typical]

156.25MHz, LVDS,  $V_{CC} = +1.8V$ ,  $T_A = +25^\circ C$



#### Phase Noise Tabulated

Typical,  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVPECL @ 25.00MHz</b>				
<b>Phase Noise</b>	-	Single Side Band		
		@ 10Hz	-82.16	dBc/Hz
		@ 100Hz	-113.77	
		@ 1kHz	-139.77	
		@ 10kHz	-156.60	
		@ 100kHz	-161.45	
		@ 1MHz	-161.31	
@ 5MHz	-159.28			
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 5MHz	192.78	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVPECL @ 100.00MHz</b>				
<b>Phase Noise</b>	-	Single Side Band		
		@ 10Hz	-65.65	dBc/Hz
		@ 100Hz	-100.19	
		@ 1kHz	-131.02	
		@ 10kHz	-145.49	
		@ 100kHz	-150.36	
		@ 1MHz	-151.37	
@ 5MHz	-152.11			
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	132.20	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVPECL @ 312.20MHz</b>				
<b>Phase Noise</b>	-	Single Side Band		
		@ 10Hz	-65.93	dBc/Hz
		@ 100Hz	-95.92	
		@ 1kHz	-128.25	
		@ 10kHz	-130.51	
		@ 100kHz	-142.82	
		@ 1MHz	-142.84	
@ 10MHz	-143.80			
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	208.52	fs



## Electrical Specifications

### Performance Data

#### Phase Noise Tabulated

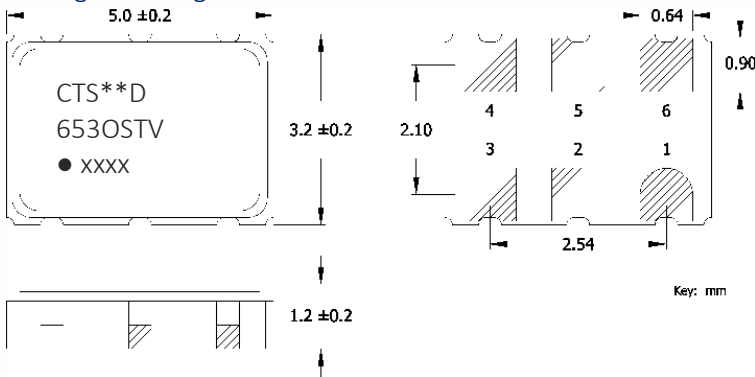
Typical,  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$  Typical,  $V_{CC} = +1.8V$ ,  $T_A = +25^\circ C$

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVDS @ 155.52MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-69.89	
		@ 100Hz	-103.42	
		@ 1kHz	-130.99	
		@ 10kHz	-142.69	dBc/Hz
		@ 100kHz	-144.46	
		@ 1MHz	-144.49	
		@ 20MHz	-145.13	
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	383.70	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVDS @ 156.25MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-74.81	
		@ 100Hz	-102.03	
		@ 1kHz	-126.12	
		@ 10kHz	-141.97	dBc/Hz
		@ 100kHz	-148.38	
		@ 1MHz	-154.15	
		@ 20MHz	-156.93	
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	102.31	fs

## Mechanical Specifications

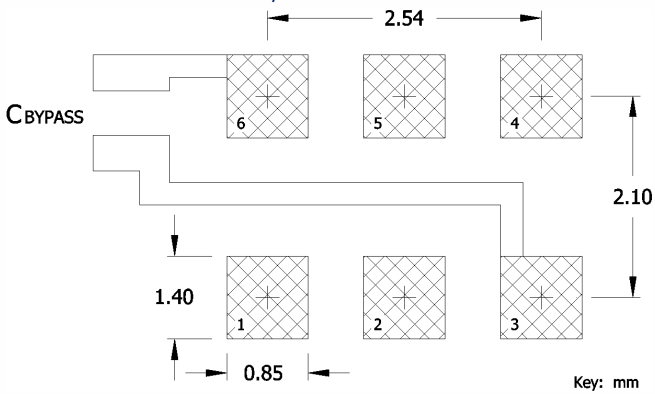
### Package Drawing



### Marking Information

- \*\* - Manufacturing Site Code.
- D - Date Code. See Table I for codes.
- O - Output Type; P or E = LVPECL, L or V = LVDS.  
[Refer to Ordering Information]
- ST - Frequency Stability/Temperature Code.  
[Refer to Ordering Information]
- V - Voltage Code; 3 = 3.3V, 2 = 2.5V, M = 1.8V.
- xxxx - Frequency Code.  
3-digits, frequencies below 100MHz  
4-digits, frequencies 100MHz or greater  
[See document 016-1454-0, Frequency Code Tables.]

### Recommended Pad Layout



### Notes

- JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020;  $+260^{\circ}\text{C}$  maximum, 20 seconds.
- MSL = 1.

### Pin Assignments

Pin	Symbol	Function
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	$V_{CC}$	Supply Voltage

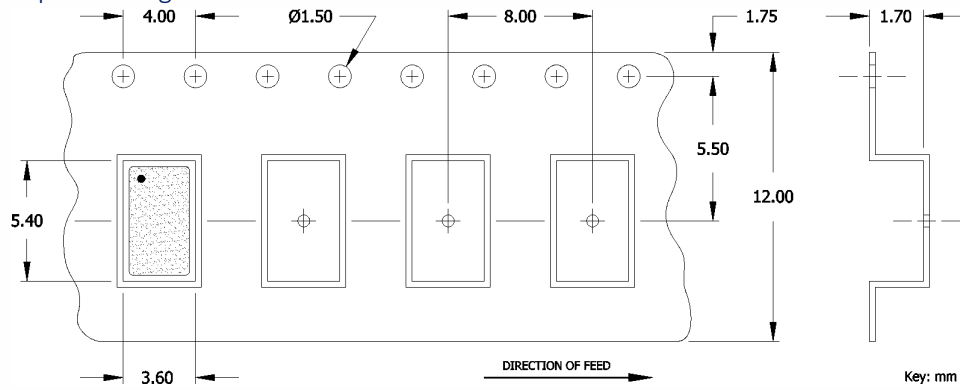
Table I - Date Code, Beginning year 2021

		MONTH														
		JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC			
YEAR																
2021	2025	2029	2033	2037	A	B	C	D	E	F	G	H	J	K	L	M
2022	2026	2030	2034	2038	N	P	Q	R	S	T	U	V	W	X	Y	Z
2023	2027	2031	2035	2039	a	b	c	d	e	f	g	h	j	k	l	m
2024	2028	2032	2036	2040	n	p	q	r	s	t	u	v	w	x	y	z

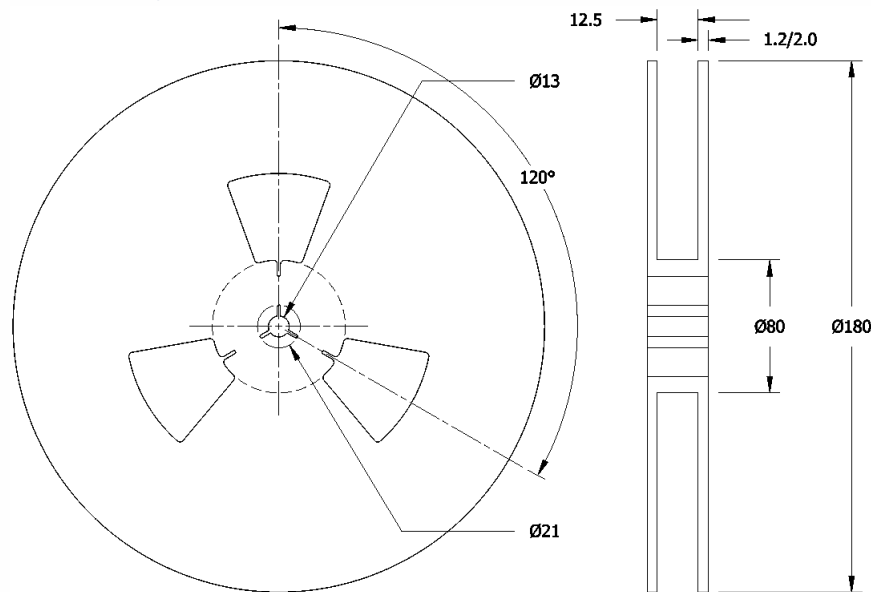


### Packaging - Tape and Reel

Tape Drawing



Reel Drawing



### Notes

1. Device quantity is 3k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.



## Addendum

### Common Frequencies Available – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
10.000000	100	80.000000	800	156.250000	1562	200.000000	2000
19.440000	194	100.000000	1000	156.253906	156A	212.500000	2125
25.000000	250	120.000000	1200	161.132800	1611	225.000000	2250
27.000000	270	125.000000	1250	167.372800	167A	250.000000	2500
40.000000	400	133.000000	1330	173.370800	1733	312.500000	3125
44.736000	447	148.351600	148A	175.000000	1750		
50.000000	500	148.500000	1485	178.500000	1785		
74.175800	74A	150.000000	1500	180.000000	1800		
74.250000	742	153.600000	1536	184.320000	1843		
80.000000	800	155.520000	1555	187.500000	1875		