December 10, 2015 FN9072.9

# Synchronous Rectified Buck MOSFET Drivers

The HIP6601B, HIP6603B and HIP6604B are high-frequency, dual MOSFET drivers specifically designed to drive two power N-Channel MOSFETs in a synchronous rectified buck converter topology. These drivers combined with a HIP63xx or the ISL65xx series of Multi-Phase Buck PWM controllers and MOSFETs form a complete core-voltage regulator solution for advanced microprocessors.

The HIP6601B drives the lower gate in a synchronous rectifier to 12V, while the upper gate can be independently driven over a range from 5V to 12V. The HIP6603B drives both upper and lower gates over a range of 5V to 12V. This drive-voltage flexibility provides the advantage of optimizing applications involving trade-offs between switching losses and conduction losses. The HIP6604B can be configured as either a HIP6601B or a HIP6603B.

The output drivers in the HIP6601B, HIP6603B and HIP6604B have the capacity to efficiently switch power MOSFETs at frequencies up to 2MHz. Each driver is capable of driving a 3000pF load with a 30ns propagation delay and 50ns transition time. These products implement bootstrapping on the upper gate with only an external capacitor required. This reduces implementation complexity and allows the use of higher performance, cost effective, N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

## Features

- Drives Two N-Channel MOSFETs
- Adaptive Shoot-Through Protection
- Internal Bootstrap Device
- Supports High Switching Frequency
  - Fast Output Rise Time
  - Propagation Delay 30ns
- Small 8 Ld SOIC and EPSOIC and 16 Ld QFN Packages
- Dual Gate-Drive Voltages for Optimal Efficiency
- Three-State Input for Output Stage Shutdown
- Supply Undervoltage Protection
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN—Quad Flat No Leads—Product Outline.
  - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile.
- Pb-Free (RoHS Compliant)

## Applications

- Core Voltage Supplies for Intel Pentium® III, AMD® Athlon™ Microprocessors
- High Frequency Low Profile DC/DC Converters
- High Current Low Voltage DC/DC Converters

## Related Literature

- Technical Brief TB363, *Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)*

## Ordering Information

| PART NUMBER (Notes 1, 2) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|
| HIP6601BCBZ* | 6601 BCBZ | 0 to +85 | 8 Ld SOIC | M8.15 |
| HIP6601BCBZA* | 6601 BCBZ | 0 to +85 | 8 Ld SOIC | M8.15 |
| HIP6601BECBZ* **(No longer available or supported)** | 6601 BECBZ | 0 to +85 | 8 Ld EPSOIC | M8.15B |
| HIP6601BECBZA* **(No longer available or supported)** | 6601 BECBZ | 0 to +85 | 8 Ld EPSOIC | M8.15B |
| HIP6603BCBZ* | 6603 BCBZ | 0 to +85 | 8 Ld SOIC | M8.15 |
| HIP6603BECBZ* **(No longer available or supported)** | 6603 BECBZ | 0 to +85 | 8 Ld EPSOIC | M8.15B |
| HIP6604BCRZ* **(No longer available or supported)** | 66 04BCRZ | 0 to +85 | 16 Ld QFN | L16.4x4 |

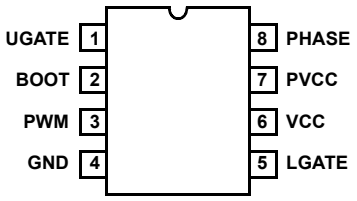
*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTES:

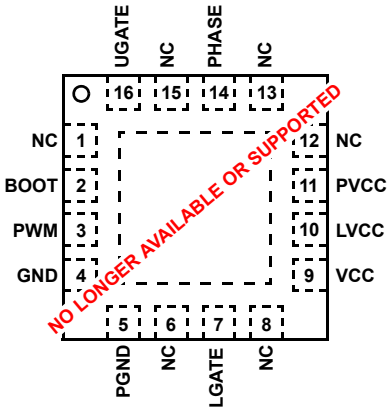
1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see device information page for HIP6601B, HIP6603B, HIP6604B. For more information on MSL, please see Technical Brief TB363.

## Pinouts

**HIP6601BCB, HIP6603BCB, HIP6601BECB, HIP6603BECB, (8 LD SOIC, EPSOIC)**
TOP VIEW

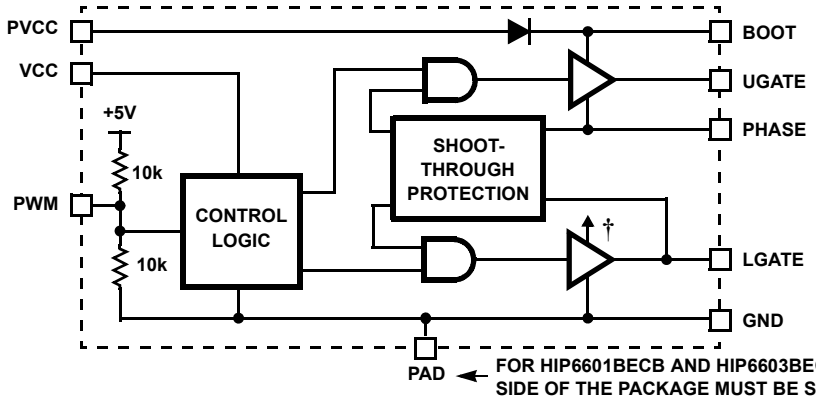



**HIP6604B (16 LD QFN)**
TOP VIEW



## Block Diagrams

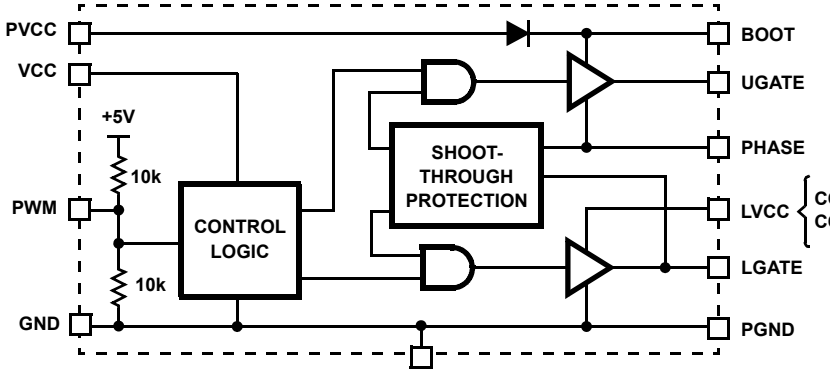
HIP6601B AND HIP6603B




† VCC FOR HIP6601B
PVCC FOR HIP6603B

FOR HIP6601BECB AND HIP6603BECB DEVICES, THE PAD ON THE BOTTOM SIDE OF THE PACKAGE MUST BE SOLDERED TO THE PC BOARD.

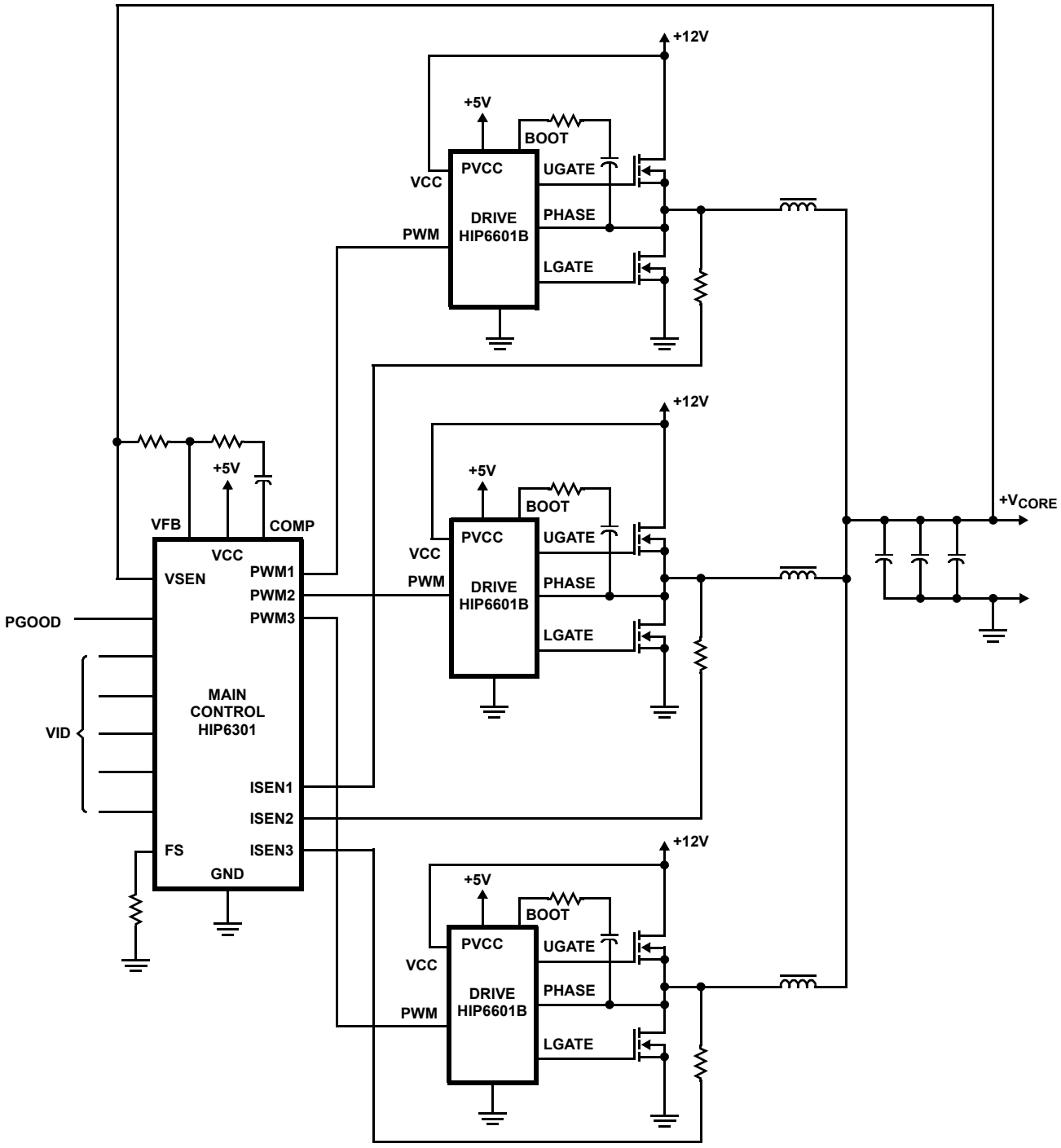
HIP6604B QFN PACKAGE




CONNECT LVCC TO VCC FOR HIP6601B CONFIGURATION
CONNECT LVCC TO PVCC FOR HIP6603B CONFIGURATION.

PAD ON THE BOTTOM SIDE OF THE PACKAGE MUST BE SOLDERED TO THE PC BOARD

## Typical Application: 3-Channel Converter Using HIP6301 and HIP6601B Gate Drivers



## Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . .15V
Supply Voltage (PVCC) . . . . . VCC + 0.3V
BOOT Voltage ($V_{BOOT}$ - $V_{PHASE}$) . . . . . .15V
Input Voltage ($V_{PWM}$) . . . . . .GND - 0.3V to 7V
UGATE. . . . . .$V_{PHASE}$ - 5V(<400ns pulse width) to $V_{BOOT}$ + 0.3V
. . . . . .$V_{PHASE}$ -0.3V(>400ns pulse width) to $V_{BOOT}$ + 0.3V
LGATE . . . . . GND - 5V(<400ns pulse width) to $V_{PVCC}$ + 0.3V
. . . . . GND -0.3V(>400ns pulse width) to $V_{PVCC}$ + 0.3V
PHASE. . . . . GND -5V(<400ns pulse width) to 15V
. . . . . .GND -0.3V(>400ns pulse width) to 15V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . . .3kV
Machine Model (Per EIAJ ED-4701 Method C-111). . . . . .200V

## Thermal Information

| Thermal Resistance | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| SOIC Package (Note 3) . . . . . | 97 | N/A |
| EPSOIC Package (Note 4). . . . . | 38 | N/A |
| QFN Package (Notes 4, 5). . . . . | 48 | 10 |

Maximum Junction Temperature (Plastic Package) . . . . . .150°C
Maximum Storage Temperature Range. . . . . .-65°C to 150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
For Recommended soldering conditions see Tech Brief TB389.

## Operating Conditions

Ambient Temperature Range. . . . . 0°C to 85°C
Maximum Operating Junction Temperature. . . . . 125°C
Supply Voltage, VCC . . . . . 12V ±10%
Supply Voltage Range, PVCC . . . . . 5V to 12V

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

3. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For $\theta_{JC}$, the “case temp” location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Boldface limits apply over the operating temperature range, 0°C to +85°C

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNITS |
|---|---|---|---|---|---|---|
| **VCC SUPPLY CURRENT** | | | | | | |
| Bias Supply Current | $I_{VCC}$ | HIP6601B, $f_{PWM}$ = 1MHz, $V_{PVCC}$ = 12V | - | 4.4 | **6.2** | mA |
| | | HIP6603B, $f_{PWM}$ = 1MHz, $V_{PVCC}$ = 12V | - | 2.5 | **3.6** | mA |
| Upper Gate Bias Current | $I_{PVCC}$ | HIP6601B, $f_{PWM}$ = 1MHz, $V_{PVCC}$ = 12V | - | 200 | **430** | µA |
| | | HIP6603B, $f_{PWM}$ = 1MHz, $V_{PVCC}$ = 12V | - | 1.8 | **3.3** | mA |
| **POWER-ON RESET** | | | | | | |
| VCC Rising Threshold | | | **9.7** | 9.95 | **10.4** | V |
| VCC Falling Threshold | | | **7.3** | 7.6 | **8.0** | V |
| **PWM INPUT** | | | | | | |
| Input Current | $I_{PWM}$ | $V_{PWM}$ = 0V or 5V (See “Block Diagrams” on page 3) | - | 500 | - | µA |
| PWM Rising Threshold | | | - | 3.6 | - | V |
| PWM Falling Threshold | | | - | 1.45 | - | V |
| UGATE Rise Time | $t_{RUGATE}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 20 | - | ns |
| LGATE Rise Time | $t_{RLGATE}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 50 | - | ns |
| UGATE Fall Time | $t_{FUGATE}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 20 | - | ns |
| LGATE Fall Time | $t_{FLGATE}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 20 | - | ns |
| UGATE Turn-Off Propagation Delay | $t_{PDLUGATE}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 30 | - | ns |
| LGATE Turn-Off Propagation Delay | $t_{PDLLGATE}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 20 | - | ns |
| Shutdown Window | | | **1.4** | - | **3.6** | V |
| Shutdown Holdoff Time | | | - | 230 | - | ns |

## Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Boldface limits apply over the operating temperature range, 0°C to +85°C

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNITS |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| Upper Drive Source Impedance | $R_{UGATE}$ | $V_{PVCC}$ = 5V | - | 1.7 | **3.0** | Ω |
| | | $V_{PVCC}$ = 12V | - | 3.0 | **5.0** | Ω |
| Upper Drive Sink Impedance | $R_{UGATE}$ | $V_{PVCC}$ = 5V | - | 2.3 | **4.0** | Ω |
| | | $V_{PVCC}$ = 12V | - | 1.1 | **2.0** | Ω |
| Lower Drive Source Current | $I_{LGATE}$ | $V_{PVCC}$ = 5V | **400** | 580 | - | mA |
| | | $V_{PVCC}$ = 12V | **500** | 730 | - | mA |
| Equivalent Drive Source Impedance | $R_{LGATE}$ | $V_{PVCC}$ = 5V | - | 9 | - | Ω |
| Lower Drive Sink Impedance | $R_{LGATE}$ | $V_{PVCC}$ = 5V or 12V | - | 1.6 | **4.0** | Ω |

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

## Functional Pin Description

### UGATE (Pin 1), (Pin 16 QFN)

Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.

### BOOT (Pin 2), (Pin 2 QFN)

Floating bootstrap supply pin for the upper gate drive. Connect a bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. A resistor in series with boot capacitor is required in certain applications to reduce ringing on the BOOT pin. See “Internal Bootstrap Device” on page 8 for guidance in choosing the appropriate capacitor and resistor values.

### PWM (Pin 3), (Pin 3 QFN)

The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the “Three-State PWM Input” on page 8 for further details. Connect this pin to the PWM output of the controller.

### GND (Pin 4), (Pin 4 QFN)

Bias and reference ground. All signals are referenced to this node.

### PGND (Pin 5 QFN Package Only)

This pin is the power ground return for the lower gate driver.

### LGATE (Pin 5), (Pin 7 QFN)

Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.

### VCC (Pin 6), (Pin 9 QFN)

Connect this pin to a +12V bias supply. Place a high quality bypass capacitor from this pin to GND.

### LVCC (Pin 10 QFN Package Only)

Lower gate driver supply voltage.

### PVCC (Pin 7), (Pin 11 QFN)

For the HIP6601B and the HIP6604B, this pin supplies the upper gate drive bias. Connect this pin from +12V down to +5V.

For the HIP6603B, this pin supplies both the upper and lower gate drive bias. Connect this pin to either +12V or +5V.

### PHASE (Pin 8), (Pin 14 QFN)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. The PHASE voltage is monitored for adaptive shoot-through protection. This pin also provides a return path for the upper gate drive.

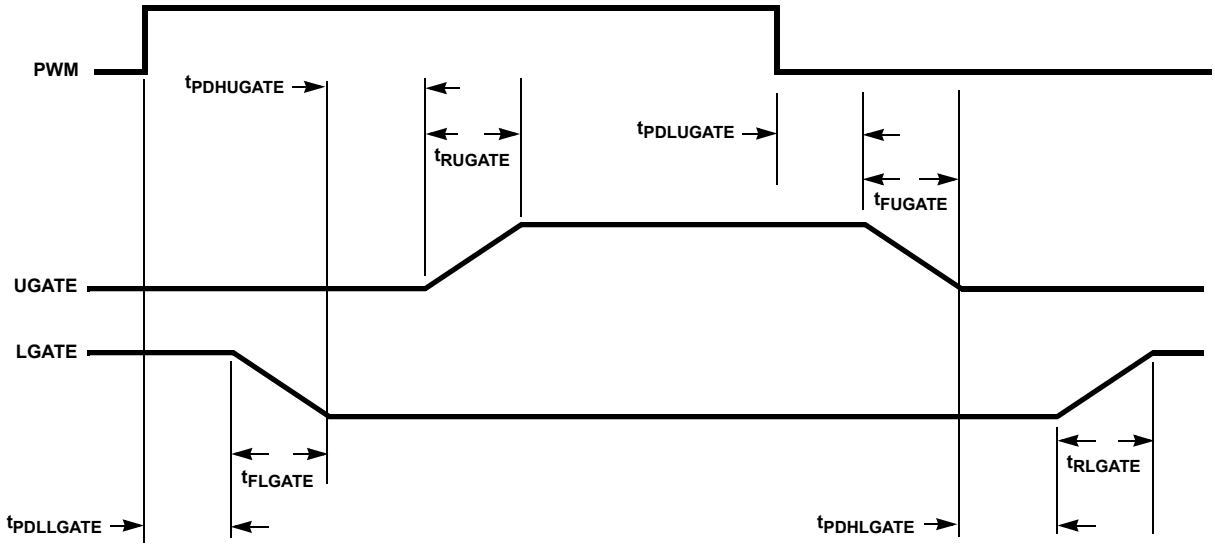
## Description

### Operation

Designed for versatility and speed, the HIP6601B, HIP6603B and HIP6604B dual MOSFET drivers control both high-side and low-side N-Channel FETs from one externally provided PWM signal.

The upper and lower gates are held low until the driver is initialized. Once the VCC voltage surpasses the VCC Rising Threshold (See “Electrical Specifications” on page 5), the PWM signal takes control of gate transitions. A rising edge on PWM initiates the turn-off of the lower MOSFET (see “Timing Diagram” on page 7). After a short propagation delay [$t_{PDLLGATE}$], the lower gate begins to fall. Typical fall times [$t_{FLGATE}$] are provided in the “Electrical Specifications” on page 5. Adaptive shoot-through circuitry monitors the LGATE voltage and determines the upper gate delay time [$t_{PDHUGATE}$] based on how quickly the LGATE voltage drops below 2.2V. This prevents both the lower and upper MOSFETs from conducting simultaneously or shoot-through. Once this delay period is complete the upper gate drive begins to rise [$t_{RUGATE}$] and the upper MOSFET turns on.

## Timing Diagram



A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [$t_{PDLUGATE}$] is encountered before the upper gate begins to fall [$t_{FUGATE}$]. Again, the adaptive shoot-through circuitry determines the lower gate delay time, $t_{PDHLGATE}$. The PHASE voltage is monitored and the lower gate is allowed to rise after PHASE drops below 0.5V. The lower gate then rises [$t_{RLGATE}$], turning on the lower MOSFET.

### Three-State PWM Input

A unique feature of the HIP660X drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the *Electrical Specifications* determine when the lower and upper gates are enabled.

### Adaptive Shoot-Through Protection

Both drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 2.2V threshold, at which time the UGATE is released to rise. Adaptive shoot-through circuitry monitors the PHASE voltage during UGATE turn-off. Once PHASE has dropped below a threshold of 0.5V, the LGATE is allowed to rise. PHASE continues to be monitored during the lower gate rise time. If PHASE has not dropped below 0.5V within 250ns, LGATE is taken high to keep the bootstrap capacitor charged. If the PHASE voltage exceeds the 0.5V threshold during this period and remains high for longer than 2μs, the LGATE transitions low. Both upper and lower gates are then held low until the next rising edge of the PWM signal.

### Power-On Reset (POR) Function

During initial start-up, the VCC voltage rise is monitored and gate drives are held low until a typical VCC rising threshold of 9.95V is reached. Once the rising VCC threshold is exceeded, the PWM input signal takes control of the gate drives. If VCC drops below a typical VCC falling threshold of 7.6V during operation, then both gate drives are again held low. This condition persists until the VCC voltage exceeds the VCC rising threshold.

### Internal Bootstrap Device

The HIP6601B, HIP6603B, and HIP6604B drivers all feature an internal bootstrap device. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

The bootstrap capacitor must have a maximum voltage rating above VCC + 5V. The bootstrap capacitor can be chosen from the following equation:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \quad \text{(EQ. 1)}$$

Where $Q_{GATE}$ is the amount of gate charge required to fully charge the gate of the upper MOSFET. The $\Delta V_{BOOT}$ term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose a HUF76139 is chosen as the upper MOSFET. The gate charge, $Q_{GATE}$, from the data sheet is 65nC for a 10V upper gate drive. We will assume a 200mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.325μF is required. The next larger standard value capacitance is 0.33μF.

In applications which require down conversion from +12V or higher and PVCC is connected to a +12V source, a boot resistor in series with the boot capacitor is required. The increased power density of these designs tend to lead to increased ringing on the BOOT and PHASE nodes, due to faster switching of larger currents across given circuit parasitic elements. The addition of the boot resistor allows for tuning of the circuit until the peak ringing on BOOT is below 29V from BOOT to GND and 17V from BOOT to VCC. A boot resistor value of 5Ω typically meets this criteria.

In some applications, a well tuned boot resistor reduces the ringing on the BOOT pin, but the PHASE to GND peak ringing exceeds 17V. A gate resistor placed in the UGATE trace between the controller and upper MOSFET gate is recommended to reduce the ringing on the PHASE node by slowing down the upper MOSFET turn-on. A gate resistor value between 2Ω to 10Ω typically reduces the PHASE to GND peak ringing below 17V.

### Gate Drive Voltage Versatility

The HIP6601B and HIP6603B provide the user total flexibility in choosing the gate drive voltage. The HIP6601B lower gate drive is fixed to VCC [+12V], but the upper drive rail can range from 12V down to 5V depending on what voltage is applied to PVCC. The HIP6603B ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC will set both driver rail voltages.

### Power Dissipation

Package power dissipation is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the SO8 package is approximately 800mW. When designing the driver into an application, it is recommended that the following calculation

be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the driver is approximated as:

$$P = 1.05f_{sw}\left(\frac{3}{2}V_U Q_U + V_L Q_L\right) + I_{DDQ}VCC \quad \text{(EQ. 2)}$$

where $f_{sw}$ is the switching frequency of the PWM signal. $V_U$ and $V_L$ represent the upper and lower gate rail voltage. $Q_U$ and $Q_L$ is the upper and lower gate charge determined by MOSFET selection and any external capacitance added to the gate pins. The $I_{DDQ}$ $V_{CC}$ product is the quiescent power of the driver and is typically 30mW.

The power dissipation approximation is a result of power transferred to and from the upper and lower gates. But, the internal bootstrap device also dissipates power on-chip during the refresh cycle. Expressing this power in terms of the upper MOSFET total gate charge is explained below.

The bootstrap device conducts when the lower MOSFET or its body diode conducts and pulls the PHASE node toward GND. While the bootstrap device conducts, a current path is formed that refreshes the bootstrap capacitor. Since the upper gate is driving a MOSFET, the charge removed from the bootstrap capacitor is equivalent to the total gate charge of the MOSFET. Therefore, the refresh power required by the bootstrap capacitor is equivalent to the power used to charge the gate capacitance of the MOSFET.

$$P_{REFRESH} = \frac{1}{2}f_{SW}Q_{LOSS}V_{PVCC} = \frac{1}{2}f_{SW}Q_U V_U \quad \text{(EQ. 3)}$$

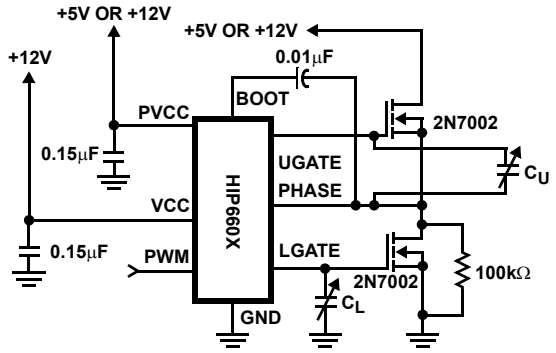
where $Q_{LOSS}$ is the total charge removed from the bootstrap capacitor and provided to the upper gate load.

The 1.05 factor is a correction factor derived from the following characterization. The base circuit for characterizing the drivers for different loading profiles and frequencies is provided. $C_U$ and $C_L$ are the upper and lower gate load capacitors. Decoupling capacitors [0.15µF] are added to the PVCC and VCC pins. The bootstrap capacitor value is 0.01µF.

In Figure 1, $C_U$ and $C_L$ values are the same and frequency is varied from 50kHz to 2MHz. PVCC and VCC are tied together to a +12V supply. Curves do exceed the 800mW cutoff, but continuous operation above this point is not recommended.

Figure 2 shows the dissipation in the driver with 3nF loading on both gates and each individually. Note the higher upper gate power dissipation which is due to the bootstrap device refresh cycle. Again PVCC and VCC are tied together and to a +12V supply.

## Test Circuit



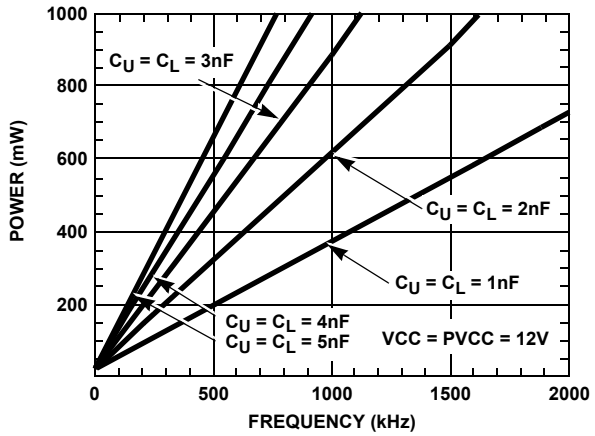




**FIGURE 1. POWER DISSIPATION vs FREQUENCY**

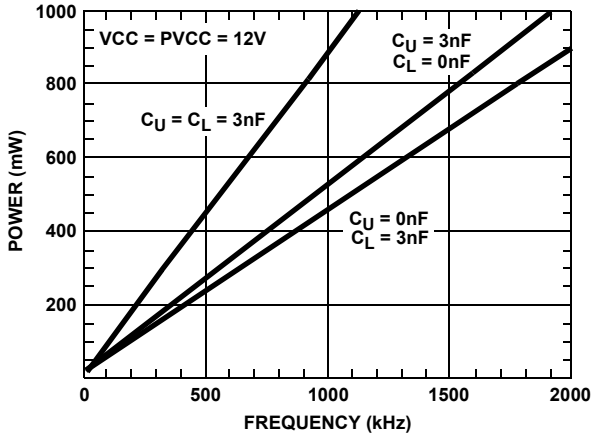



**FIGURE 2. 3nF LOADING PROFILE**

The impact of loading on power dissipation is shown in Figure 3. Frequency is held constant while the gate capacitors are varied from 1nF to 5nF. VCC and PVCC are tied together and to a +12V supply. Figures 4, 5 and 6 show the same characterization for the HIP6603B with a +5V supply on PVCC and VCC tied to a +12V supply.

Since both upper and lower gate capacitance can vary, Figure 8 shows dissipation curves versus lower gate capacitance with upper gate capacitance held constant at three different values. These curves apply only to the HIP6601B due to power supply configuration.

## Typical Performance Curves

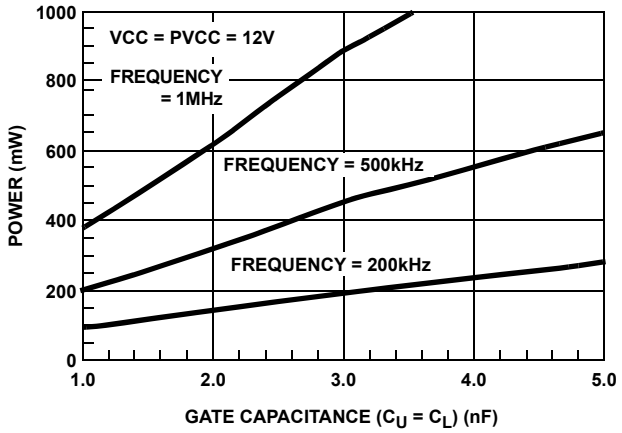



FIGURE 3. POWER DISSIPATION vs LOADING

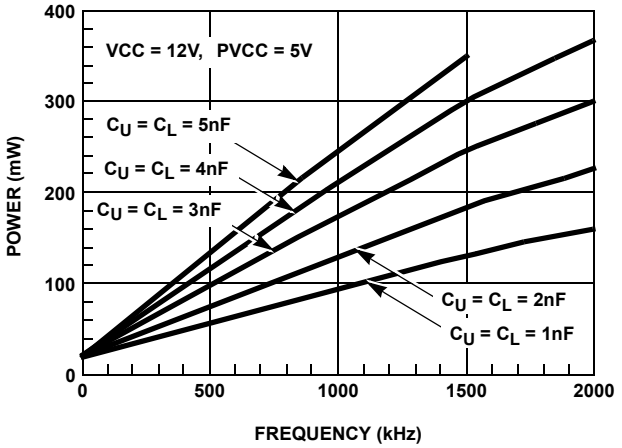



FIGURE 4. POWER DISSIPATION vs FREQUENCY (HIP6603B)

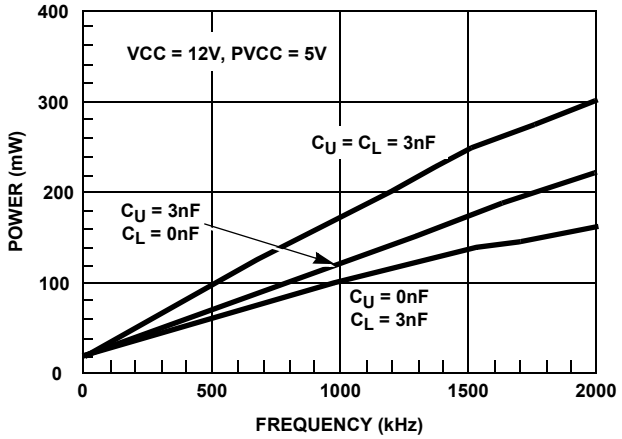



FIGURE 5. 3nF LOADING PROFILE (HIP6603B)

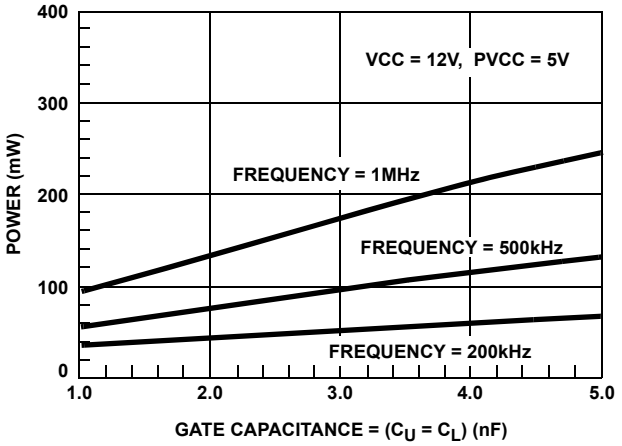



FIGURE 6. VARIABLE LOADING PROFILE (HIP6603B)

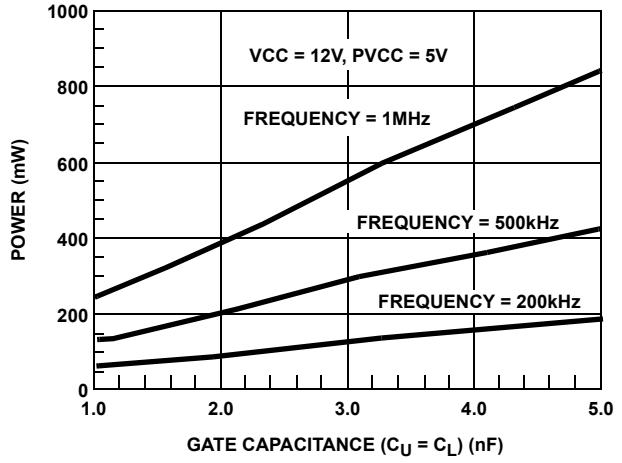



FIGURE 7. POWER DISSIPATION vs FREQUENCY (HIP6601B)

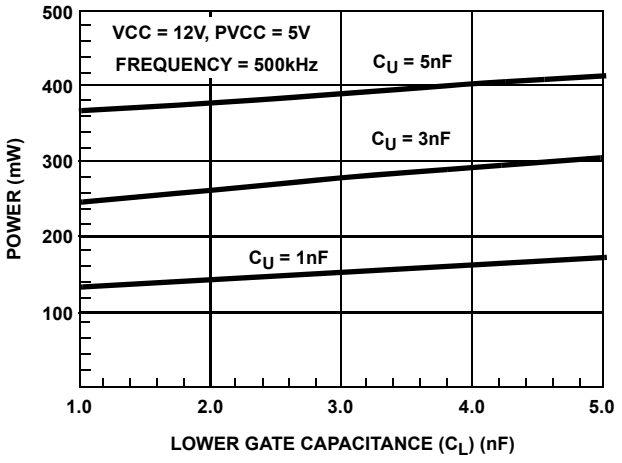



FIGURE 8. POWER DISSIPATION vs LOWER GATE CAPACITANCE FOR FIXED VALUES OF UPPER GATE CAPACITANCE

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| December 10, 2015 | FN9072.9 | - Updated Ordering Information Table on page 2.<br>- Added Revision History.<br>- Added About Intersil Verbiage.<br>- Updated POD M8.15 to latest revision changes are as follow:<br>Changed Note 1 "1982" to "1994"<br>Changed in Typical Recommended Land Pattern the following:<br>2.41(0.095) to 2.20(0.087)<br>0.76 (0.030) to 0.60(0.023)<br>0.200 to 5.20(0.205)<br>Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. |

## About Intersil

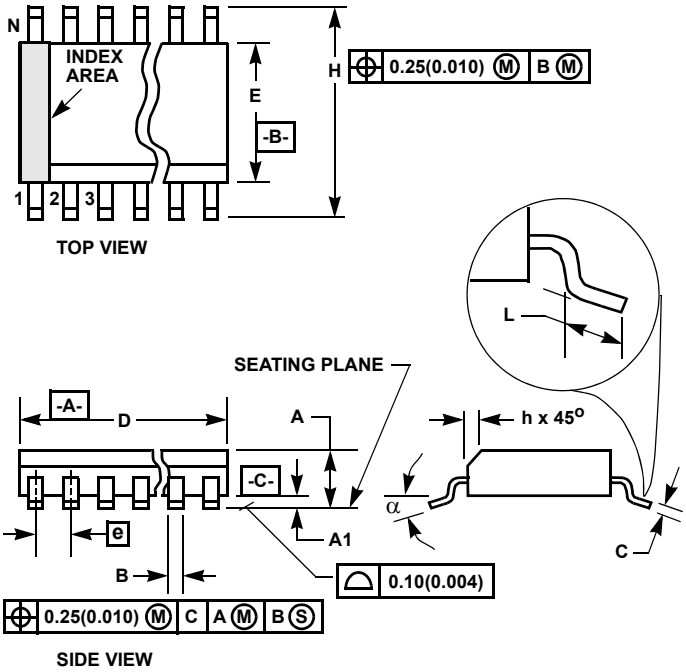
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

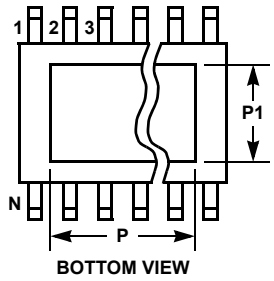
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

## Small Outline Exposed Pad Plastic Packages (EPSOIC)




### M8.15B

**8 LEAD NARROW BODY SMALL OUTLINE EXPOSED PAD PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.056 | 0.066 | 1.43 | 1.68 | - |
| A1 | 0.001 | 0.005 | 0.03 | 0.13 | - |
| B | 0.0138 | 0.0192 | 0.35 | 0.49 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.189 | 0.196 | 4.80 | 4.98 | 3 |
| E | 0.150 | 0.157 | 3.81 | 3.99 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.230 | 0.244 | 5.84 | 6.20 | - |
| h | 0.010 | 0.016 | 0.25 | 0.41 | 5 |
| L | 0.016 | 0.035 | 0.41 | 0.89 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |
| P | - | 0.094 | - | 2.387 | 11 |
| P1 | - | 0.094 | - | 2.387 | 11 |

Rev. 5 8/10

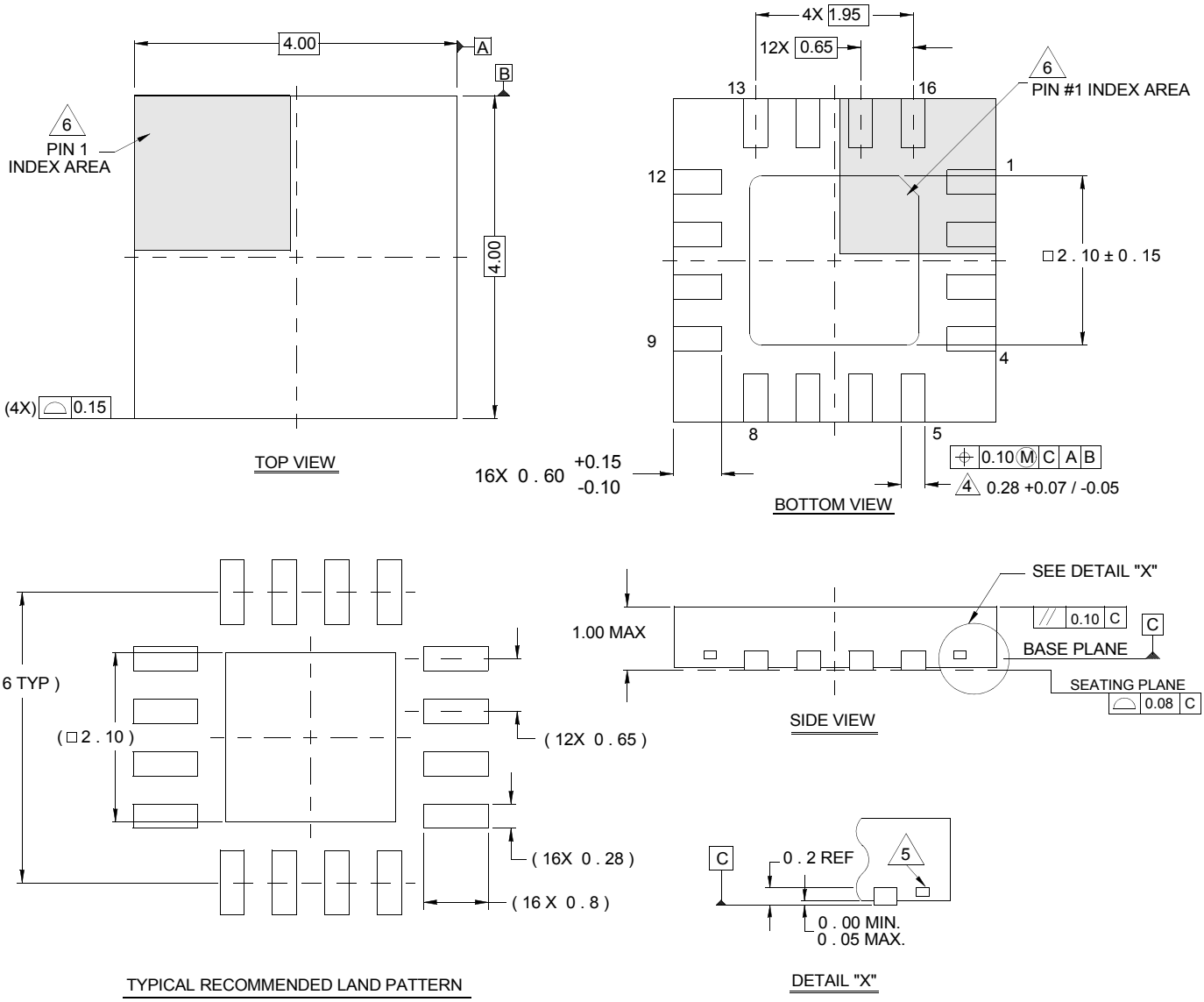
NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
11. Dimensions “P” and “P1” are thermal and/or electrical enhanced variations. Values shown are maximum size of exposed pad within lead count and body size.

# Package Outline Drawing

## L16.4x4

**16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 6, 02/08**




NOTES:

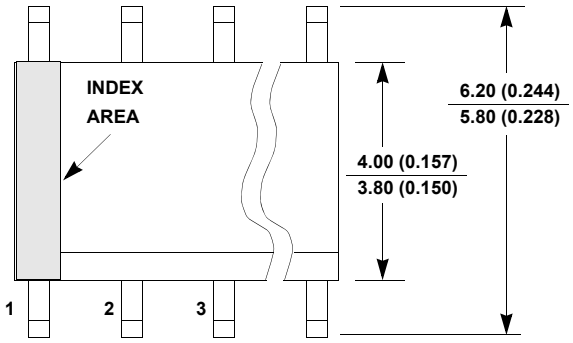
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

# Package Outline Drawing

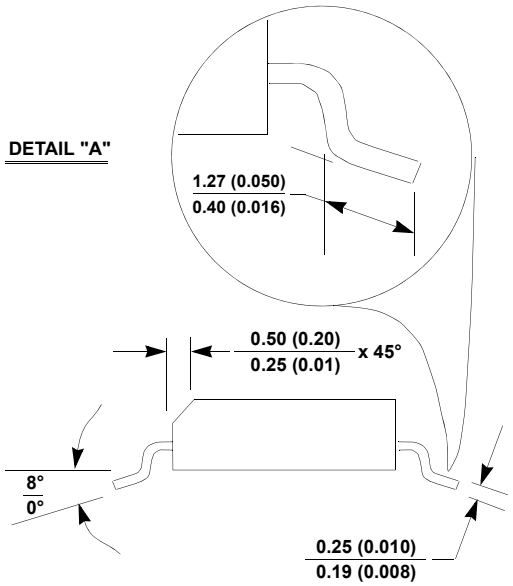
## M8.15

**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

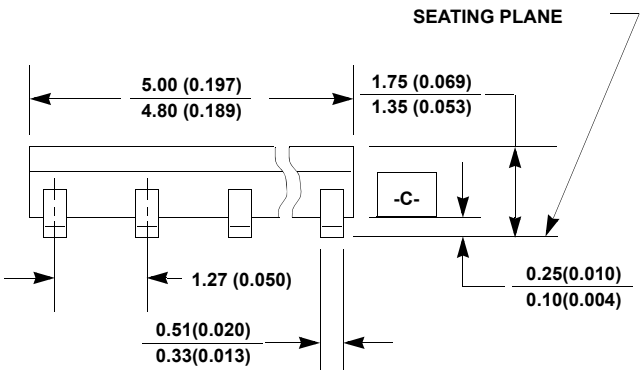
**Rev 4, 1/12**



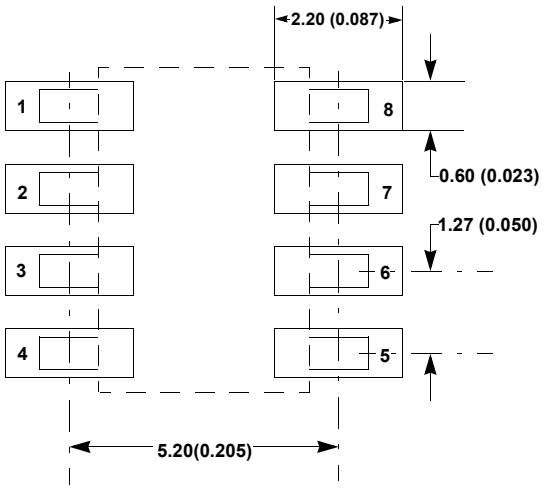

TOP VIEW




SIDE VIEW “B”




SIDE VIEW “A”




TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.