- **Low $r_{DS(on)}$ . . . 1 Ω Typ**
- **Output Short-Circuit Protection**
- **Avalanche Energy . . . 75 mJ**
- **Eight 350-mA DMOS Outputs**
- **50-V Switching Capability**
- **Four Distinct Function Modes**
- **Low Power Consumption**

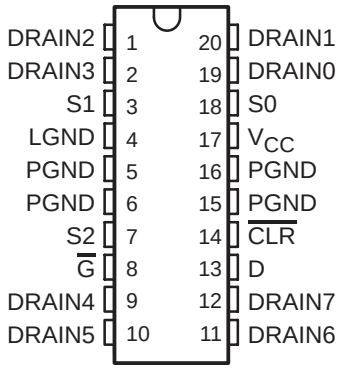
## description

This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of operating as eight addressable latches or an 8-line demultiplexer with active-low DMOS outputs. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

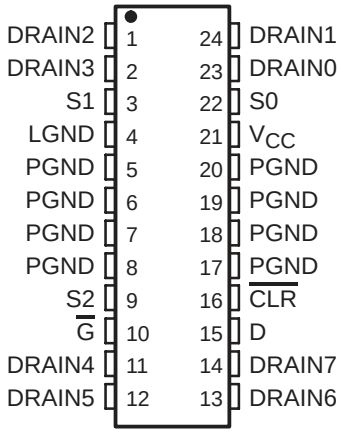
Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 8-line demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

**NE PACKAGE**
**(TOP VIEW)**




**DW PACKAGE**
**(TOP VIEW)**




**FUNCTION TABLE**

| INPUTS | | | OUTPUT OF ADDRESSED DRAIN | EACH OTHER DRAIN | FUNCTION |
|---|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{G}$ | D | | | |
| H | L | H | L | $Q_{io}$ | Addressable Latch |
| H | L | L | H | $Q_{io}$ | |
| H | H | X | $Q_{io}$ | $Q_{io}$ | Memory |
| L | L | H | L | H | 8-Line Demultiplexer |
| L | L | L | H | H | |
| L | H | X | H | H | Clear |

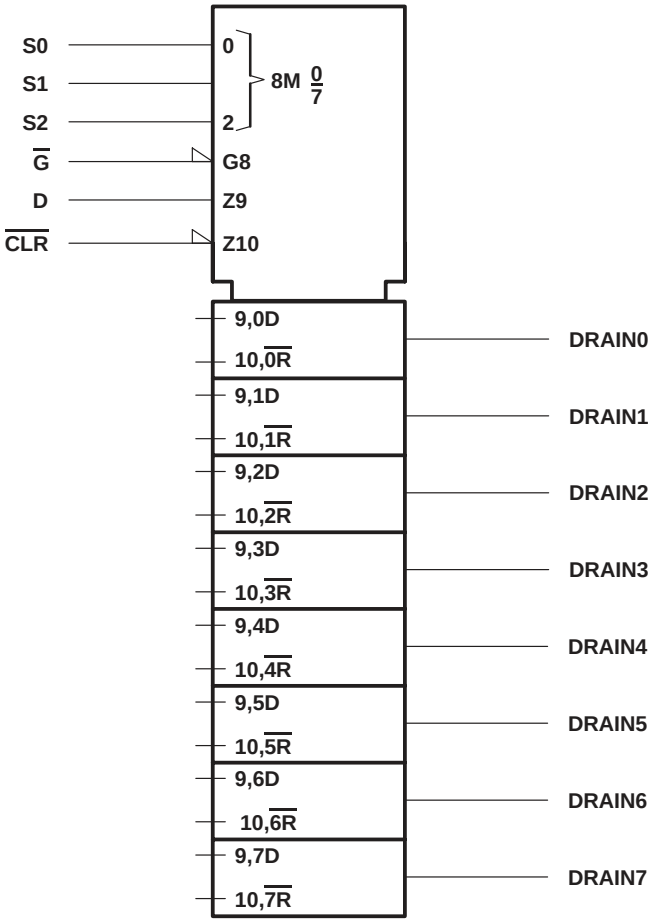
**LATCH SELECTION TABLE**

| SELECT INPUTS | | | DRAIN ADDRESSED |
|---|---|---|---|
| S2 | S1 | S0 | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

## description (continued)

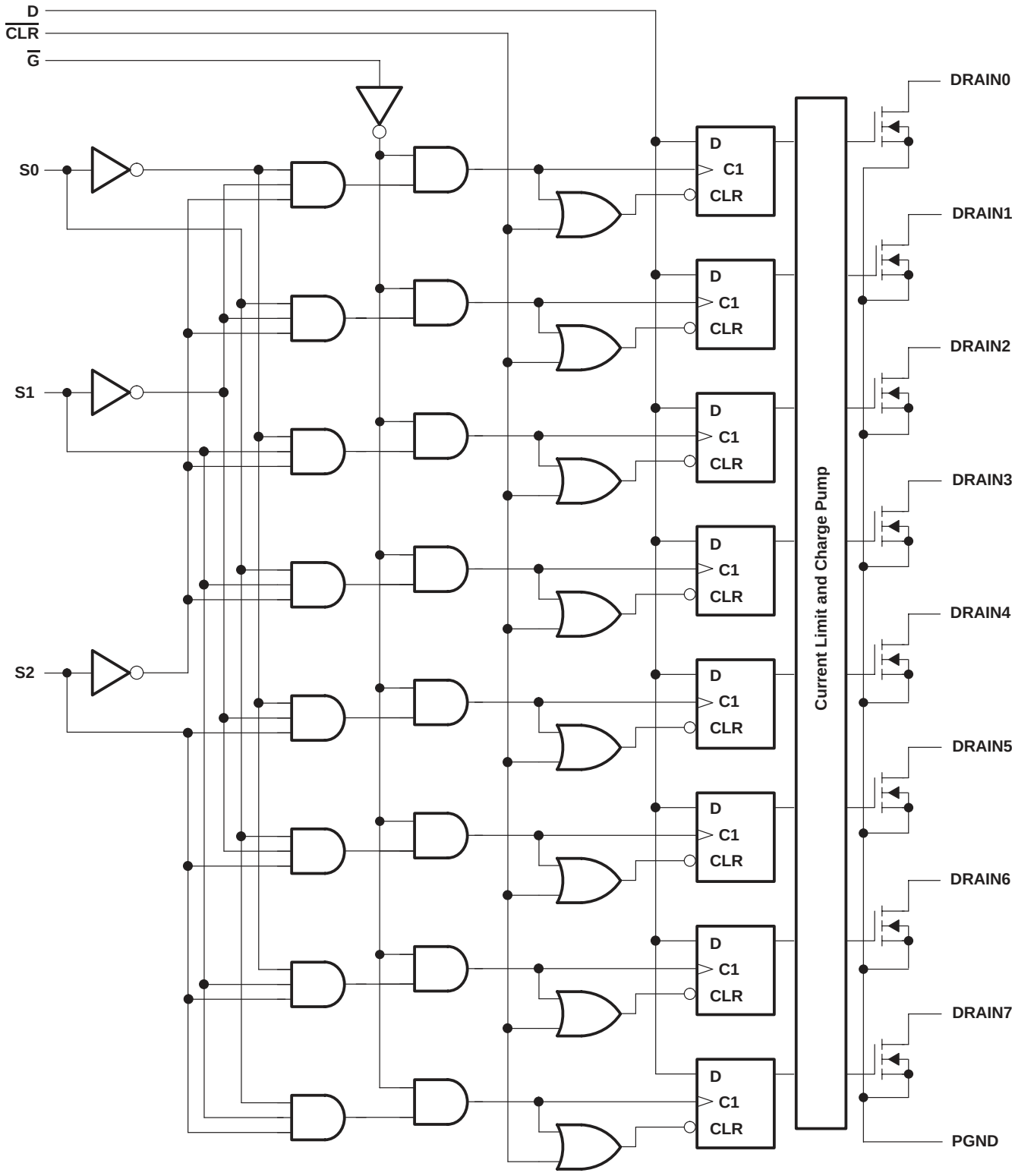
The TPIC6A259 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body, surface-mount (DW) package. The TPIC6A259 is characterized for operation over the operating case temperature range of −40°C to 125°C.

## logic symbol†

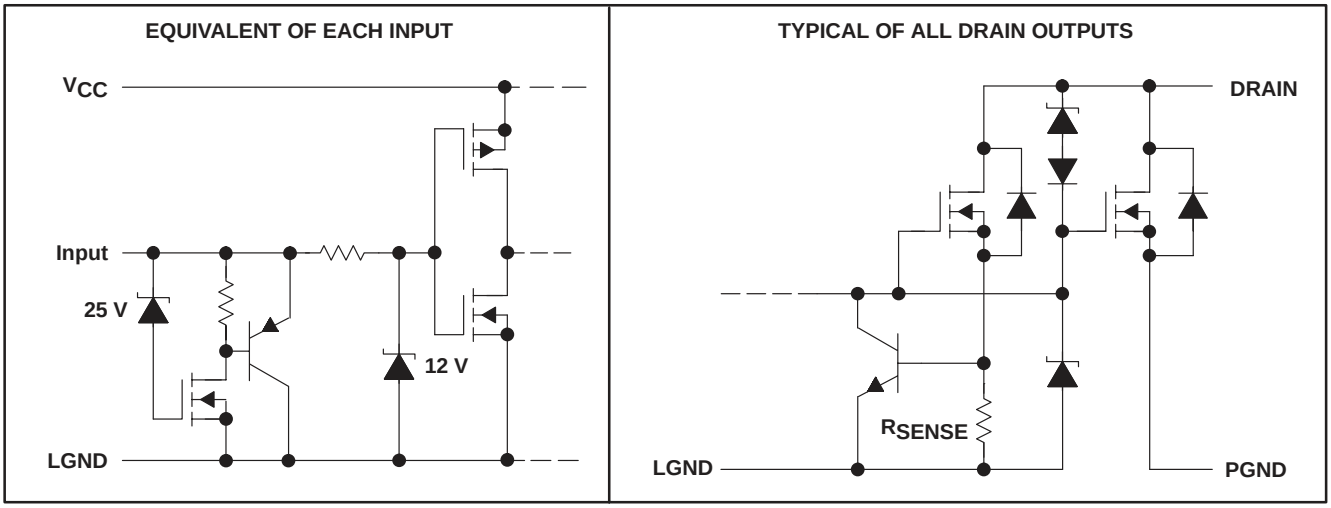



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## schematic of inputs and outputs




## absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

| | |
|---|---|
| Logic supply voltage, $V_{CC}$ (see Note 1) | 7 V |
| Logic input voltage range, $V_I$ | −0.3 V to 7 V |
| Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2) | 50 V |
| Continuous source-to-drain diode anode current | 1 A |
| Pulsed source-to-drain diode anode current (see Note 3) | 2 A |
| Pulsed drain current, each output, all outputs on, $I_D$, $T_C$ = 25°C (see Note 3) | 1.1 A |
| Continuous drain current, each output, all outputs on, $I_D$, $T_C$ = 25°C | 350 mA |
| Peak drain current single output, $T_C$ = 25°C (see Note 3) | 1.1 A |
| Single-pulse avalanche energy, $E_{AS}$ (see Figure 6) | 75 mJ |
| Avalanche current, $I_{AS}$ (see Note 4) | 600 mA |
| Continuous total dissipation | See Dissipation Rating Table |
| Operating virtual junction temperature range, $T_J$ | −40°C to 150°C |
| Operating case temperature range, $T_C$ | −40°C to 125°C |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature ($T_{JS}$) = 25°C, L = 210 mH, and $I_{AS}$ = 600 mA (see Figure 6).

**DISSIPATION RATING TABLE**

| PACKAGE | $T_C \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_C$ = 25°C | $T_C$ = 125°C POWER RATING |
|---|---|---|---|
| DW | 1750 mW | 14 mW/°C | 350 mW |
| NE | 2500 mW | 20 mW/°C | 500 mW |

## recommended operating conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Logic supply voltage, $V_{CC}$ | 4.5 | 5.5 | V |
| High-level input voltage, $V_{IH}$ | 0.85 $V_{CC}$ | $V_{CC}$ | V |
| Low-level input voltage, $V_{IL}$ | 0 | 0.15 $V_{CC}$ | V |
| Pulsed drain output current, $T_C$ = 25°C, $V_{CC}$ = 5 V (see Notes 3 and 5) | −1.8 | 0.6 | A |
| Setup time, D high before $\overline{G}\uparrow$, $t_{su}$ (see Figure 2) | 10 | | ns |
| Hold time, D high before $\overline{G}\uparrow$, $t_h$ (see Figure 2) | 5 | | ns |
| Pulse duration, $t_w$ (see Figure 2) | 15 | | ns |
| Operating case temperature, $T_C$ | −40 | 125 | °C |

## electrical characteristics, $V_{CC}$ = 5 V, $T_C$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{(BR)DSX}$ | Drain-to-source breakdown voltage | $I_D$ = 1 mA | | | 50 | | | V |
| $V_{SD}$ | Source-to-drain diode forward voltage | $I_F$ = 350 mA, | See Note 3 | | | 0.8 | 1.1 | V |
| $I_{IH}$ | High-level input current | $V_I = V_{CC}$ | | | | | 1 | µA |
| $I_{IL}$ | Low-level input current | $V_I$ = 0 | | | | | −1 | µA |
| $I_{CC}$ | Logic supply current | $I_O$ = 0, | $V_I = V_{CC}$ or 0 | | | 0.5 | 5 | mA |
| $I_{OK}$ | Output current at which chopping starts | $T_C$ = 25°C, | See Note 5 and Figures 3 and 4 | | 0.6 | 0.8 | 1.1 | A |
| $I_{(nom)}$ | Nominal current | $V_{DS(on)}$ = 0.5 V, $V_{CC}$ = 5 V, | $I_{(nom)} = I_D$, See Notes 5, 6, and 7 | $T_C$ = 85°C, | | 350 | | mA |
| $I_D$ | Off-state drain current | $V_{DS}$ = 40 V, | $T_C$ = 25°C | | | 0.1 | 1 | µA |
| | | $V_{DS}$ = 40 V, | $T_C$ = 125°C | | | 0.2 | 5 | |
| $r_{DS(on)}$ | Static drain-to-source on-state resistance | $I_D$ = 350 mA, | $T_C$ = 25°C | See Notes 5 and 6 and Figures 9 and 10 | | 1 | 1.5 | Ω |
| | | $I_D$ = 350 mA, | $T_C$ = 125°C | | | 1.7 | 2.5 | |

## switching characteristics, $V_{CC}$ = 5 V, $T_C$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation delay time, high- to low-level output from D | $C_L$ = 30 pF, | $I_D$ = 350 mA, See Figures 1, 2, and 11 | | 30 | | ns |
| $t_{PLH}$ | Propagation delay time, low- to high-level output from D | | | | 125 | | ns |
| $t_r$ | Rise time, drain output | | | | 60 | | ns |
| $t_f$ | Fall time, drain output | | | | 30 | | ns |
| $t_a$ | Reverse-recovery-current rise time | $I_F$ = 350 mA, | di/dt = 20 A/µs, See Notes 5 and 6 and Figure 5 | | 100 | | ns |
| $t_{rr}$ | Reverse-recovery time | | | | 300 | | ns |

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C$ = 85°C.

## thermal resistance

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal resistance, junction-to-case | DW | All eight outputs with equal power | | 10 | °C/W |
| | | NE | | | 10 | |
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient | DW | All eight outputs with equal power | | 50 | °C/W |
| | | NE | | | 50 | |

## PARAMETER MEASUREMENT INFORMATION

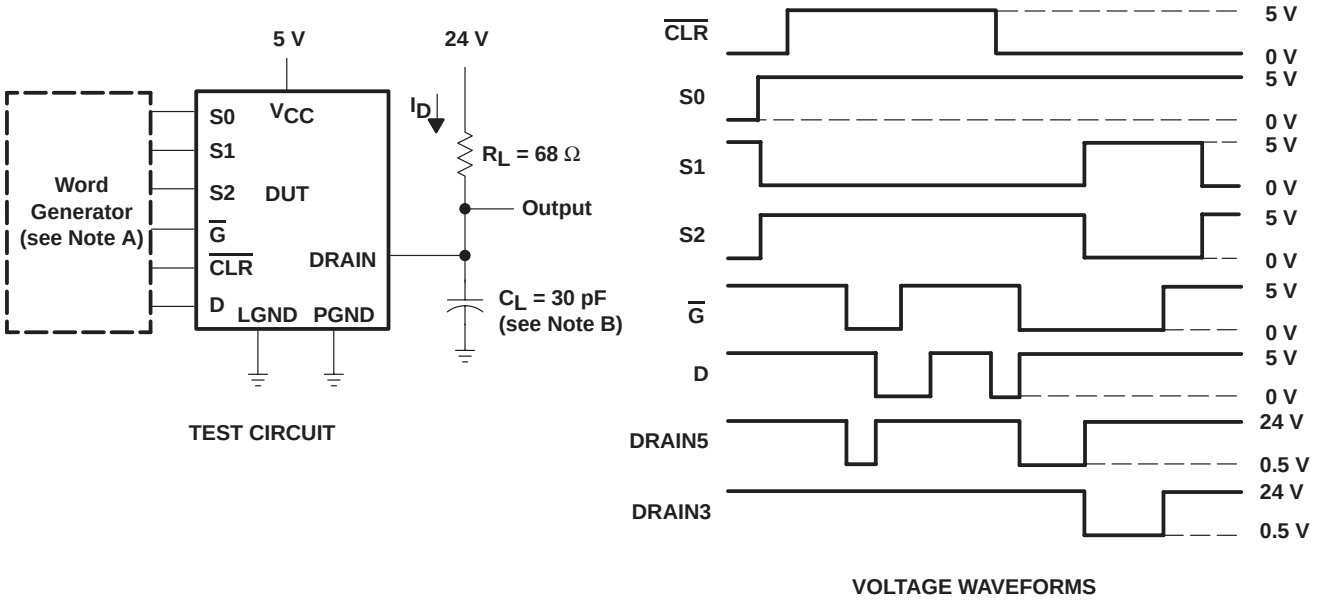



**Figure 1. Typical Operation Mode**

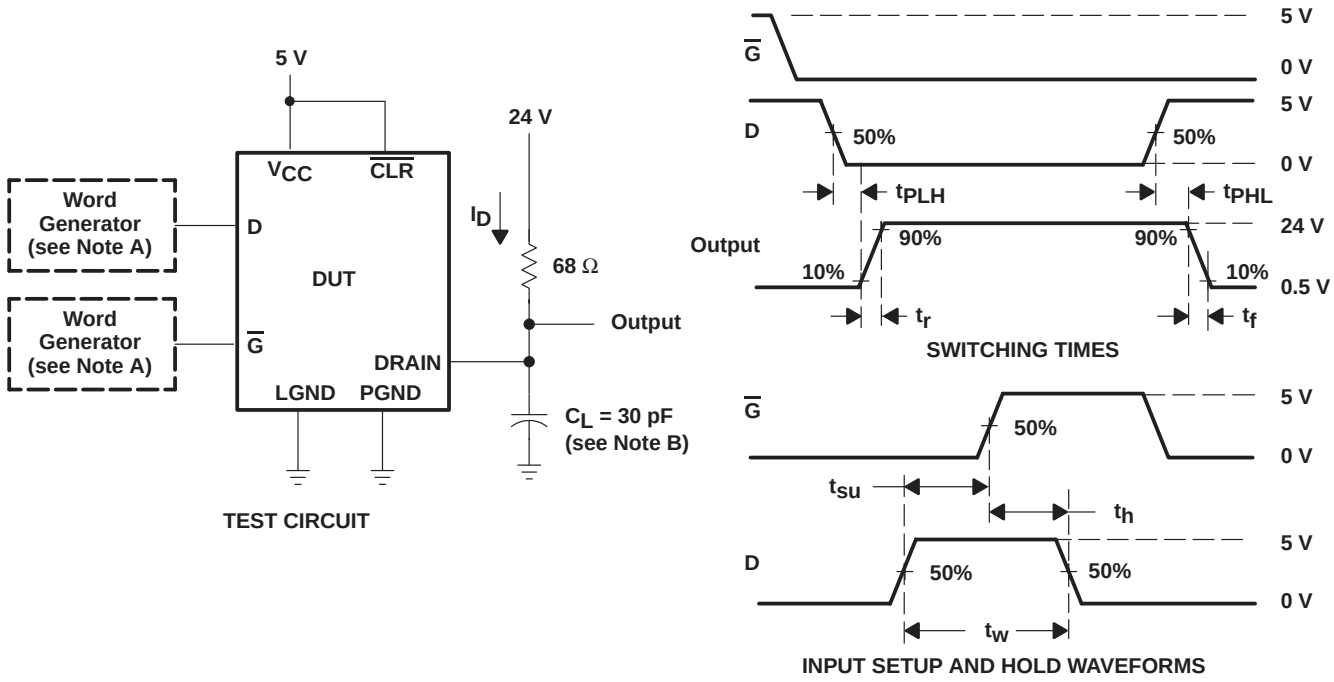


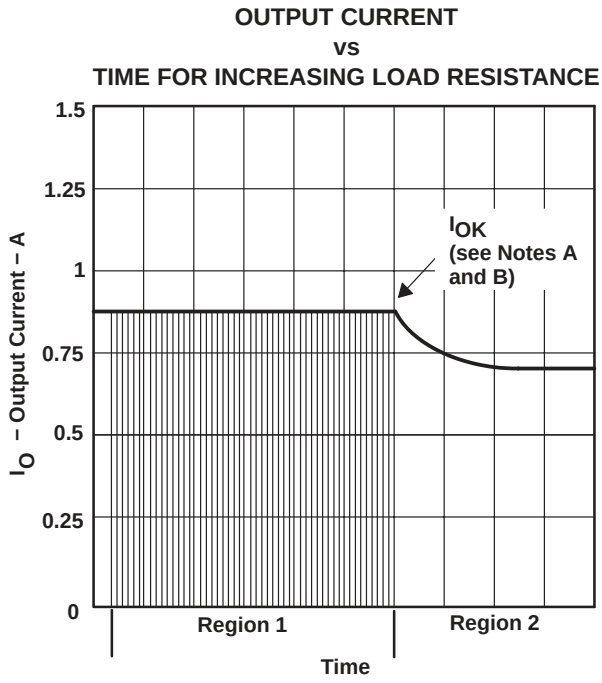

**Figure 2. Test Circuit, Switching Times, and Voltage Waveforms**

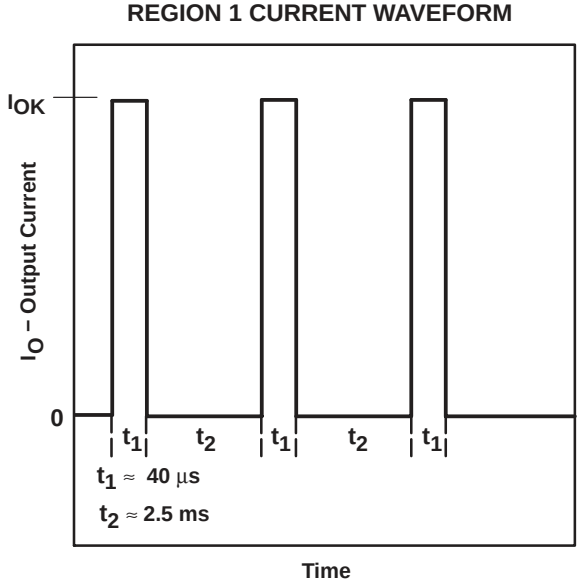
NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

## PARAMETER MEASUREMENT INFORMATION




First output current pulses after turn-on in chopping mode with resistive load.

NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to $I_{OK}$. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.

B. Region 1 duty cycle is approximately 2%.

**Figure 3. Chopping-Mode Characteristics**

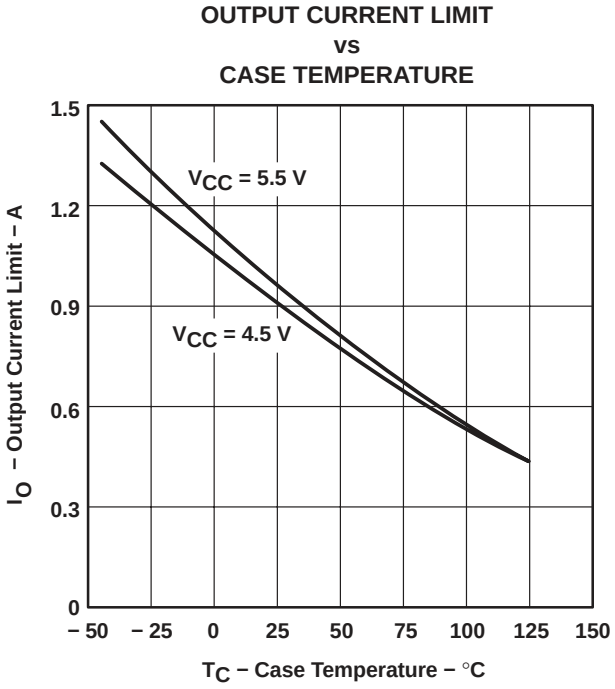
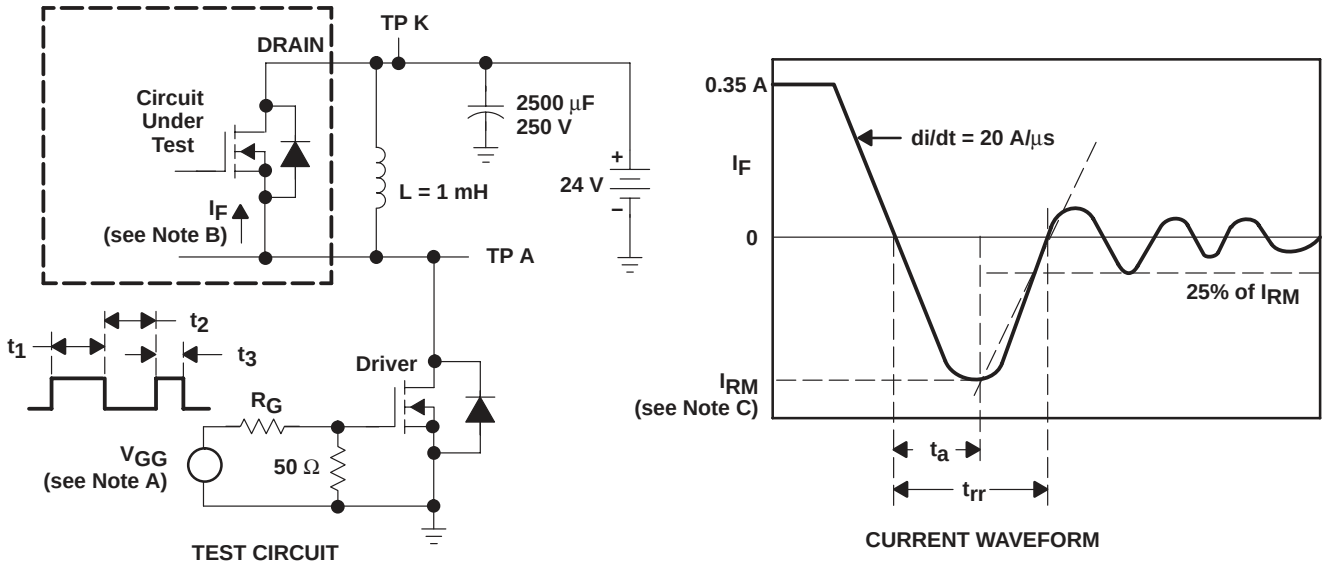


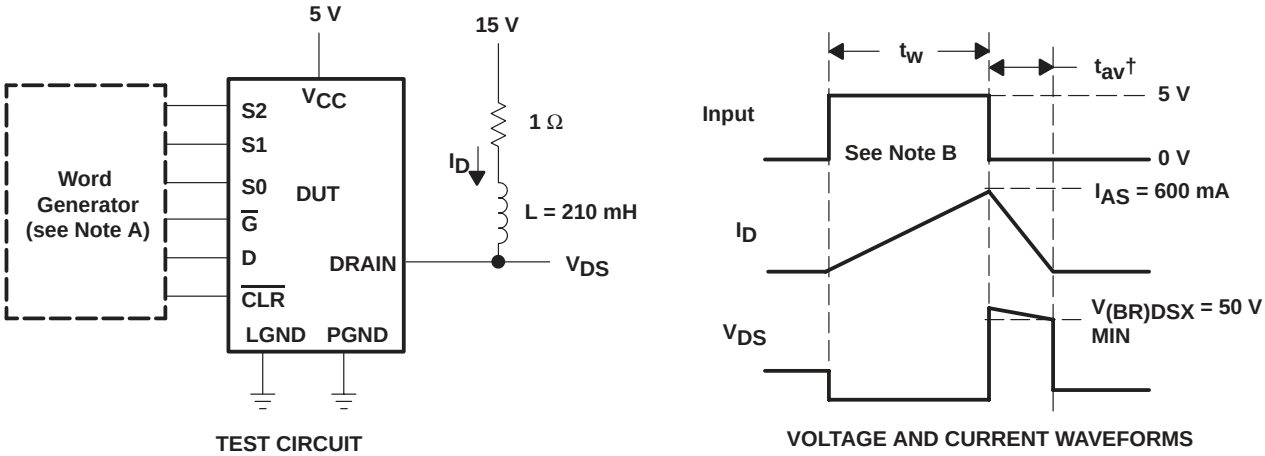

**Figure 4**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. The $V_{GG}$ amplitude and $R_G$ are adjusted for di/dt = 20 A/μs. A $V_{GG}$ double-pulse train is used to set $I_F$ = 0.35 A, where $t_1$ = 10 μs, $t_2$ = 7 μs, and $t_3$ = 3 μs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
C. $I_{RM}$ = maximum recovery current

**Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode**




† Non-JEDEC symbol for avalanche time.

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O$ = 50 Ω.
B. Input pulse duration, $t_w$, is increased until peak current $I_{AS}$ = 600 mA.
Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av})/2$ = 75 mJ.

**Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms**



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

## TYPICAL CHARACTERISTICS

**MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY**

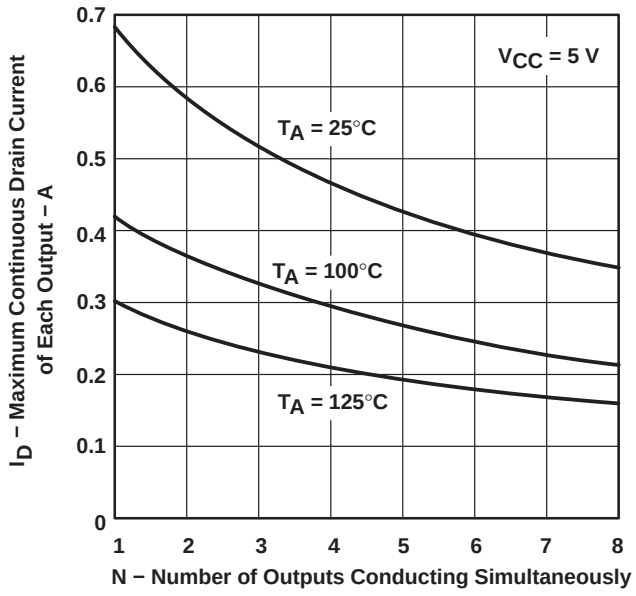



Figure 7

**MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY**

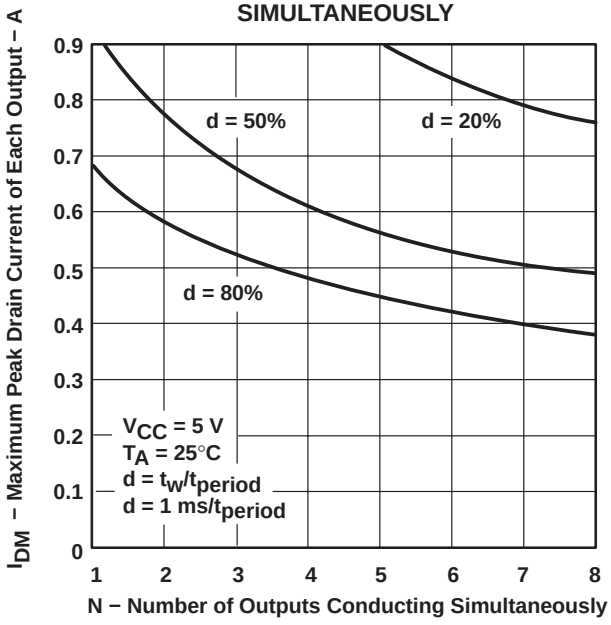



Figure 8

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT**

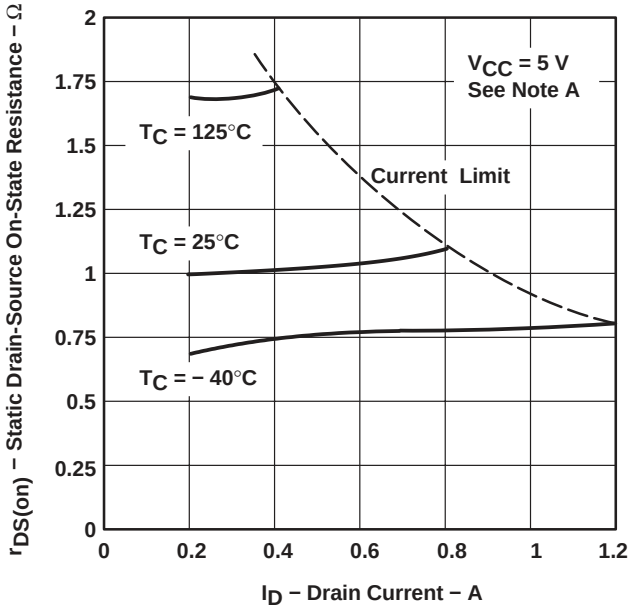



Figure 9

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE**

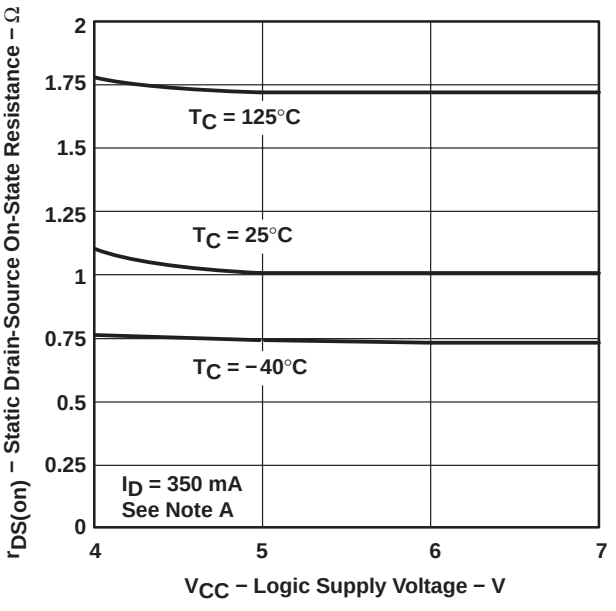
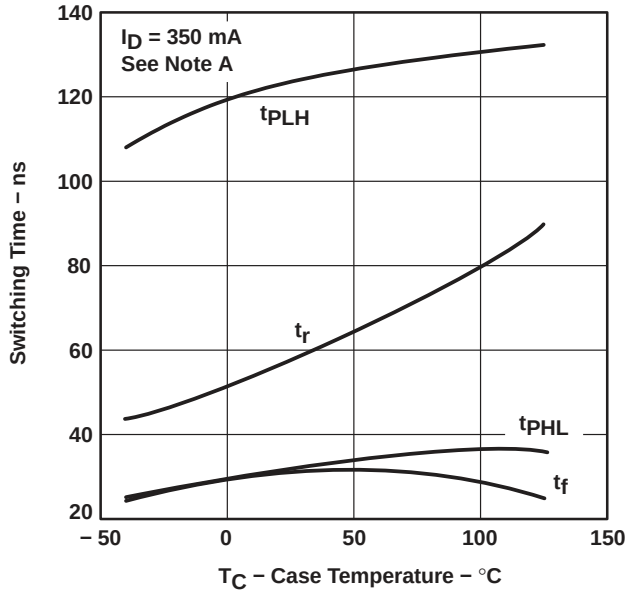



Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

## TYPICAL CHARACTERISTICS

**SWITCHING TIME vs CASE TEMPERATURE**

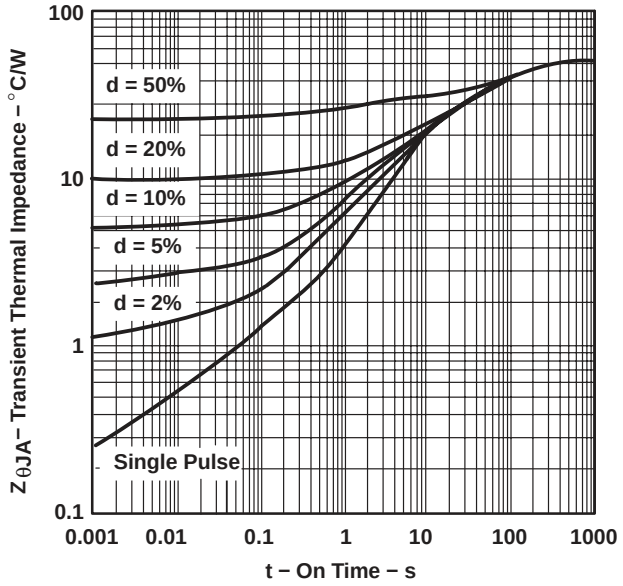



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

**Figure 11**

## THERMAL INFORMATION

**NE PACKAGE TRANSIENT THERMAL IMPEDANCE vs ON TIME**




The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left|\frac{t_w}{t_c}\right| R_{\theta JA} + \left|1 - \frac{t_w}{t_c}\right| Z_\theta(t_w + t_c) + Z_\theta(t_w) - Z_\theta(t_c)$$

Where:

$Z_\theta(t_w)$ = the single-pulse thermal impedance for t = $t_w$ seconds

$Z_\theta(t_c)$ = the single-pulse thermal impedance for t = $t_c$ seconds

$Z_\theta(t_w + t_c)$ = the single-pulse thermal impedance for t = $t_w + t_c$ seconds

$d = t_w/t_c$

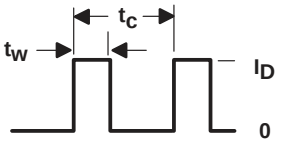



**Figure 12**



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPIC6A259DW | ACTIVE | SOIC | DW | 24 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TPIC6A259 | Samples |
| TPIC6A259DWG4 | ACTIVE | SOIC | DW | 24 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TPIC6A259 | Samples |
| TPIC6A259DWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TPIC6A259 | Samples |
| TPIC6A259NE | ACTIVE | PDIP | NE | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TPIC6A259NE | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

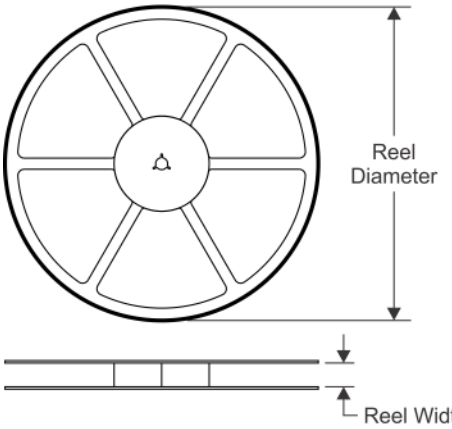
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

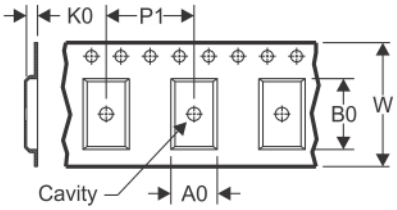
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

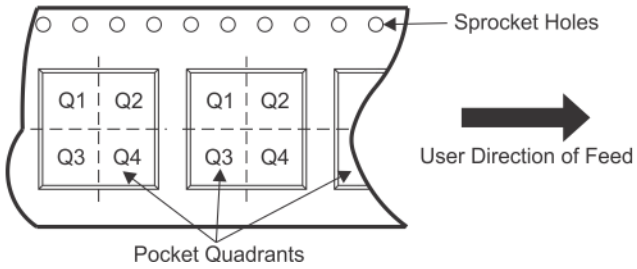



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

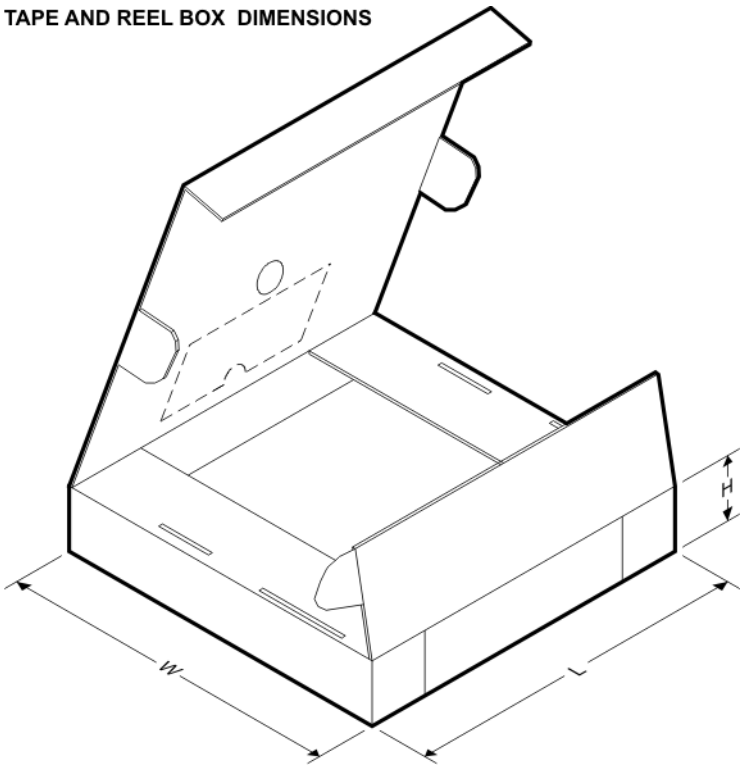
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPIC6A259DWRG4 | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

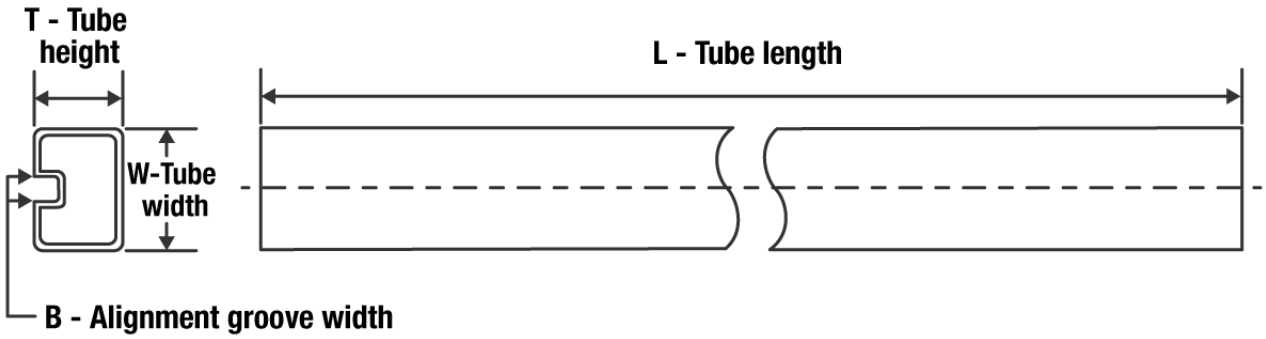
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPIC6A259DWRG4 | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |

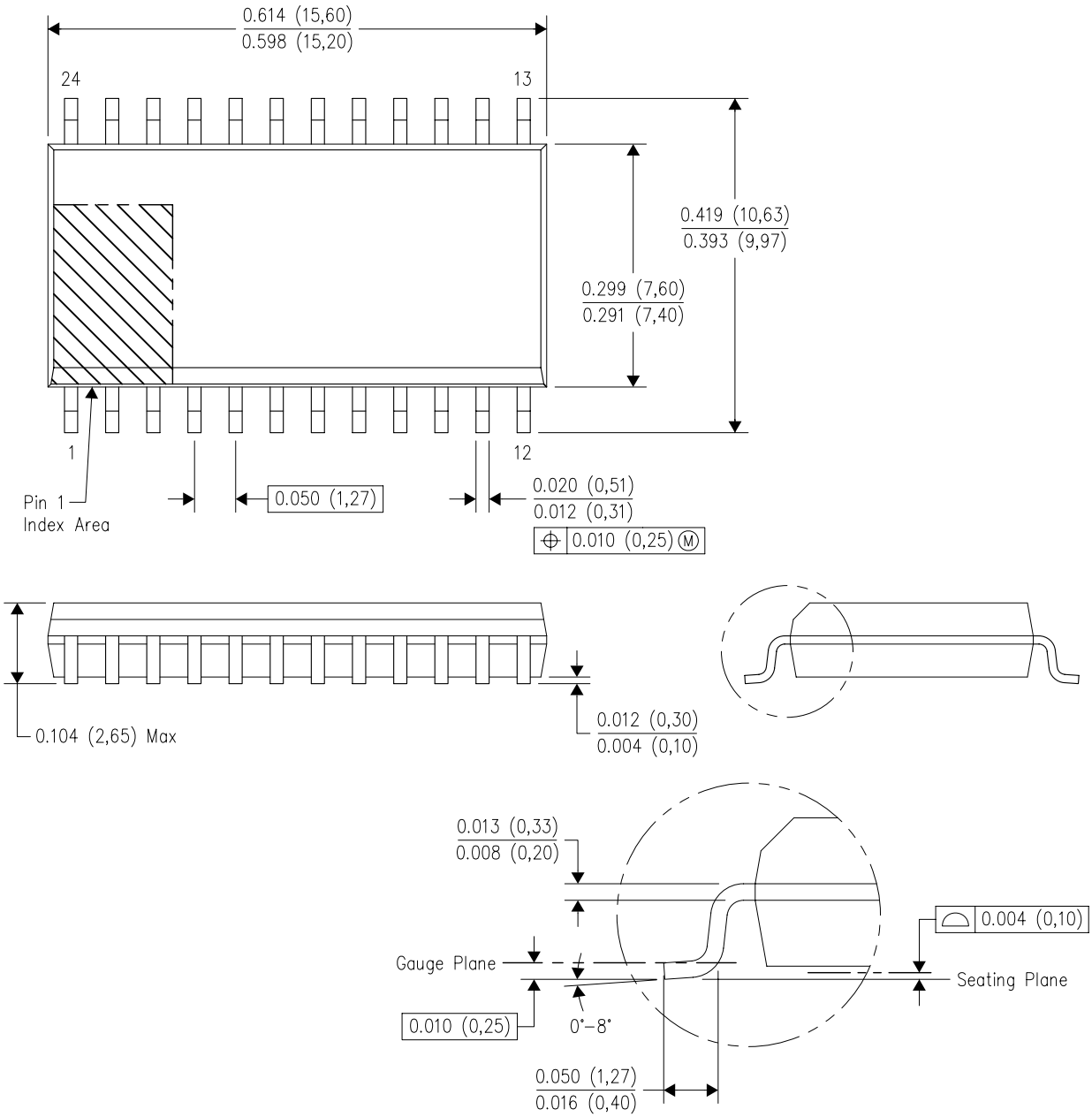
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPIC6A259DW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| TPIC6A259DWG4 | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| TPIC6A259NE | NE | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265