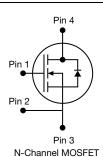
Vishay Siliconix

HALOGEN FREE

## **E Series Power MOSFET with Fast Body Diode**

PRODUCT SUMMARY					
V <sub>DS</sub> (V) at T <sub>J</sub> max.	650				
R <sub>DS(on)</sub> typ. (Ω) at 25 °C	V <sub>GS</sub> = 10 V 0.123				
Q <sub>g</sub> max. (nC)	120				
Q <sub>gs</sub> (nC)	16				
Q <sub>gd</sub> (nC)	33				
Configuration	Single				





#### **FEATURES**

- Completely lead (Pb)-free device
- Low figure-of-merit (FOM) Ron x Qg
- Low input capacitance (C<sub>iss</sub>)
- · Reduced switching and conduction losses
- Ultra low gate charge (Q<sub>q</sub>)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912"><u>www.vishav.com/doc?99912</u></a>

#### **APPLICATIONS**

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

ORDERING INFORMATION	
Package	PowerPAK 8 x 8
Lead (Pb)-free and Halogen-free	SiHH26N60EF-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T	C = 25 °C, unless otherv	/ise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	V <sub>DS</sub>	600	V		
Gate-Source Voltage	V <sub>GS</sub>	± 30	7 v		
Continuous Drain Current (T <sub>.I</sub> = 150 °C)	$V_{GS}$ at 10 V $T_{C} = 25 ^{\circ}\text{C}$	I-	24	А	
Continuous Drain Gunerit (1) = 130 G)	$T_C = 100  ^{\circ}$	ID	15		
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	67			
Linear Derating Factor		1.6	W/°C		
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	353	mJ		
Maximum Power Dissipation	P <sub>D</sub>	202	W		
Operating Junction and Storage Temperature Ra	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C		
Drain-Source Voltage Slope T <sub>J</sub> = 125 °C		dV/dt	70	V/ns	
Reverse Diode dV/dt <sup>c</sup>	uv/at	14	) v/ris		

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b.  $V_{DD}$  = 140 V, starting  $T_J$  = 25 °C, L = 28.2 mH,  $R_g$  = 25  $\Omega$ ,  $I_{AS}$  = 5 A.
- c.  $I_{SD} \le I_D$ , dI/dt = 100 A/ $\mu$ s, starting  $T_J = 25$  °C.



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THERMAL RESISTANCE RATINGS					
PARAMETER SYMBOL TYP. MAX. UNIT					
Maximum Junction-to-Ambient	R <sub>thJA</sub>	38	50	°C/W	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	0.48	0.62	C/VV	

PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static		•		•			
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> =	= 0 V, I <sub>D</sub> = 250 μA	600	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I <sub>D</sub> = 10 mA	-	0.58	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> =	· V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Octo Corres Laslana	I <sub>GSS</sub>	,	V <sub>GS</sub> = ± 20 V		-	± 100	nA
Gate-Source Leakage		,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
Z. o. O. I. Vallana Buria O anal		V <sub>DS</sub> =	480 V, V <sub>GS</sub> = 0 V	-	-	1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 480 V	, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	500	μA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 13 A	-	0.123	0.141	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub>	= 30 V, I <sub>D</sub> = 13 A	-	9.5	-	S
Dynamic		•					
Input Capacitance	C <sub>iss</sub>		$V_{GS} = 0 V$ ,	-	2744	-	
Output Capacitance	C <sub>oss</sub>	,	V <sub>DS</sub> = 100 V,	-	126	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		f = 1 MHz	-	7	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	., .,	//. 400 // // O //	-	82	-	pF
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$	$V_{DS} = 0$	/ to 480 V, V <sub>GS</sub> = 0 V	-	357	-	
Total Gate Charge	Qg			-	80	120	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$I_D = 13 \text{ A}, V_{DS} = 480 \text{ V}$	-	16	-	nC
Gate-Drain Charge	Q <sub>gd</sub>			-	33	-	
Turn-On Delay Time	t <sub>d(on)</sub>			-	25	50	
Rise Time	t <sub>r</sub>	V <sub>DD</sub> =	: 480 V, I <sub>D</sub> = 13 A,	-	46	92	
Turn-Off Delay Time	t <sub>d(off)</sub>		$= 10 \text{ V, } R_g = 9.1 \Omega$	-	93	140	ns
Fall Time	t <sub>f</sub>	7		-	56	84	1
Gate Input Resistance	$R_g$	f = 1	MHz, open drain	0.3	0.6	1.2	Ω
Drain-Source Body Diode Characteristic				•	•	•	
Continuous Source-Drain Diode Current	Is	MOSFET sym showing the	bol	-	-	24	_
Pulsed Diode Forward Current	I <sub>SM</sub>	integral revers p - n junction		-	-	67	A
Diode Forward Voltage	V <sub>SD</sub>	$T_J = 25  ^{\circ}\text{C},  I_S = 13  \text{A},  V_{GS} = 0  \text{V}$		-	0.9	1.2	V
Reverse Recovery Time	t <sub>rr</sub>			-	146	292	ns
Reverse Recovery Charge	Q <sub>rr</sub>		5 °C, I <sub>F</sub> = I <sub>S</sub> = 13 A, 100 A/µs, V <sub>B</sub> = 25 V	-	0.9	1.8	μC
Reverse Recovery Current	I <sub>RRM</sub>		100 AV µS, VR = 20 V	-	12	-	Α

#### Notes

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ . b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .



#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

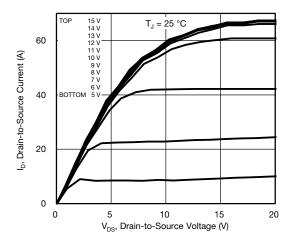


Fig. 1 - Typical Output Characteristics

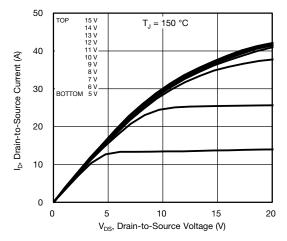


Fig. 2 - Typical Output Characteristics

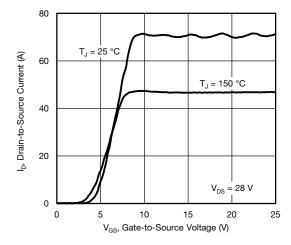


Fig. 3 - Typical Transfer Characteristics

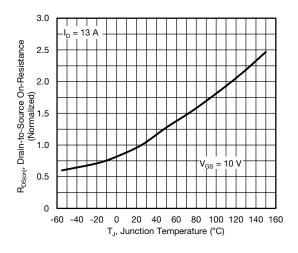


Fig. 4 - Normalized On-Resistance vs. Temperature

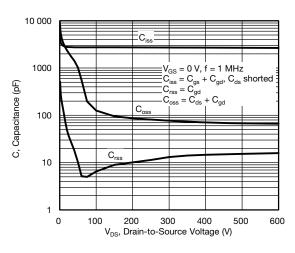


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

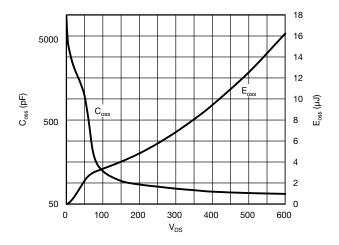


Fig. 6 -  $C_{OSS}$  and  $E_{OSS}$  vs.  $V_{DS}$ 



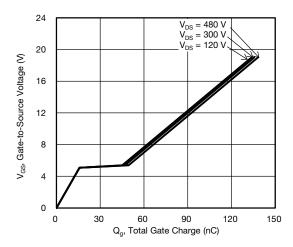


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

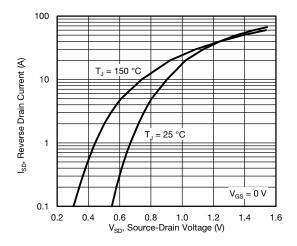


Fig. 8 - Typical Source-Drain Diode Forward Voltage

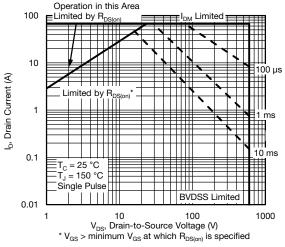


Fig. 9 - Maximum Safe Operating Area

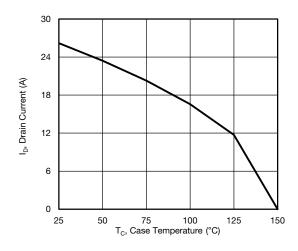


Fig. 10 - Maximum Drain Current vs. Case Temperature

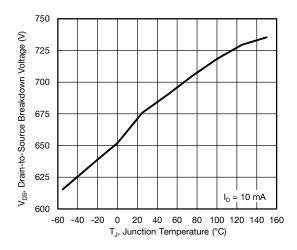


Fig. 11 - Temperature vs. Drain-to-Source Voltage



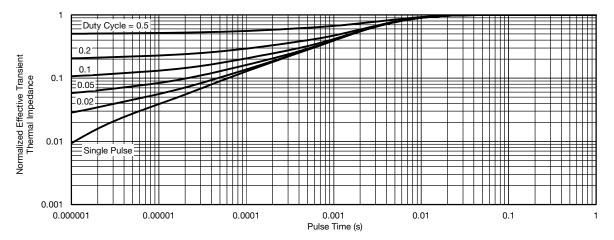


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

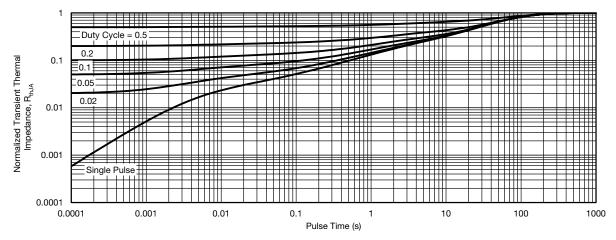


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

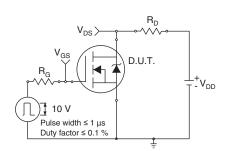


Fig. 14 - Switching Time Test Circuit

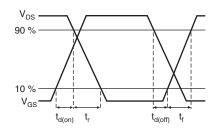


Fig. 15 - Switching Time Waveforms

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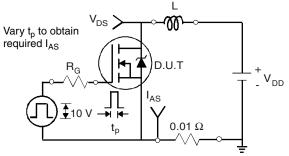


Fig. 16 - Unclamped Inductive Test Circuit

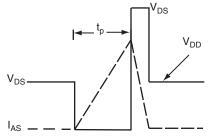


Fig. 17 - Unclamped Inductive Waveforms



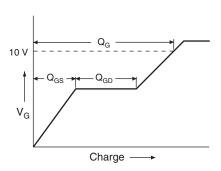


Fig. 18 - Basic Gate Charge Waveform

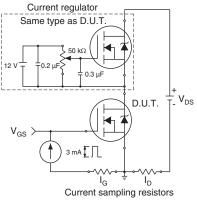
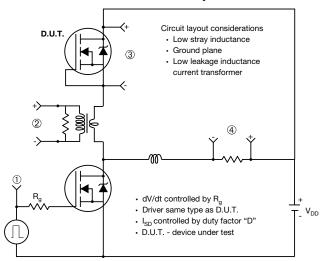


Fig. 19 - Gate Charge Test Circuit

#### Peak Diode Recovery dV/dt Test Circuit



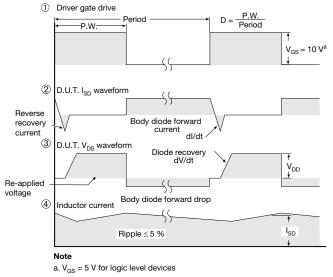


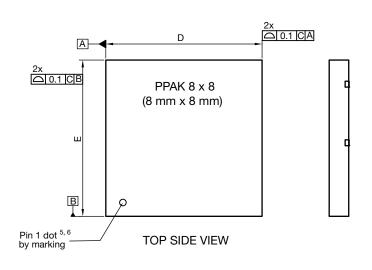
Fig. 20 - For N-Channel

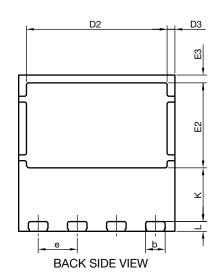
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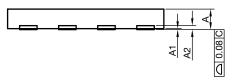


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## PowerPAK® 8 x 8 Case Outline







DIM	MILLIMETERS			INCHES			
DIM. MIN.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.95	1.00	1.05	0.037	0.039	0.041	
A1	0.00	-	0.05	0.000	-	0.002	
A2	020 ref.		0.008 ref.				
b	0.95	1.00	1.05	0.037	0.039	0.041	
D	7.90	8.00	8.10	0.311	0.315	0.319	
D2	7.10	7.20	7.30	0.280	0.283	0.287	
D3	0.40 BSC		0.016 BSC				
е	2.00 BSC		0.079 BSC				
E	7.90	8.00	8.10	0.311	0.315	0.319	
E2	4.30	4.35	4.40	0.169	0.171	0.173	
E3	0.40 BSC		0.016 BSC				
K	2.75 BSC		0.108 BSC				
L	0.45	0.50	0.55	0.018	0.020	0.022	
N <sup>(3)</sup>	8				8		

#### Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5 M 1994
- (3) N is the number of terminals
- (4) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (5) Exact shape and size of this feature is optional

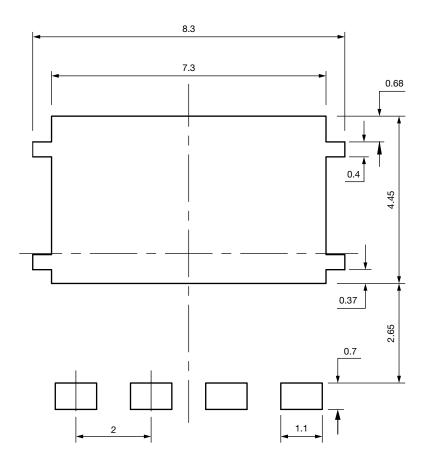
ECN: E20-0518-Rev. B, 28-Sep-2020

DWG: 6041

Revision: 28-Sep-2020 1 Document Number: 67859



# Recommended Minimum PADs for PowerPAK® 8 mm x 8 mm



Dimensions in millimeters



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